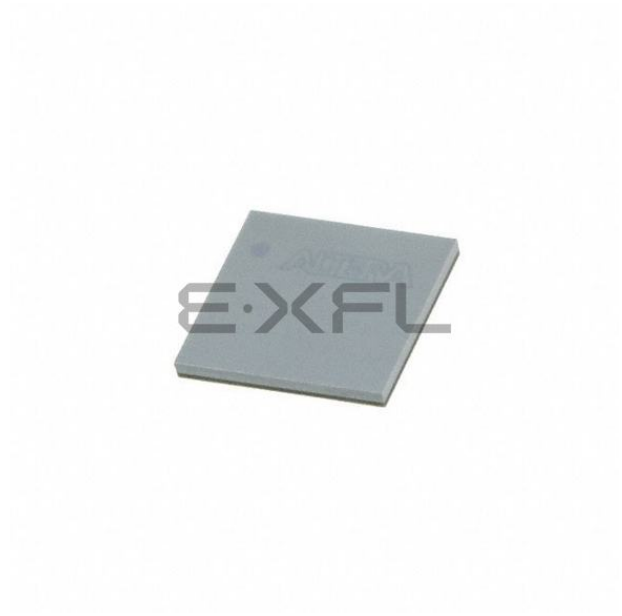

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	125
Number of Logic Elements/Cells	2000
Total RAM Bits	110592
Number of I/O	27
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	36-UFBGA, WLCSP
Supplier Device Package	36-WLCSP (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10m02dcv36c7g

Operating Conditions

Intel MAX 10 devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Intel MAX 10 devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions for Intel MAX 10 devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Caution: Conditions outside the range listed in the absolute maximum ratings tables may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Single Supply Devices Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings for Intel MAX 10 Single Supply Devices

Symbol	Parameter	Min	Max	Unit
V_{CC_ONE}	Supply voltage for core and periphery through on-die voltage regulator	–0.5	3.9	V
V_{CCIO}	Supply voltage for input and output buffers	–0.5	3.9	V
V_{CCA}	Supply voltage for phase-locked loop (PLL) regulator and analog-to-digital converter (ADC) block (analog)	–0.5	3.9	V

Dual Supply Devices Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings for Intel MAX 10 Dual Supply Devices

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply voltage for core and periphery	–0.5	1.63	V
V_{CCIO}	Supply voltage for input and output buffers	–0.5	3.9	V
V_{CCA}	Supply voltage for PLL regulator (analog)	–0.5	3.41	V

continued...

Condition (V)	Overshoot Duration as % of High Time	Unit
4.32	2.6	%
4.37	1.6	%
4.42	1.0	%
4.47	0.6	%
4.52	0.3	%
4.57	0.2	%

Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Intel MAX 10 devices. The tables list the steady-state voltage values expected from Intel MAX 10 devices. Power supply ramps must all be strictly monotonic, without plateaus.

Single Supply Devices Power Supplies Recommended Operating Conditions

Table 6. Power Supplies Recommended Operating Conditions for Intel MAX 10 Single Supply Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CC_ONE}(1)	Supply voltage for core and periphery through on-die voltage regulator	—	2.85/3.135	3.0/3.3	3.15/3.465	V
V_{CCIO}(2)	Supply voltage for input and output buffers	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V

continued...

(1) V_{CCA} must be connected to V_{CC_ONE} through a filter.

(2) V_{CCIO} for all I/O banks must be powered up during user mode because V_{CCIO} I/O banks are used for the ADC and I/O functionalities.

Table 24. Differential HSTL and HSUL I/O Standards Specifications for Intel MAX 10 Devices

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.85	—	0.95	0.85	—	0.95	0.4
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.71	—	0.79	0.71	—	0.79	0.4
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO}	0.48 × V_{CCIO}	0.5 × V_{CCIO}	0.52 × V_{CCIO}	0.48 × V_{CCIO}	0.5 × V_{CCIO}	0.52 × V_{CCIO}	0.3
HSUL-12	1.14	1.2	1.3	0.26	—	0.5 × V_{CCIO} – 0.12	0.5 × V_{CCIO}	0.5 × V_{CCIO} + 0.12	0.4 × V_{CCIO}	0.5 × V_{CCIO}	0.6 × V_{CCIO}	0.44

Differential I/O Standards Specifications

Table 25. Differential I/O Standards Specifications for Intel MAX 10 Devices

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)		V_{ICM} (V) (18)			V_{OD} (mV) (19)(20)			V_{OS} (V) (19)		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVPECL (21)	2.375	2.5	2.625	100	—	0.05	D_{MAX} ≤ 500 Mbps	1.8	—	—	—	—	—	—
						0.55	500 Mbps ≤ D_{MAX} ≤ 700 Mbps	1.8						
						1.05	D_{MAX} > 700 Mbps	1.55						
LVDS	2.375	2.5	2.625	100	—	0.05	D_{MAX} ≤ 500 Mbps	1.8	247	—	600	1.125	1.25	1.375
						0.55	500 Mbps ≤ D_{MAX} ≤ 700 Mbps	1.8						

continued...

(18) V_{IN} range: 0 V ≤ V_{IN} ≤ 1.85 V.

(19) R_L range: 90 ≤ R_L ≤ 110 Ω.

(20) Low V_{OD} setting is only supported for RSDS standard.

(21) LVPECL input standard is only supported at clock input. Output standard is not supported.

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)		V_{ICM} (V) (18)			V_{OD} (mV) (19)(20)			V_{OS} (V) (19)		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
						1.05	D_{MAX} > 700 Mbps	1.55						
BLVDS (22)	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—
mini-LVDS (23)	2.375	2.5	2.625	—	—	—	—	—	300	—	600	1	1.2	1.4
RSDS (23)	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.5
PPDS (Row I/Os) (23)	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.4
TMDS(24)	2.375	2.5	2.625	100	—	0.05	D_{MAX} ≤ 500 Mbps	1.8	—	—	—	—	—	—
						0.55	500 Mbps ≤ D_{MAX} ≤ 700 Mbps	1.8						
						1.05	D_{MAX} > 700 Mbps	1.55						
Sub-LVDS (25)	1.71	1.8	1.89	100	—	0.55	—	1.25	(26)			0.8	0.9	1
SLVS	2.375	2.5	2.625	100	—	0.05	—	1.1	(26)			(27)		

continued...

(18) V_{IN} range: 0 V ≤ V_{IN} ≤ 1.85 V.
(19) R_L range: 90 ≤ R_L ≤ 110 Ω.
(20) Low V_{OD} setting is only supported for RSDS standard.

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)		V_{ICM} (V) (18)			V_{OD} (mV) (19)(20)			V_{OS} (V) (19)		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
HiSpi	2.375	2.5	2.625	100	—	0.05	D_{MAX} ≤ 500 Mbps	1.8	—	—	—	—	—	—
						0.55	500 Mbps ≤ D_{MAX} ≤ 700 Mbps	1.8						
						1.05	D_{MAX} > 700 Mbps	1.55						

Related Information

Intel MAX 10 LVDS SERDES I/O Standards Support, Intel MAX 10 High-Speed LVDS I/O User Guide
Provides the list of I/O standards supported in single supply and dual supply devices.

Switching Characteristics

This section provides the performance characteristics of Intel MAX 10 core and periphery blocks.

(18) V_{IN} range: 0 V ≤ V_{IN} ≤ 1.85 V.
(19) R_L range: 90 ≤ R_L ≤ 110 Ω.
(20) Low V_{OD} setting is only supported for RSDS standard.

(22) No fixed V_{IN} , V_{OD} , and V_{OS} specifications for Bus LVDS (BLVDS). They are dependent on the system topology.

(23) Mini-LVDS, RSDS, and Point-to-Point Differential Signaling (PPDS) standards are only supported at the output pins for Intel MAX 10 devices.

(24) Supported with requirement of an external level shift

(25) Sub-LVDS input buffer is using 2.5 V differential buffer.

(26) Differential output depends on the values of the external termination resistors.

(27) Differential output offset voltage depends on the values of the external termination resistors.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{VCO} (29)	PLL internal voltage-controlled oscillator (VCO) operating range	—	600	—	1300	MHz
f_{INDUTY}	Input clock duty cycle	—	40	—	60	%
$t_{INJITTER\_CCJ}$ (30)	Input clock cycle-to-cycle jitter	F_{INPFD} ≥ 100 MHz	—	—	0.15	UI
		F_{INPFD} < 100 MHz	—	—	±750	ps
f_{OUT_EXT} (28)	PLL output frequency for external clock output	—	—	—	472.5	MHz
f_{OUT}	PLL output frequency to global clock	–6 speed grade	—	—	472.5	MHz
		–7 speed grade	—	—	450	MHz
		–8 speed grade	—	—	402.5	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output	Duty cycle set to 50%	45	50	55	%
t_{LOCK}	Time required to lock from end of device configuration	—	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically	After switchover, reconfiguring any non-post-scale counters or delays, or when `areset` is deasserted	—	—	1	ms
$t_{OUTJITTER\_PERIOD\_IO}$ (31)	Regular I/O period jitter	F_{OUT} ≥ 100 MHz	—	—	650	ps
		F_{OUT} < 100 MHz	—	—	75	mUI
$t_{OUTJITTER\_CCJ\_IO}$ (31)	Regular I/O cycle-to-cycle jitter	F_{OUT} ≥ 100 MHz	—	—	650	ps
		F_{OUT} < 100 MHz	—	—	75	mUI

continued...

(29) The VCO frequency reported by the Intel Quartus Prime software in the PLL summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

(30) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source, which is less than 200 ps.

(31) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied.

Internal Oscillator Specifications

Table 32. Internal Oscillator Frequencies for Intel MAX 10 Devices

You can access to the internal oscillator frequencies in this table. The duty cycle of internal oscillator is approximately 45%–55%.

Device	Frequency			Unit
	Minimum	Typical	Maximum	
10M02	55	82	116	MHz
10M04				
10M08				
10M16				
10M25				
10M40	35	52	77	MHz
10M50				

UFM Performance Specifications

Table 33. UFM Performance Specifications for Intel MAX 10 Devices

Block	Mode	Interface	Device	Frequency		Unit
				Minimum	Maximum	
UFM	Avalon®-MM slave	Parallel (33)	10M02 (34)	3.43	7.25	MHz
			10M04, 10M08, 10M16, 10M25, 10M40, 10M50	5	116	MHz
		Serial (34)	10M02, 10M04, 10M08, 10M16, 10M25	3.43	7.25	MHz
			10M40, 10M50	2.18	4.81	MHz

(33) Clock source is derived from user, except for 10M02 device.

(34) Clock source is derived from 1/16 of the frequency of the internal oscillator.

Parameter		Symbol	Condition	Min	Typ	Max	Unit
			Internal V_{REF}, no missing code	–1	—	1.7	LSB
	Integral non linearity	INL	—	–2	—	2	LSB
AC Accuracy	Total harmonic distortion	THD	F_{IN} = 50 kHz, F_S = 1 MHz, PLL	–70 (44)(45)(46)	—	—	dB
	Signal-to-noise ratio	SNR	F_{IN} = 50 kHz, F_S = 1 MHz, PLL	62 (47)(48)(46)	—	—	dB
	Signal-to-noise and distortion	SINAD	F_{IN} = 50 kHz, F_S = 1 MHz, PLL	61.5 (49)(50)(46)	—	—	dB
On-Chip Temperature Sensor	Temperature sampling rate	T_S	—	—	—	50	kSPS
	Absolute accuracy	—	–40 to 125°C, with 64 samples averaging (51)	—	—	±5	°C

continued...

(44) Total harmonic distortion is –65 dB for dual function pin.

(45) THD with prescalar enabled is 6dB less than the specification.

(46) When using internal V_{REF}, THD = 66 dB, SNR = 58 dB and SINAD = 57.5 dB for dedicated ADC input channels.

(47) Signal-to-noise ratio is 54 dB for dual function pin.

(48) SNR with prescalar enabled is 6dB less than the specification.

(49) Signal-to-noise and distortion is 53 dB for dual function pin.

(50) SINAD with prescalar enabled is 6dB less than the specification.

(51) For the Intel Quartus Prime software version 15.0 and later, Modular ADC Core and Modular Dual ADC Core IP cores handle the 64 samples averaging. For the Intel Quartus Prime software versions prior to 14.1, you need to implement your own averaging calculation.

True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications

Table 36. True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

True **PPDS** transmitter is only supported at bottom I/O banks. Emulated **PPDS** transmitter is supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	—	155	5	—	155	5	—	155	MHz
		×8	5	—	155	5	—	155	5	—	155	MHz
		×7	5	—	155	5	—	155	5	—	155	MHz
		×4	5	—	155	5	—	155	5	—	155	MHz
		×2	5	—	155	5	—	155	5	—	155	MHz
		×1	5	—	310	5	—	310	5	—	310	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	—	310	100	—	310	100	—	310	Mbps
		×8	80	—	310	80	—	310	80	—	310	Mbps
		×7	70	—	310	70	—	310	70	—	310	Mbps
		×4	40	—	310	40	—	310	40	—	310	Mbps
		×2	20	—	310	20	—	310	20	—	310	Mbps
		×1	10	—	310	10	—	310	10	—	310	Mbps
f_{HSCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	—	150	5	—	150	5	—	150	MHz
		×8	5	—	150	5	—	150	5	—	150	MHz
		×7	5	—	150	5	—	150	5	—	150	MHz
		×4	5	—	150	5	—	150	5	—	150	MHz
		×2	5	—	150	5	—	150	5	—	150	MHz
		×1	5	—	300	5	—	300	5	—	300	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	—	300	100	—	300	100	—	300	Mbps
		×8	80	—	300	80	—	300	80	—	300	Mbps
		×7	70	—	300	70	—	300	70	—	300	Mbps

continued...

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×4	40	—	300	40	—	300	40	—	300	Mbps
		×2	20	—	300	20	—	300	20	—	300	Mbps
		×1	10	—	300	10	—	300	10	—	300	Mbps
t_{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS[57]	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
$t_{x\ Jitter}$[58]	Output jitter (high-speed I/O performance pin)	—	—	—	425	—	—	425	—	—	425	ps
	Output jitter (low-speed I/O performance pin)	—	—	—	470	—	—	470	—	—	470	ps
t_{RISE}	Rise time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	Fall time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

(57) TCCS specifications apply to I/O banks from the same side only.

(58) TX jitter is the jitter induced from core noise and I/O switching noise.

Emulated RSDS_E_1R Transmitter Timing Specifications

Table 39. Emulated RSDS_E_1R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

Emulated **RSDS_E_1R** transmitter is supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	—	85	5	—	85	5	—	85	MHz
		×8	5	—	85	5	—	85	5	—	85	MHz
		×7	5	—	85	5	—	85	5	—	85	MHz
		×4	5	—	85	5	—	85	5	—	85	MHz
		×2	5	—	85	5	—	85	5	—	85	MHz
		×1	5	—	170	5	—	170	5	—	170	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	—	170	100	—	170	100	—	170	Mbps
		×8	80	—	170	80	—	170	80	—	170	Mbps
		×7	70	—	170	70	—	170	70	—	170	Mbps
		×4	40	—	170	40	—	170	40	—	170	Mbps
		×2	20	—	170	20	—	170	20	—	170	Mbps
		×1	10	—	170	10	—	170	10	—	170	Mbps
f_{HSCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	—	85	5	—	85	5	—	85	MHz
		×8	5	—	85	5	—	85	5	—	85	MHz
		×7	5	—	85	5	—	85	5	—	85	MHz
		×4	5	—	85	5	—	85	5	—	85	MHz
		×2	5	—	85	5	—	85	5	—	85	MHz
		×1	5	—	170	5	—	170	5	—	170	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	—	170	100	—	170	100	—	170	Mbps
		×8	80	—	170	80	—	170	80	—	170	Mbps
		×7	70	—	170	70	—	170	70	—	170	Mbps

continued...

Symbol	Parameter	Mode	–C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{RISE}	Rise time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	Fall time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

Dual Supply Devices True LVDS Transmitter Timing Specifications

Table 42. True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

True **LVDS** transmitter is only supported at the bottom I/O banks.

Symbol	Parameter	Mode	–I6			–A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	Input clock frequency	×10	5	—	360	5	—	340	5	—	310	5	—	300	MHz
		×8	5	—	360	5	—	360	5	—	320	5	—	320	MHz
		×7	5	—	360	5	—	340	5	—	310	5	—	300	MHz
		×4	5	—	360	5	—	350	5	—	320	5	—	320	MHz
		×2	5	—	360	5	—	350	5	—	320	5	—	320	MHz
		×1	5	—	360	5	—	350	5	—	320	5	—	320	MHz
HSIODR	Data rate	×10	100	—	720	100	—	680	100	—	620	100	—	600	Mbps
		×8	80	—	720	80	—	720	80	—	640	80	—	640	Mbps
		×7	70	—	720	70	—	680	70	—	620	70	—	600	Mbps
		×4	40	—	720	40	—	700	40	—	640	40	—	640	Mbps
		×2	20	—	720	20	—	700	20	—	640	20	—	640	Mbps

continued...

Symbol	Parameter	Mode	–I6			–A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×1	10	—	360	10	—	350	10	—	320	10	—	320	Mbps
t_{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	45	—	55	%
TCCS(65)	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	—	—	300	ps
$t_{x\ Jitter}$(66)	Output jitter	—	—	—	380	—	—	380	—	—	380	—	—	380	ps
t_{RISE}	Rise time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	Fall time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	—	—	1	ms

(65) TCCS specifications apply to I/O banks from the same side only.

(66) TX jitter is the jitter induced from core noise and I/O switching noise.

Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications

Single Supply Devices Emulated LVDS_E_3R Transmitter Timing Specifications

Table 43. Emulated LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices

Emulated **LVDS_E_3R** transmitters are supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	–C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	—	142.5	5	—	100	5	—	100	MHz
		×8	5	—	142.5	5	—	100	5	—	100	MHz
		×7	5	—	142.5	5	—	100	5	—	100	MHz
		×4	5	—	142.5	5	—	100	5	—	100	MHz
		×2	5	—	142.5	5	—	100	5	—	100	MHz
		×1	5	—	285	5	—	200	5	—	200	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	—	285	100	—	200	100	—	200	Mbps
		×8	80	—	285	80	—	200	80	—	200	Mbps
		×7	70	—	285	70	—	200	70	—	200	Mbps
		×4	40	—	285	40	—	200	40	—	200	Mbps
		×2	20	—	285	20	—	200	20	—	200	Mbps
		×1	10	—	285	10	—	200	10	—	200	Mbps
f_{HSCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	—	100	5	—	100	5	—	100	MHz
		×8	5	—	100	5	—	100	5	—	100	MHz
		×7	5	—	100	5	—	100	5	—	100	MHz
		×4	5	—	100	5	—	100	5	—	100	MHz
		×2	5	—	100	5	—	100	5	—	100	MHz
		×1	5	—	200	5	—	200	5	—	200	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	—	200	100	—	200	100	—	200	Mbps

continued...

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7		–A7		–C8		Unit
			Min	Max	Min	Max	Min	Max	
	Sampling window (low-speed I/O performance pin)	—	—	910	—	910	—	910	ps
$t_{x\ Jitter}$[72]	Input jitter	—	—	500	—	500	—	500	ps
t_{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	1	—	1	—	1	ms

Memory Standards Supported by the Soft Memory Controller

Table 47. Memory Standards Supported by the Soft Memory Controller for Intel MAX 10 Devices

Contact your local sales representatives for access to the -I6 or -A6 speed grade devices in the Intel Quartus Prime software.

External Memory Interface Standard	Rate Support	Speed Grade	Voltage (V)	Max Frequency (MHz)
DDR3 SDRAM	Half	–I6	1.5	303
DDR3L SDRAM	Half	–I6	1.35	303
DDR2 SDRAM	Half	–I6	1.8	200
		–I7 and –C7		167
LPDDR2[73]	Half	–I6	1.2	200[74]

Related Information

External Memory Interface Spec Estimator
Provides the specific details of the memory standards supported.

(72) TX jitter is the jitter induced from core noise and I/O switching noise.

(73) Intel MAX 10 devices support only single-die LPDDR2.

(74) To achieve the specified performance, constrain the memory device I/O and core power supply variation to within ±3%. By default, the frequency is 167 MHz.

JTAG Timing Parameters

Table 49. JTAG Timing Parameters for Intel MAX 10 Devices

The values are based on C_L = 10 pF of TDO.

The affected Boundary Scan Test (BST) instructions are SAMPLE/PRELOAD, EXTEST, INTEST, and CHECK_STATUS.

Symbol	Parameter	Non-BST and non-CONFIG_IO Operation		BST and CONFIG_IO Operation		Unit
		Minimum	Maximum	Minimum	Maximum	
t_{JCP}	TCK clock period	40	—	50	—	ns
t_{JCH}	TCK clock high time	20	—	25	—	ns
t_{JCL}	TCK clock low time	20	—	25	—	ns
t_{JPSU_TDI}	JTAG port setup time	2	—	2	—	ns
t_{JPSU_TMS}	JTAG port setup time	3	—	3	—	ns
t_{JPH}	JTAG port hold time	10	—	10	—	ns
t_{JPCO}	JTAG port clock to output	—	• 15 (for V_{CCIO} = 3.3, 3.0, and 2.5 V) • 17 (for V_{CCIO} = 1.8 and 1.5 V)	—	• 18 (for V_{CCIO} = 3.3, 3.0, and 2.5 V) • 20 (for V_{CCIO} = 1.8 and 1.5 V)	ns
t_{JPZX}	JTAG port high impedance to valid output	—	• 15 (for V_{CCIO} = 3.3, 3.0, and 2.5 V) • 17 (for V_{CCIO} = 1.8 and 1.5 V)	—	• 15 (for V_{CCIO} = 3.3, 3.0, and 2.5 V) • 17 (for V_{CCIO} = 1.8 and 1.5 V)	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	• 15 (for V_{CCIO} = 3.3, 3.0, and 2.5 V) • 17 (for V_{CCIO} = 1.8 and 1.5 V)	—	• 15 (for V_{CCIO} = 3.3, 3.0, and 2.5 V) • 17 (for V_{CCIO} = 1.8 and 1.5 V)	ns

Remote System Upgrade Circuitry Timing Specifications

Table 50. Remote System Upgrade Circuitry Timing Specifications for Intel MAX 10 Devices

Parameter	Device	Minimum	Maximum	Unit
$t_{MAX\_RU\_CLK}$	All	—	40	MHz
$t_{RU\_nCONFIG}$	10M02, 10M04, 10M08, 10M16, 10M25	250	—	ns
	10M40, 10M50	350	—	ns
$t_{RU\_nRSTIMER}$	10M02, 10M04, 10M08, 10M16, 10M25	300	—	ns
	10M40, 10M50	500	—	ns

User Watchdog Internal Circuitry Timing Specifications

Table 51. User Watchdog Timer Specifications for Intel MAX 10 Devices

The specifications are subject to PVT changes.

Parameter	Device	Minimum	Typical	Maximum	Unit
User watchdog frequency	10M02, 10M04, 10M08, 10M16, 10M25	3.4	5.1	7.3	MHz
	10M40, 10M50	2.2	3.3	4.8	MHz

Uncompressed Raw Binary File (.rbf) Sizes

Table 52. Uncompressed .rbf Sizes for Intel MAX 10 Devices

Device	CFM Data Size (bits)	
	Without Memory Initialization	With Memory Initialization
10M02	554,000	—
10M04	1,540,000	1,880,000
10M08	1,540,000	1,880,000
10M16	2,800,000	3,430,000

continued...

Table 54. Internal Configuration Time for Intel MAX 10 Devices (Compressed .rbf)

Compression ratio depends on design complexity. The minimum value is based on the best case (25% of original `.rbf` sizes) and the maximum value is based on the typical case (70% of original `.rbf` sizes).

Device	Internal Configuration Time (ms)			
	Unencrypted/Encrypted			
	Without Memory Initialization		With Memory Initialization	
	Min	Max	Min	Max
10M02	0.3	5.2	—	—
10M04	0.6	10.7	1.0	13.9
10M08	0.6	10.7	1.0	13.9
10M16	1.1	17.9	1.4	22.3
10M25	1.1	26.9	1.4	32.2
10M40	2.6	66.1	3.2	82.2
10M50	2.6	66.1	3.2	82.2

Internal Configuration Timing Parameter

Table 55. Internal Configuration Timing Parameter for Intel MAX 10 Devices

Symbol	Parameter	Device	Minimum	Maximum	Unit
t_{CD2UM}	`CONF_DONE` high to user mode	10M02, 10M04, 10M08, 10M16, 10M25	182.8	385.5	µs
		10M40, 10M50	275.3	605.7	µs

I/O Timing

The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

The Intel Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specific device and design after you complete place-and-route.

Programmable IOE Delay for Column Pins

Table 58. IOE Programmable Delay on Column Pins for Intel MAX 10 Devices

The incremental values for the settings are generally linear. For exact values of each setting, refer to the **Assignment Name** column in the latest version of the Intel Quartus Prime software.

The minimum and maximum offset timing numbers are in reference to setting '0' as available in the Intel Quartus Prime software.

Parameter	Paths Affected	Number of Settings	Minimum Offset	Maximum Offset							Unit
				Fast Corner		Slow Corner					
				–I7	–C8	–A6	–C7	–C8	–I7	–A7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	0.81	0.868	1.823	1.802	1.864	1.862	1.912	ns
Input delay from pin to input register	Pad to I/O input register	8	0	0.914	0.981	2.06	2.032	2.101	2.102	2.161	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.435	0.466	0.971	0.97	1.013	1.001	1.028	ns

Date	Version	Changes
		• Added –A6 speed grade in the following tables: — Intel MAX 10 Device Grades and Speed Grades Supported — Series OCT without Calibration Specifications for Intel MAX 10 Devices — Clock Tree Specifications for Intel MAX 10 Devices — Embedded Multiplier Specifications for Intel MAX 10 Devices — Memory Block Performance Specifications for Intel MAX 10 Devices — True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — Emulated RSDS_E_1R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices — IOE Programmable Delay on Row Pins for Intel MAX 10 Devices — IOE Programmable Delay on Column Pins for Intel MAX 10 Devices • Updated the maximum value for input clock cycle-to-cycle jitter ($t_{INJITTER\_CCJ}$) with F_{INPFD} < 100 MHz condition from 750 ps to ±750 ps in PLL Specifications for Intel MAX 10 Devices table. • Updated the dual supply mode performance in Embedded Multiplier Specifications for Intel MAX 10 Devices table. • Updated the dual supply mode performance in Memory Block Performance Specifications for Intel MAX 10 Devices table. • Added typical specifications in Internal Oscillator Frequencies for Intel MAX 10 Devices table. • Updated specifications in UFM Performance Specifications for Intel MAX 10 Devices table. • Updated sampling window specifications in LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices table. • Updated IOE programmable delay for row and column pins. • Changed instances of *Quartus II* to *Quartus Prime*.
June 2015	2015.06.12	• Updated the maximum values in Internal Weak Pull-Up Resistor for Intel MAX 10 Devices table. • Removed Internal Weak Pull-Up Resistor equation. • Updated the note for input resistance and input capacitance parameters in the ADC Performance Specifications table for both single supply and dual supply devices. Note: Download the SPICE models for simulation. • Added a note to AC Accuracy - THD, SNR, and SINAD parameters in the ADC Performance Specifications for Intel MAX 10 Dual Supply Devices table. Note: When using internal V_{REF}, THD = 66 dB, SNR = 58 dB and SINAD = 57.5 dB for dedicated ADC input channels. • Updated clock period jitter and cycle-to-cycle period jitter parameters in the Memory Output Clock Jitter Specifications for Intel MAX 10 Devices table.

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