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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

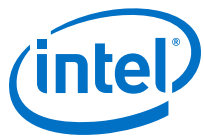
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

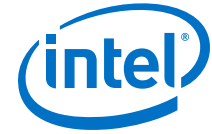
Details

Product Status	Active
Number of LABs/CLBs	125
Number of Logic Elements/Cells	2000
Total RAM Bits	110592
Number of I/O	27
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	36-UFBGA, WLCSP
Supplier Device Package	36-WLCSP (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10m02dcv36c8g



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Intel® MAX® 10 FPGA Device Datasheet

This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and timing for Intel MAX® 10 devices.

Table 1. Intel MAX 10 Device Grades and Speed Grades Supported

Device Grade	Speed Grade Supported
Commercial	–C7 –C8 (slowest)
Industrial	–I6 (fastest) –I7
Automotive	–A6 –A7

Note: The –I6 and –A6 speed grades of the Intel MAX 10 FPGA devices are not available by default in the Intel Quartus® Prime software. Contact your local Intel sales representatives for support.

Related Information

[Device Ordering Information, Intel MAX 10 FPGA Device Overview](#)

Provides more information about the densities and packages of devices in the Intel MAX 10.

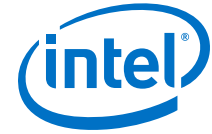
Electrical Characteristics

The following sections describe the operating conditions and power consumption of Intel MAX 10 devices.

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Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{CCA}^{(1)}$	Supply voltage for PLL regulator and ADC block (analog)	1.35 V	1.2825	1.35	1.4175	V
		1.2 V	1.14	1.2	1.26	V
		—	2.85/3.135	3.0/3.3	3.15/3.465	V

Dual Supply Devices Power Supplies Recommended Operating Conditions

Table 7. Power Supplies Recommended Operating Conditions for Intel MAX 10 Dual Supply Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CC}	Supply voltage for core and periphery	—	1.15	1.2	1.25	V
$V_{CCIO}^{(3)}$	Supply voltage for input and output buffers	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.35 V	1.2825	1.35	1.4175	V
		1.2 V	1.14	1.2	1.26	V
$V_{CCA}^{(4)}$	Supply voltage for PLL regulator (analog)	—	2.375	2.5	2.625	V
$V_{CCD_PLL}^{(5)}$	Supply voltage for PLL regulator (digital)	—	1.15	1.2	1.25	V
V_{CCA_ADC}	Supply voltage for ADC analog block	—	2.375	2.5	2.625	V
V_{CCINT}	Supply voltage for ADC digital block	—	1.15	1.2	1.25	V

⁽³⁾ V_{CCIO} for all I/O banks must be powered up during user mode because V_{CCIO} I/O banks are used for the ADC and I/O functionalities.

⁽⁴⁾ All V_{CCA} pins must be powered to 2.5 V (even when PLLs are not used), and must be powered up and powered down at the same time.

⁽⁵⁾ V_{CCD_PLL} must always be connected to V_{CC} through a decoupling capacitor and ferrite bead.

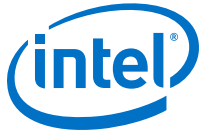


Table 11. ADC_VREF Pin Leakage Current for Intel MAX 10 Devices

Symbol	Parameter	Condition	Min	Max	Unit
I _{adc_vref}	ADC_VREF pin leakage current	Single supply mode	—	10	μA
		Dual supply mode	—	20	μA

Bus Hold Parameters

Bus hold retains the last valid logic state after the source driving it either enters the high impedance state or is removed. Each I/O pin has an option to enable bus hold in user mode. Bus hold is always disabled in configuration mode.

Table 12. Bus Hold Parameters for Intel MAX 10 Devices

Parameter	Condition	V _{CCIO} (V)												Unit
		1.2		1.5		1.8		2.5		3.0		3.3		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold low, sustaining current	V _{IN} > V _{IL} (maximum)	8	—	12	—	30	—	50	—	70	—	70	—	μA
Bus-hold high, sustaining current	V _{IN} < V _{IH} (minimum)	−8	—	−12	—	−30	—	−50	—	−70	—	−70	—	μA
Bus-hold low, overdrive current	0 V < V _{IN} < V _{CCIO}	—	125	—	175	—	200	—	300	—	500	—	500	μA
Bus-hold high, overdrive current	0 V < V _{IN} < V _{CCIO}	—	−125	—	−175	—	−200	—	−300	—	−500	—	−500	μA
Bus-hold trip point	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

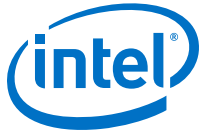


Table 15. OCT Variation after Calibration at Device Power-Up for Intel MAX 10 Devices

This table lists the change percentage of the OCT resistance with voltage and temperature.

Description	Nominal Voltage	dR/dT (%/°C)	dR/dV (%/mV)
OCT variation after calibration at device power-up	3.00	0.25	-0.027
	2.50	0.245	-0.04
	1.80	0.242	-0.079
	1.50	0.235	-0.125
	1.35	0.229	-0.16
	1.20	0.197	-0.208

Figure 1. Equation for OCT Resistance after Calibration at Device Power-Up

$$\Delta R_V = (V_2 - V_1) \times 1000 \times dR/dV$$

$$\Delta R_T = (T_2 - T_1) \times dR/dT$$

$$\text{For } \Delta R_X < 0; MF_X = 1/(|\Delta R_X|/100 + 1)$$

$$\text{For } \Delta R_X > 0; MF_X = \Delta R_X/100 + 1$$

$$MF = MF_V \times MF_T$$

$$R_{final} = R_{initial} \times MF$$

The definitions for equation are as follows:

- T_1 is the initial temperature.
- T_2 is the final temperature.
- MF is multiplication factor.
- $R_{initial}$ is initial resistance.
- R_{final} is final resistance.

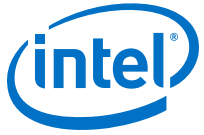
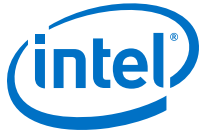


Table 19. Hysteresis Specifications for Schmitt Trigger Input for Intel MAX 10 Devices

Symbol	Parameter	Condition	Minimum	Unit
V _{HYS}	Hysteresis for Schmitt trigger input	V _{CCIO} = 3.3 V	180	mV
		V _{CCIO} = 2.5 V	150	mV
		V _{CCIO} = 1.8 V	120	mV
		V _{CCIO} = 1.5 V	110	mV



Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

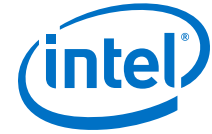
Table 21. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Intel MAX 10 Devices

I/O Standard	V _{CCIO} (V)			V _{REF} (V)			V _{TT} (V) ⁽¹⁴⁾		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	1.19	1.25	1.31	V _{REF} - 0.04	V _{REF}	V _{REF} + 0.04
SSTL-18 Class I, II	1.7	1.8	1.9	0.833	0.9	0.969	V _{REF} - 0.04	V _{REF}	V _{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 × V _{CCIO}	0.5 × V _{CCIO}	0.51 × V _{CCIO}	0.49 × V _{CCIO}	0.5 × V _{CCIO}	0.51 × V _{CCIO}
SSTL-135 Class I, II	1.283	1.35	1.45	0.49 × V _{CCIO}	0.5 × V _{CCIO}	0.51 × V _{CCIO}	0.49 × V _{CCIO}	0.5 × V _{CCIO}	0.51 × V _{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	0.85	0.9	0.95
HSTL-15 Class I, II	1.425	1.5	1.575	0.71	0.75	0.79	0.71	0.75	0.79
HSTL-12 Class I, II	1.14	1.2	1.26	0.48 × V _{CCIO} ⁽¹⁵⁾	0.5 × V _{CCIO} ⁽¹⁵⁾	0.52 × V _{CCIO} ⁽¹⁵⁾	—	0.5 × V _{CCIO}	—
				0.47 × V _{CCIO} ⁽¹⁶⁾	0.5 × V _{CCIO} ⁽¹⁶⁾	0.53 × V _{CCIO} ⁽¹⁶⁾			
HSUL-12	1.14	1.2	1.3	0.49 × V _{CCIO}	0.5 × V _{CCIO}	0.51 × V _{CCIO}	—	—	—

⁽¹⁴⁾ V_{TT} of transmitting device must track V_{REF} of the receiving device.

⁽¹⁵⁾ Value shown refers to DC input reference voltage, V_{REF(DC)}.

⁽¹⁶⁾ Value shown refers to AC input reference voltage, V_{REF(AC)}.



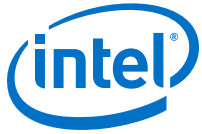
Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications

Table 22. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Intel MAX 10 Devices

To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL-15 Class I specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	$V_{IL(DC)} (V)$		$V_{IH(DC)} (V)$		$V_{IL(AC)} (V)$		$V_{IH(AC)} (V)$		$V_{OL} (V)$	$V_{OH} (V)$	$I_{OL} (mA)$	$I_{OH} (mA)$
	Min	Max	Min	Max	Min	Max	Min	Max	Max	Min		
SSTL-2 Class I	—	$V_{REF} - 0.18$	$V_{REF} + 0.18$	—	—	$V_{REF} - 0.31$	$V_{REF} + 0.31$	—	$V_{TT} - 0.57$	$V_{TT} + 0.57$	8.1	-8.1
SSTL-2 Class II	—	$V_{REF} - 0.18$	$V_{REF} + 0.18$	—	—	$V_{REF} - 0.31$	$V_{REF} + 0.31$	—	$V_{TT} - 0.76$	$V_{TT} + 0.76$	16.4	-16.4
SSTL-18 Class I	—	$V_{REF} - 0.125$	$V_{REF} + 0.125$	—	—	$V_{REF} - 0.25$	$V_{REF} + 0.25$	—	$V_{TT} - 0.475$	$V_{TT} + 0.475$	6.7	-6.7
SSTL-18 Class II	—	$V_{REF} - 0.125$	$V_{REF} + 0.125$	—	—	$V_{REF} - 0.25$	$V_{REF} + 0.25$	—	0.28	$V_{CCIO} - 0.28$	13.4	-13.4
SSTL-15 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	—	$V_{REF} - 0.175$	$V_{REF} + 0.175$	—	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	8	-8
SSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	—	$V_{REF} - 0.175$	$V_{REF} + 0.175$	—	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	16	-16
SSTL-135	—	$V_{REF} - 0.09$	$V_{REF} + 0.09$	—	—	$V_{REF} - 0.16$	$V_{REF} + 0.16$	—	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	—	—
HSTL-18 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	—	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-18 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	—	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-15 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	—	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	—	0.4	$V_{CCIO} - 0.4$	16	-16

continued...



Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	—	±50	ps
t_{ARESET}	Minimum pulse width on areset signal.	—	10	—	—	ns
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for PLLs	—	—	3.5 ⁽³²⁾	—	SCANCLK cycles
$f_{SCANCLK}$	scanclk frequency	—	—	—	100	MHz

Table 28. PLL Specifications for Intel MAX 10 Single Supply Devices

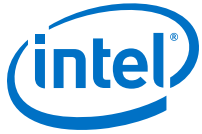
For V36 package, the PLL specification is based on single supply devices.

Symbol	Parameter	Condition	Max	Unit
$t_{OUTJITTER_PERIOD_DEDCLK}$ ⁽³¹⁾	Dedicated clock output period jitter	$F_{OUT} \geq 100$ MHz	660	ps
		$F_{OUT} < 100$ MHz	66	mUI
$t_{OUTJITTER_CCJ_DEDCLK}$ ⁽³¹⁾	Dedicated clock output cycle-to-cycle jitter	$F_{OUT} \geq 100$ MHz	660	ps
		$F_{OUT} < 100$ MHz	66	mUI

Table 29. PLL Specifications for Intel MAX 10 Dual Supply Devices

Symbol	Parameter	Condition	Max	Unit
$t_{OUTJITTER_PERIOD_DEDCLK}$ ⁽³¹⁾	Dedicated clock output period jitter	$F_{OUT} \geq 100$ MHz	300	ps
		$F_{OUT} < 100$ MHz	30	mUI
$t_{OUTJITTER_CCJ_DEDCLK}$ ⁽³¹⁾	Dedicated clock output cycle-to-cycle jitter	$F_{OUT} \geq 100$ MHz	300	ps
		$F_{OUT} < 100$ MHz	30	mUI

⁽³²⁾ With 100 MHz scanclk frequency.



Internal Oscillator Specifications

Table 32. Internal Oscillator Frequencies for Intel MAX 10 Devices

You can access to the internal oscillator frequencies in this table. The duty cycle of internal oscillator is approximately 45%–55%.

Device	Frequency			Unit
	Minimum	Typical	Maximum	
10M02	55	82	116	MHz
10M04				
10M08				
10M16				
10M25				
10M40	35	52	77	MHz
10M50				

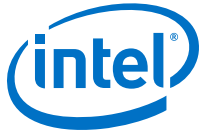
UFM Performance Specifications

Table 33. UFM Performance Specifications for Intel MAX 10 Devices

Block	Mode	Interface	Device	Frequency		Unit
				Minimum	Maximum	
UFM	Avalon®-MM slave	Parallel ⁽³³⁾	10M02 ⁽³⁴⁾	3.43	7.25	MHz
			10M04, 10M08, 10M16, 10M25, 10M40, 10M50	5	116	MHz
		Serial ⁽³⁴⁾	10M02, 10M04, 10M08, 10M16, 10M25	3.43	7.25	MHz
			10M40, 10M50	2.18	4.81	MHz

⁽³³⁾ Clock source is derived from user, except for 10M02 device.

⁽³⁴⁾ Clock source is derived from 1/16 of the frequency of the internal oscillator.



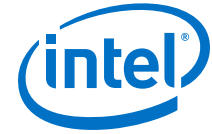
True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications

Single Supply Devices True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications

Table 37. True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices

True **RSDS** transmitter is only supported at bottom I/O banks. Emulated **RSDS** transmitter is supported at the output pin of all I/O banks.

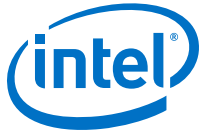
Symbol	Parameter	Mode	-I6, -A6, -C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{HSCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	—	50	5	—	50	5	—	50	MHz
		×8	5	—	50	5	—	50	5	—	50	MHz
		×7	5	—	50	5	—	50	5	—	50	MHz
		×4	5	—	50	5	—	50	5	—	50	MHz
		×2	5	—	50	5	—	50	5	—	50	MHz
		×1	5	—	100	5	—	100	5	—	100	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	—	100	100	—	100	100	—	100	Mbps
		×8	80	—	100	80	—	100	80	—	100	Mbps
		×7	70	—	100	70	—	100	70	—	100	Mbps
		×4	40	—	100	40	—	100	40	—	100	Mbps
		×2	20	—	100	20	—	100	20	—	100	Mbps
		×1	10	—	100	10	—	100	10	—	100	Mbps
f _{HSCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	—	50	5	—	50	5	—	50	MHz
		×8	5	—	50	5	—	50	5	—	50	MHz
		×7	5	—	50	5	—	50	5	—	50	MHz
		×4	5	—	50	5	—	50	5	—	50	MHz
		×2	5	—	50	5	—	50	5	—	50	MHz
		×1	5	—	100	5	—	100	5	—	100	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	—	100	100	—	100	100	—	100	Mbps
continued...												



Symbol	Parameter	Mode	-I6, -A6, -C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×8	80	—	100	80	—	100	80	—	100	Mbps
		×7	70	—	100	70	—	100	70	—	100	Mbps
		×4	40	—	100	40	—	100	40	—	100	Mbps
		×2	20	—	100	20	—	100	20	—	100	Mbps
		×1	10	—	100	10	—	100	10	—	100	Mbps
t _{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS ⁽⁵⁵⁾	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
t _x Jitter ⁽⁵⁶⁾	Output jitter (high-speed I/O performance pin)	—	—	—	425	—	—	425	—	—	425	ps
	Output jitter (low-speed I/O performance pin)	—	—	—	470	—	—	470	—	—	470	ps
t _{RISE}	Rise time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{FALL}	Fall time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

⁽⁵⁵⁾ TCCS specifications apply to I/O banks from the same side only.

⁽⁵⁶⁾ TX jitter is the jitter induced from core noise and I/O switching noise.



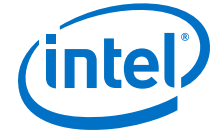
Dual Supply Devices True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications

Table 38. True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

True **RSDS** transmitter is only supported at bottom I/O banks. Emulated **RSDS** transmitter is supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	-I6, -A6, -C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{HCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	—	155	5	—	155	5	—	155	MHz
		×8	5	—	155	5	—	155	5	—	155	MHz
		×7	5	—	155	5	—	155	5	—	155	MHz
		×4	5	—	155	5	—	155	5	—	155	MHz
		×2	5	—	155	5	—	155	5	—	155	MHz
		×1	5	—	310	5	—	310	5	—	310	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	—	310	100	—	310	100	—	310	Mbps
		×8	80	—	310	80	—	310	80	—	310	Mbps
		×7	70	—	310	70	—	310	70	—	310	Mbps
		×4	40	—	310	40	—	310	40	—	310	Mbps
		×2	20	—	310	20	—	310	20	—	310	Mbps
		×1	10	—	310	10	—	310	10	—	310	Mbps
f _{HCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	—	150	5	—	150	5	—	150	MHz
		×8	5	—	150	5	—	150	5	—	150	MHz
		×7	5	—	150	5	—	150	5	—	150	MHz
		×4	5	—	150	5	—	150	5	—	150	MHz
		×2	5	—	150	5	—	150	5	—	150	MHz
		×1	5	—	300	5	—	300	5	—	300	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	—	300	100	—	300	100	—	300	Mbps
		×8	80	—	300	80	—	300	80	—	300	Mbps
		×7	70	—	300	70	—	300	70	—	300	Mbps

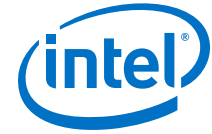
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Symbol	Parameter	Mode	-I6, -A6, -C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×4	40	—	300	40	—	300	40	—	300	Mbps
		×2	20	—	300	20	—	300	20	—	300	Mbps
		×1	10	—	300	10	—	300	10	—	300	Mbps
t _{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS ⁽⁵⁷⁾	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
t _{x Jitter} ⁽⁵⁸⁾	Output jitter (high-speed I/O performance pin)	—	—	—	425	—	—	425	—	—	425	ps
	Output jitter (low-speed I/O performance pin)	—	—	—	470	—	—	470	—	—	470	ps
t _{RISE}	Rise time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{FALL}	Fall time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

⁽⁵⁷⁾ TCCS specifications apply to I/O banks from the same side only.

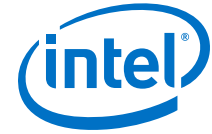
⁽⁵⁸⁾ TX jitter is the jitter induced from core noise and I/O switching noise.



Symbol	Parameter	Mode	-I6, -A6, -C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×4	40	—	170	40	—	170	40	—	170	Mbps
		×2	20	—	170	20	—	170	20	—	170	Mbps
		×1	10	—	170	10	—	170	10	—	170	Mbps
t _{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS ⁽⁵⁹⁾	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
t _{x jitter} ⁽⁶⁰⁾	Output jitter (high-speed I/O performance pin)	—	—	—	425	—	—	425	—	—	425	ps
	Output jitter (low-speed I/O performance pin)	—	—	—	470	—	—	470	—	—	470	ps
t _{RISE}	Rise time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{FALL}	Fall time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

⁽⁵⁹⁾ TCCS specifications apply to I/O banks from the same side only.

⁽⁶⁰⁾ TX jitter is the jitter induced from core noise and I/O switching noise.



Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications

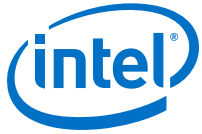
Single Supply Devices Emulated LVDS_E_3R Transmitter Timing Specifications

Table 43. Emulated LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices

Emulated **LVDS_E_3R** transmitters are supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	-C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{HCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	—	142.5	5	—	100	5	—	100	MHz
		×8	5	—	142.5	5	—	100	5	—	100	MHz
		×7	5	—	142.5	5	—	100	5	—	100	MHz
		×4	5	—	142.5	5	—	100	5	—	100	MHz
		×2	5	—	142.5	5	—	100	5	—	100	MHz
		×1	5	—	285	5	—	200	5	—	200	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	—	285	100	—	200	100	—	200	Mbps
		×8	80	—	285	80	—	200	80	—	200	Mbps
		×7	70	—	285	70	—	200	70	—	200	Mbps
		×4	40	—	285	40	—	200	40	—	200	Mbps
		×2	20	—	285	20	—	200	20	—	200	Mbps
		×1	10	—	285	10	—	200	10	—	200	Mbps
f _{HCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	—	100	5	—	100	5	—	100	MHz
		×8	5	—	100	5	—	100	5	—	100	MHz
		×7	5	—	100	5	—	100	5	—	100	MHz
		×4	5	—	100	5	—	100	5	—	100	MHz
		×2	5	—	100	5	—	100	5	—	100	MHz
		×1	5	—	200	5	—	200	5	—	200	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	—	200	100	—	200	100	—	200	Mbps

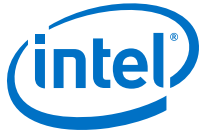
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Symbol	Parameter	Mode	-C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×8	80	—	200	80	—	200	80	—	200	Mbps
		×7	70	—	200	70	—	200	70	—	200	Mbps
		×4	40	—	200	40	—	200	40	—	200	Mbps
		×2	20	—	200	20	—	200	20	—	200	Mbps
		×1	10	—	200	10	—	200	10	—	200	Mbps
t _{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS ⁽⁶⁷⁾	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
t _{x jitter} ⁽⁶⁸⁾	Output jitter	—	—	—	1,000	—	—	1,000	—	—	1,000	ps
t _{RISE}	Rise time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{FALL}	Fall time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

(67) TCCS specifications apply to I/O banks from the same side only.

(68) TX jitter is the jitter induced from core noise and I/O switching noise.



Symbol	Parameter	Mode	-I6, -A6, -C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×7	70	—	300	70	—	300	70	—	300	Mbps
		×4	40	—	300	40	—	300	40	—	300	Mbps
		×2	20	—	300	20	—	300	20	—	300	Mbps
		×1	10	—	300	10	—	300	10	—	300	Mbps
t _{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS ⁽⁶⁹⁾	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
t _{x jitter} ⁽⁷⁰⁾	Output jitter (high-speed I/O performance pin)	—	—	—	425	—	—	425	—	—	425	ps
	Output jitter (low-speed I/O performance pin)	—	—	—	470	—	—	470	—	—	470	ps
t _{RISE}	Rise time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{FALL}	Fall time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

⁽⁶⁹⁾ TCCS specifications apply to I/O banks from the same side only.

⁽⁷⁰⁾ TX jitter is the jitter induced from core noise and I/O switching noise.

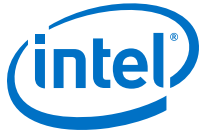


Table 56. I/O Timing for Intel MAX 10 Devices

These I/O timing parameters are for the 3.3-V LVTTTL I/O standard with the maximum drive strength and fast slew rate for 10M08DAF484 device.

Symbol	Parameter	-C7, -I7	-C8	Unit
T _{su}	Global clock setup time	-0.750	-0.808	ns
T _h	Global clock hold time	1.180	1.215	ns
T _{co}	Global clock to output delay	5.131	5.575	ns
T _{pd}	Best case pin-to-pin propagation delay through one LUT	4.907	5.467	ns

Programmable IOE Delay

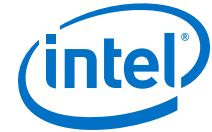
Programmable IOE Delay On Row Pins

Table 57. IOE Programmable Delay on Row Pins for Intel MAX 10 Devices

The incremental values for the settings are generally linear. For exact values of each setting, refer to the **Assignment Name** column in the latest version of the Intel Quartus Prime software.

The minimum and maximum offset timing numbers are in reference to setting '0' as available in the Intel Quartus Prime software.

Parameter	Paths Affected	Number of Settings	Minimum Offset	Maximum Offset							Unit
				Fast Corner		Slow Corner					
				−I7	−C8	−A6	−C7	−C8	−I7	−A7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	0.815	0.873	1.831	1.811	1.874	1.871	1.922	ns
Input delay from pin to input register	Pad to I/O input register	8	0	0.924	0.992	2.081	2.055	2.125	2.127	2.185	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.479	0.514	1.069	1.070	1.117	1.105	1.134	ns



Date	Version	Changes
		- Added –A6 speed grade in the following tables: - Intel MAX 10 Device Grades and Speed Grades Supported - Series OCT without Calibration Specifications for Intel MAX 10 Devices - Clock Tree Specifications for Intel MAX 10 Devices - Embedded Multiplier Specifications for Intel MAX 10 Devices - Memory Block Performance Specifications for Intel MAX 10 Devices - True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices - True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices - Emulated RSDS_E_1R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices - True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices - True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices - Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices - LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices - IOE Programmable Delay on Row Pins for Intel MAX 10 Devices - IOE Programmable Delay on Column Pins for Intel MAX 10 Devices - Updated the maximum value for input clock cycle-to-cycle jitter ($t_{INJITTER_CCJ}$) with $F_{INPFD} < 100$ MHz condition from 750 ps to ± 750 ps in PLL Specifications for Intel MAX 10 Devices table. - Updated the dual supply mode performance in Embedded Multiplier Specifications for Intel MAX 10 Devices table. - Updated the dual supply mode performance in Memory Block Performance Specifications for Intel MAX 10 Devices table. - Added typical specifications in Internal Oscillator Frequencies for Intel MAX 10 Devices table. - Updated specifications in UFM Performance Specifications for Intel MAX 10 Devices table. - Updated sampling window specifications in LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices table. - Updated IOE programmable delay for row and column pins. - Changed instances of <i>Quartus II</i> to <i>Quartus Prime</i>.
June 2015	2015.06.12	- Updated the maximum values in Internal Weak Pull-Up Resistor for Intel MAX 10 Devices table. - Removed Internal Weak Pull-Up Resistor equation. - Updated the note for input resistance and input capacitance parameters in the ADC Performance Specifications table for both single supply and dual supply devices. Note: Download the SPICE models for simulation. - Added a note to AC Accuracy - THD, SNR, and SINAD parameters in the ADC Performance Specifications for Intel MAX 10 Dual Supply Devices table. Note: When using internal V_{REF}, THD = 66 dB, SNR = 58 dB and SINAD = 57.5 dB for dedicated ADC input channels. - Updated clock period jitter and cycle-to-cycle period jitter parameters in the Memory Output Clock Jitter Specifications for Intel MAX 10 Devices table.
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