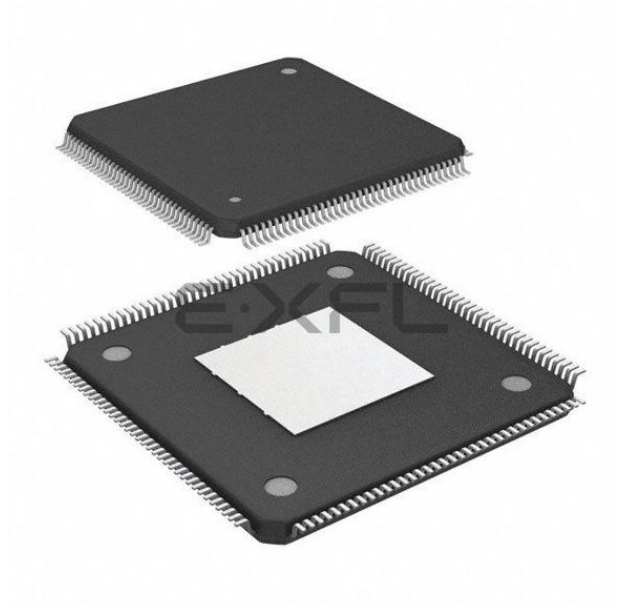

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	500
Number of Logic Elements/Cells	8000
Total RAM Bits	387072
Number of I/O	101
Number of Gates	-
Voltage - Supply	2.85V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	144-EQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10m08sae144i7g

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Symbol	Parameter	Condition	Min	Typ	Max	Unit
		1.35 V	1.2825	1.35	1.4175	V
		1.2 V	1.14	1.2	1.26	V
V_{CCA} (1)	Supply voltage for PLL regulator and ADC block (analog)	—	2.85/3.135	3.0/3.3	3.15/3.465	V

Dual Supply Devices Power Supplies Recommended Operating Conditions

Table 7. Power Supplies Recommended Operating Conditions for Intel MAX 10 Dual Supply Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CC}	Supply voltage for core and periphery	—	1.15	1.2	1.25	V
V_{CCIO} (3)	Supply voltage for input and output buffers	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.35 V	1.2825	1.35	1.4175	V
		1.2 V	1.14	1.2	1.26	V
V_{CCA}(4)	Supply voltage for PLL regulator (analog)	—	2.375	2.5	2.625	V
V_{CCD_PLL}(5)	Supply voltage for PLL regulator (digital)	—	1.15	1.2	1.25	V
V_{CCA_ADC}	Supply voltage for ADC analog block	—	2.375	2.5	2.625	V
V_{CCINT}	Supply voltage for ADC digital block	—	1.15	1.2	1.25	V

(3) V_{CCIO} for all I/O banks must be powered up during user mode because V_{CCIO} I/O banks are used for the ADC and I/O functionalities.

(4) All V_{CCA} pins must be powered to 2.5 V (even when PLLs are not used), and must be powered up and powered down at the same time.

(5) V_{CCD_PLL} must always be connected to V_{CC} through a decoupling capacitor and ferrite bead.

DC Characteristics

Supply Current and Power Consumption

Intel offers two ways to estimate power for your design—the Excel-based Early Power Estimator (EPE) and the Intel Quartus Prime Power Analyzer feature.

Use the Excel-based EPE before you start your design to estimate the supply current for your design. The EPE provides a magnitude estimate of the device power because these currents vary greatly with the usage of the resources.

The Intel Quartus Prime Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yield very accurate power estimates.

Related Information

- Early Power Estimator User Guide
  Provides more information about power estimation tools.
- Power Analysis chapter, Intel Quartus Prime Handbook
  Provides more information about power estimation tools.

I/O Pin Leakage Current

The values in the table are specified for normal device operation. The values vary during device power-up. This applies for all V_{CCIO} settings (3.3, 3.0, 2.5, 1.8, 1.5, 1.35, and 1.2 V).

10 µA I/O leakage current limit is applicable when the internal clamping diode is off. A higher current can be the observed when the diode is on.

Input channel leakage of ADC I/O pins due to hot socket is up to maximum of 1.8 mA. The input channel leakage occurs when the ADC IP core is enabled or disabled. This is applicable to all Intel MAX 10 devices with ADC IP core, which are 10M04, 10M08, 10M16, 10M25, 10M40, and 10M50 devices. The ADC I/O pins are in Bank 1A.

Table 10. I/O Pin Leakage Current for Intel MAX 10 Devices

Symbol	Parameter	Condition	Min	Max	Unit
I_I	Input pin leakage current	V_I = 0 V to $V_{CCIOMAX}$	–10	10	µA
I_{OZ}	Tristated I/O pin leakage current	V_O = 0 V to $V_{CCIOMAX}$	–10	10	µA

Series OCT without Calibration Specifications

Table 13. Series OCT without Calibration Specifications for Intel MAX 10 Devices

This table shows the variation of on-chip termination (OCT) without calibration across process, voltage, and temperature (PVT).

Description	V_{CCIO} (V)	Resistance Tolerance		Unit
		–C7, –I6, –I7, –A6, –A7	–C8	
Series OCT without calibration	3.00	±35	±30	%
	2.50	±35	±30	%
	1.80	±40	±35	%
	1.50	±40	±40	%
	1.35	±40	±50	%
	1.20	±45	±60	%

Series OCT with Calibration at Device Power-Up Specifications

Table 14. Series OCT with Calibration at Device Power-Up Specifications for Intel MAX 10 Devices

OCT calibration is automatically performed at device power-up for OCT enabled I/Os.

Description	V_{CCIO} (V)	Calibration Accuracy	Unit
Series OCT with calibration at device power-up	3.00	±12	%
	2.50	±12	%
	1.80	±12	%
	1.50	±12	%
	1.35	±12	%
	1.20	±12	%

OCT Variation after Calibration at Device Power-Up

The OCT resistance may vary with the variation of temperature and voltage after calibration at device power-up.

Use the following table and equation to determine the final OCT resistance considering the variations after calibration at device power-up.

Table 17. Internal Weak Pull-Up Resistor for Intel MAX 10 Devices

Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$R_{\_PU}$	Value of I/O pin (dedicated and dual-purpose) pull-up resistor before and during configuration, as well as user mode if the programmable pull-up resistor option is enabled	V_{CCIO} = 3.3 V ± 5%	7	12	34	kΩ
		V_{CCIO} = 3.0 V ± 5%	8	13	37	kΩ
		V_{CCIO} = 2.5 V ± 5%	10	15	46	kΩ
		V_{CCIO} = 1.8 V ± 5%	16	25	75	kΩ
		V_{CCIO} = 1.5 V ± 5%	20	36	106	kΩ
		V_{CCIO} = 1.2 V ± 5%	33	82	179	kΩ

Hot-Socketing Specifications

Table 18. Hot-Socketing Specifications for Intel MAX 10 Devices

Symbol	Parameter	Maximum
$I_{IOPIN(DC)}$	DC current per I/O pin	300 µA
$I_{IOPIN(AC)}$	AC current per I/O pin	8 mA (13)

Hysteresis Specifications for Schmitt Trigger Input

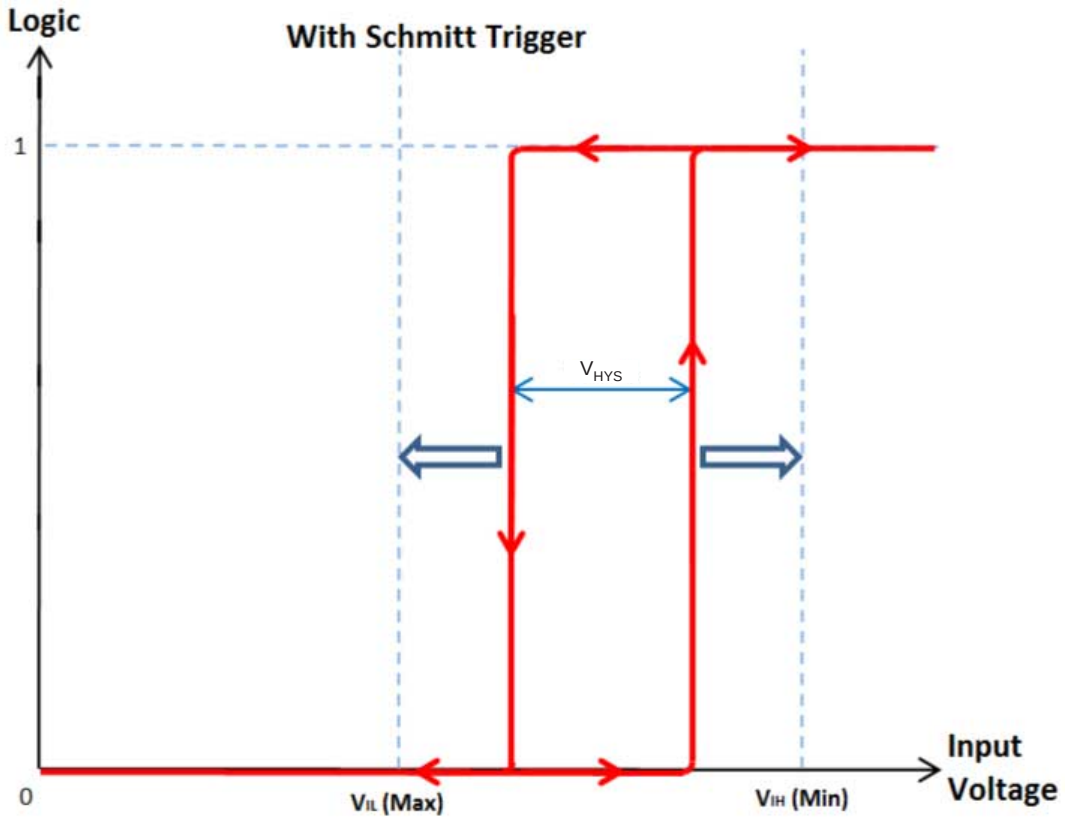
Intel MAX 10 devices support Schmitt trigger input on all I/O pins. A Schmitt trigger feature introduces hysteresis to the input signal for improved noise immunity, especially for signal with slow edge rate.

(13) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}|$ = C dv/dt, in which C is I/O pin capacitance and dv/dt is the slew rate.

Table 19. Hysteresis Specifications for Schmitt Trigger Input for Intel MAX 10 Devices

Symbol	Parameter	Condition	Minimum	Unit
V_{HYS}	Hysteresis for Schmitt trigger input	V_{CCIO} = 3.3 V	180	mV
		V_{CCIO} = 2.5 V	150	mV
		V_{CCIO} = 1.8 V	120	mV
		V_{CCIO} = 1.5 V	110	mV

Figure 4. Schmitt Trigger Input Standard Voltage Diagram



I/O Standards Specifications

Tables in this section list input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Intel MAX 10 devices.

For minimum voltage values, use the minimum V_{CCIO} values. For maximum voltage values, use the maximum V_{CCIO} values.

You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.

Single-Ended I/O Standards Specifications

Table 20. Single-Ended I/O Standards Specifications for Intel MAX 10 Devices

To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the 3.3-V LVTTL specification (4 mA), you should set the current strength settings to 4 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3 V LVTTL	3.135	3.3	3.465	–0.3	0.8	1.7	3.6	0.45	2.4	4	–4
3.3 V LVCMOS	3.135	3.3	3.465	–0.3	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	2	–2
3.0 V LVTTL	2.85	3	3.15	–0.3	0.8	1.7	V_{CCIO} + 0.3	0.45	2.4	4	–4
3.0 V LVCMOS	2.85	3	3.15	–0.3	0.8	1.7	V_{CCIO} + 0.3	0.2	V_{CCIO} – 0.2	0.1	–0.1
2.5 V LVTTL and LVCMOS	2.375	2.5	2.625	–0.3	0.7	1.7	V_{CCIO} + 0.3	0.4	2	1	–1
1.8 V LVTTL and LVCMOS	1.71	1.8	1.89	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	2.25	0.45	V_{CCIO} – 0.45	2	–2
1.5 V LVCMOS	1.425	1.5	1.575	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2
1.2 V LVCMOS	1.14	1.2	1.26	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2
3.3 V Schmitt Trigger	3.135	3.3	3.465	–0.3	0.8	1.7	V_{CCIO} + 0.3	—	—	—	—
2.5 V Schmitt Trigger	2.375	2.5	2.625	–0.3	0.7	1.7	V_{CCIO} + 0.3	—	—	—	—
1.8 V Schmitt Trigger	1.71	1.8	1.89	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	—	—	—	—
1.5 V Schmitt Trigger	1.425	1.5	1.575	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	—	—	—	—
3.0 V PCI	2.85	3	3.15	—	0.3 × V_{CCIO}	0.5 × V_{CCIO}	V_{CCIO} + 0.3	0.1 × V_{CCIO}	0.9 × V_{CCIO}	1.5	–0.5

Core Performance Specifications

Clock Tree Specifications

Table 26. Clock Tree Specifications for Intel MAX 10 Devices

Device	Performance					Unit
	–I6	–A6, –C7	–I7	–A7	–C8	
10M02	450	416	416	382	402	MHz
10M04	450	416	416	382	402	MHz
10M08	450	416	416	382	402	MHz
10M16	450	416	416	382	402	MHz
10M25	450	416	416	382	402	MHz
10M40	450	416	416	382	402	MHz
10M50	450	416	416	382	402	MHz

PLL Specifications

Table 27. PLL Specifications for Intel MAX 10 Devices

V_{CCD_PLL} should always be connected to V_{CCINT} through decoupling capacitor and ferrite bead.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{IN} (28)	Input clock frequency	—	5	—	472.5	MHz
f_{INPFD}	Phase frequency detector (PFD) input frequency	—	5	—	325	MHz

continued...

(28) This parameter is limited in the Intel Quartus Prime software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	—	±50	ps
t_{ARESET}	Minimum pulse width on areset signal.	—	10	—	—	ns
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for PLLs	—	—	3.5 (32)	—	SCANCLK cycles
$f_{SCANCLK}$	scanclk frequency	—	—	—	100	MHz

Table 28. PLL Specifications for Intel MAX 10 Single Supply Devices

For V36 package, the PLL specification is based on single supply devices.

Symbol	Parameter	Condition	Max	Unit
$t_{OUTJITTER\_PERIOD\_DEDCLK}$ (31)	Dedicated clock output period jitter	$F_{OUT} \geq 100$ MHz	660	ps
		$F_{OUT} < 100$ MHz	66	mUI
$t_{OUTJITTER\_CCJ\_DEDCLK}$ (31)	Dedicated clock output cycle-to-cycle jitter	$F_{OUT} \geq 100$ MHz	660	ps
		$F_{OUT} < 100$ MHz	66	mUI

Table 29. PLL Specifications for Intel MAX 10 Dual Supply Devices

Symbol	Parameter	Condition	Max	Unit
$t_{OUTJITTER\_PERIOD\_DEDCLK}$ (31)	Dedicated clock output period jitter	$F_{OUT} \geq 100$ MHz	300	ps
		$F_{OUT} < 100$ MHz	30	mUI
$t_{OUTJITTER\_CCJ\_DEDCLK}$ (31)	Dedicated clock output cycle-to-cycle jitter	$F_{OUT} \geq 100$ MHz	300	ps
		$F_{OUT} < 100$ MHz	30	mUI

(32) With 100 MHz scanclk frequency.

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×4	40	—	300	40	—	300	40	—	300	Mbps
		×2	20	—	300	20	—	300	20	—	300	Mbps
		×1	10	—	300	10	—	300	10	—	300	Mbps
t_{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS[53]	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
$t_{x\ Jitter}$[54]	Output jitter (high-speed I/O performance pin)	—	—	—	425	—	—	425	—	—	425	ps
	Output jitter (low-speed I/O performance pin)	—	—	—	470	—	—	470	—	—	470	ps
t_{RISE}	Rise time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	Fall time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

(53) TCCS specifications apply to I/O banks from the same side only.

(54) TX jitter is the jitter induced from core noise and I/O switching noise.

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×7	70	—	300	70	—	300	70	—	300	Mbps
		×4	40	—	300	40	—	300	40	—	300	Mbps
		×2	20	—	300	20	—	300	20	—	300	Mbps
		×1	10	—	300	10	—	300	10	—	300	Mbps
t_{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS[61]	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
$t_{x\ Jitter}$[62]	Output jitter (high-speed I/O performance pin)	—	—	—	425	—	—	425	—	—	425	ps
	Output jitter (low-speed I/O performance pin)	—	—	—	470	—	—	470	—	—	470	ps
t_{RISE}	Rise time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	Fall time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	Time required for the PLL to lock, after `CONF_DONE` signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

(61) TCCS specifications apply to I/O banks from the same side only.

(62) TX jitter is the jitter induced from core noise and I/O switching noise.

Symbol	Parameter	Mode	–C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×8	80	—	200	80	—	200	80	—	200	Mbps
		×7	70	—	200	70	—	200	70	—	200	Mbps
		×4	40	—	200	40	—	200	40	—	200	Mbps
		×2	20	—	200	20	—	200	20	—	200	Mbps
		×1	10	—	200	10	—	200	10	—	200	Mbps
t_{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS[67]	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
$t_{x\ Jitter}$[68]	Output jitter	—	—	—	1,000	—	—	1,000	—	—	1,000	ps
t_{RISE}	Rise time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	Fall time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

(67) TCCS specifications apply to I/O banks from the same side only.

(68) TX jitter is the jitter induced from core noise and I/O switching noise.

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×7	70	—	300	70	—	300	70	—	300	Mbps
		×4	40	—	300	40	—	300	40	—	300	Mbps
		×2	20	—	300	20	—	300	20	—	300	Mbps
		×1	10	—	300	10	—	300	10	—	300	Mbps
t_{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS[69]	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
$t_{x\ Jitter}$[70]	Output jitter (high-speed I/O performance pin)	—	—	—	425	—	—	425	—	—	425	ps
	Output jitter (low-speed I/O performance pin)	—	—	—	470	—	—	470	—	—	470	ps
t_{RISE}	Rise time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	Fall time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

(69) TCCS specifications apply to I/O banks from the same side only.

(70) TX jitter is the jitter induced from core noise and I/O switching noise.

Remote System Upgrade Circuitry Timing Specifications

Table 50. Remote System Upgrade Circuitry Timing Specifications for Intel MAX 10 Devices

Parameter	Device	Minimum	Maximum	Unit
$t_{MAX\_RU\_CLK}$	All	—	40	MHz
$t_{RU\_nCONFIG}$	10M02, 10M04, 10M08, 10M16, 10M25	250	—	ns
	10M40, 10M50	350	—	ns
$t_{RU\_nRSTIMER}$	10M02, 10M04, 10M08, 10M16, 10M25	300	—	ns
	10M40, 10M50	500	—	ns

User Watchdog Internal Circuitry Timing Specifications

Table 51. User Watchdog Timer Specifications for Intel MAX 10 Devices

The specifications are subject to PVT changes.

Parameter	Device	Minimum	Typical	Maximum	Unit
User watchdog frequency	10M02, 10M04, 10M08, 10M16, 10M25	3.4	5.1	7.3	MHz
	10M40, 10M50	2.2	3.3	4.8	MHz

Uncompressed Raw Binary File (.rbf) Sizes

Table 52. Uncompressed .rbf Sizes for Intel MAX 10 Devices

Device	CFM Data Size (bits)	
	Without Memory Initialization	With Memory Initialization
10M02	554,000	—
10M04	1,540,000	1,880,000
10M08	1,540,000	1,880,000
10M16	2,800,000	3,430,000

continued...

Term	Definition
t_{DUTY}	HIGH-SPEED I/O Block: Duty cycle on high-speed transmitter output clock.
t_{FALL}	Signal high-to-low transition time (80–20%).
t_H	Input register hold time.
Timing Unit Interval (TUI)	HIGH-SPEED I/O block: The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w).
$t_{INJITTER}$	Period jitter on PLL clock input.
$t_{OUTJITTER\_DEDCLK}$	Period jitter on dedicated clock output driven by a PLL.
$t_{OUTJITTER\_IO}$	Period jitter on general purpose I/O driven by a PLL.
t_{plicin}	Delay from PLL inclk pad to I/O input register.
$t_{plicout}$	Delay from PLL inclk pad to I/O output register.
t_{RISE}	Signal low-to-high transition time (20–80%).
t_{SU}	Input register setup time.
$V_{CM(DC)}$	DC common mode input voltage.
$V_{DIF(AC)}$	AC differential input voltage: The minimum AC input differential voltage required for switching.
$V_{DIF(DC)}$	DC differential input voltage: The minimum DC input differential voltage required for switching.
V_{HYS}	Hysteresis for Schmitt trigger input.
V_{ICM}	Input common mode voltage: The common mode of the differential signal at the receiver.
V_{ID}	Input differential Voltage Swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
V_{IH}	Voltage input high: The minimum positive voltage applied to the input which is accepted by the device as a logic high.
$V_{IH(AC)}$	High-level AC input voltage.
$V_{IH(DC)}$	High-level DC input voltage.
V_{IL}	Voltage input low: The maximum positive voltage applied to the input which is accepted by the device as a logic low.
$V_{IL\ (AC)}$	Low-level AC input voltage.
$V_{IL\ (DC)}$	Low-level DC input voltage.
V_{IN}	DC input voltage.

continued...

Term	Definition
V_{OCM}	Output common mode voltage: The common mode of the differential signal at the transmitter.
V_{OD}	Output differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission line at the transmitter. $V_{OD} = V_{OH} – V_{OL}$.
V_{OH}	Voltage output high: The maximum positive voltage from an output which the device considers is accepted as the minimum positive high level.
V_{OL}	Voltage output low: The maximum positive voltage from an output which the device considers is accepted as the maximum positive low level.
V_{OS}	Output offset voltage: $V_{OS} = (V_{OH} + V_{OL}) / 2$.
$V_{OX\ (AC)}$	AC differential Output cross point voltage: The voltage at which the differential output signals must cross.
V_{REF}	Reference voltage for SSTL, HSTL, and HSUL I/O Standards.
$V_{REF(AC)}$	AC input reference voltage for SSTL, HSTL, and HSUL I/O Standards. $V_{REF(AC)} = V_{REF(DC)}$ + noise. The peak-to-peak AC noise on V_{REF} should not exceed 2% of $V_{REF(DC)}$.
$V_{REF(DC)}$	DC input reference voltage for SSTL, HSTL, and HSUL I/O Standards.
$V_{SWING\ (AC)}$	AC differential input voltage: AC Input differential voltage required for switching.
$V_{SWING\ (DC)}$	DC differential input voltage: DC Input differential voltage required for switching.
V_{TT}	Termination voltage for SSTL, HSTL, and HSUL I/O Standards.
$V_{X\ (AC)}$	AC differential Input cross point voltage: The voltage at which the differential input signals must cross.

Document Revision History for the Intel MAX 10 FPGA Device Datasheet

Document Version	Changes
2018.06.29	• Removed links on instant-on feature. • Added JTAG timing specifications term in *Glossary*. • Renamed the following IP cores as per Intel rebranding: — Renamed Altera Modular ADC IP core to Modular ADC core Intel FPGA IP core. — Renamed Altera Modular Dual ADC IP core to Modular Dual ADC core Intel FPGA IP core.

Date	Version	Changes
January 2016	2016.01.22	• Added description about automotive temperature devices in the Programming/Erasure Specifications table. • Changed the pin capacitance to maximum values. • Updated maximum TCCS specifications from 410 ps to 300 ps in the following tables: — True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — Emulated RSDS_E_1R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True LVDS Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices — True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — Emulated LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices — Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices • Added new table: True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices. • Updated maximum f_{HSCLK} and HSIODR specifications for –A6, –C7, and –I7 speed grades in True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices table. • Updated SW specifications in the following tables: — LVDS Receiver Timing Specifications for Intel MAX 10 Single Supply Devices — LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices • Updated maximum f_{HSCLK} and HSIODR (high-speed I/O performance pin) specifications for –I6, –A6, –C7, –I7 speed grades in LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices table. • Removed Internal Configuration Time information in the Uncompressed .rbf Sizes for Intel MAX 10 Devices table. • Added Internal Configuration Time tables for uncompressed `.rbf` files and compressed `.rbf` files. • Removed Preliminary tags for all tables.
November 2015	2015.11.02	• Added description to *Maximum Allowed Overshoot During Transitions over a 11.4-Year Time Frame* topic. • Added ADC_VREF Pin Leakage Current for Intel MAX 10 Devices table. • Updated the condition for "Bus-hold high, sustaining current" parameter from "$V_{IN} < V_{IL}$ (minimum)" to "$V_{IN} < V_{IH}$ (minimum)" in Bus Hold Parameters table.

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Date	Version	Changes
May 2015	2015.05.04	• Updated a note to V_{CCIO} for both single supply and dual supply power supplies recommended operating conditions tables. Note updated: V_{CCIO} for all I/O banks must be powered up during user mode because V_{CCIO} I/O banks are used for the ADC and I/O functionalities. • Updated Example for OCT Resistance Calculation after Calibration at Device Power-Up. • Removed a note to BLVDS in Differential I/O Standards Specifications for Intel MAX 10 Devices table. BLVDS is now supported in Intel MAX 10 single supply devices. Note removed: BLVDS TX is not supported in single supply devices. • Updated ADC Performance Specifications for both single supply and dual supply devices. — Changed the symbol for Operating junction temperature range parameter from T_A to T_J. — Edited sampling rate maximum value from 1000 kSPS to 1 MSPS. — Added a note to analog input voltage parameter. — Removed input frequency, f_{IN} specification. — Updated the condition for DNL specification: External V_{REF}, no missing code. Added DNL specification for condition: Internal V_{REF}, no missing code. — Added notes to AC accuracy specifications that the value with prescalar enabled is 6dB less than the specification. — Added a note to On-Chip Temperature Sensor (absolute accuracy) parameter about the averaging calculation. • Updated ADC Performance Specifications for Intel MAX 10 Single Supply Devices table. — Added condition for On-Chip Temperature Sensor (absolute accuracy) parameter: with 64 samples averaging. • Updated ADC Performance Specifications for Intel MAX 10 Dual Supply Devices table. — Updated Digital Supply Voltage minimum value from 1.14 V to 1.15 V and maximum value from 1.26 V to 1.25 V. • Updated f_{HSCLK} and HSIODR specifications for –A7 speed grade in the following tables: — True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True LVDS Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices — True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — Emulated LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices — Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — LVDS Receiver Timing Specifications for Intel MAX 10 Single Supply Devices — LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices

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Date	Version	Changes
		• Updated SSTL-2 Class I and II I/O standard specifications for JEDEC compliance as follows: — VIL(AC) Max: Updated from V_{REF} – 0.35 to V_{REF} – 0.31 — VIH(AC) Min: Updated from V_{REF} + 0.35 to V_{REF} + 0.31 • Added a note to BLVDS in Differential I/O Standards Specifications for Intel MAX 10 Devices table: BLVDS TX is not supported in single supply devices. • Added a link to MAX 10 High-Speed LVDS I/O User Guide for the list of I/O standards supported in single supply and dual supply devices. • Added a statement in PLL Specifications for Intel MAX 10 Single Supply Device table: For V36 package, the PLL specification is based on single supply devices. • Added Internal Oscillator Specifications from Intel MAX 10 Clocking and PLL User Guide. • Added UFM specifications for serial interface. • Updated total harmonic distortion (THD) specifications as follows: — Single supply devices: Updated from 65 dB to –65 dB — Dual supply devices: Updated from 70 dB to –70 dB (updated from 65 dB to –65 dB for dual function pin) • Added condition for On-Chip Temperature Sensor—Absolute accuracy parameter in ADC Performance Specifications for Intel MAX 10 Dual Supply Devices table. The condition is: with 64 samples averaging. • Updated the description in Periphery Performance Specifications to mention that proper timing closure is required in design. • Updated HSIODR and f_{HSCLK} specifications for x10 and x7 modes in True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices. • Added specifications for low-speed I/O performance pin sampling window in LVDS Receiver Timing Specifications for Intel MAX 10 Single Supply Devices table: Max = 900 ps for –C7, –I7, –A7, and –C8 speed grades. • Added $t_{RU\_nCONFIG}$ and $t_{RU\_nRSTIMER}$ specifications for different devices in Remote System Upgrade Circuitry Timing Specifications for Intel MAX 10 Devices table. • Removed the word "internal oscillator" in User Watchdog Timer Specifications for Intel MAX 10 Devices table to avoid confusion. • Added IOE programmable delay specifications.
September 2014	2014.09.22	Initial release.