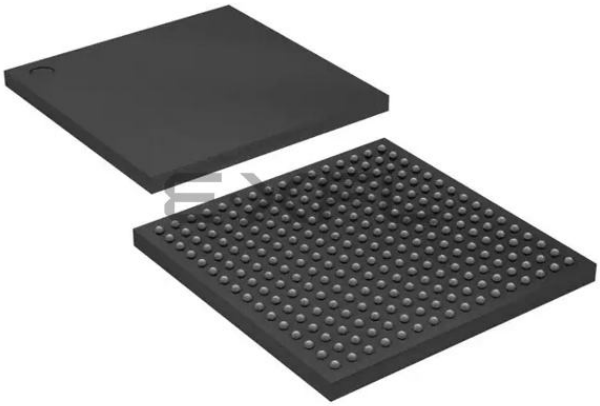


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1000
Number of Logic Elements/Cells	16000
Total RAM Bits	562176
Number of I/O	178
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10m16dcf256c8g

Contents

Condition (V)	Overshoot Duration as % of High Time	Unit
4.32	2.6	%
4.37	1.6	%
4.42	1.0	%
4.47	0.6	%
4.52	0.3	%
4.57	0.2	%

Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Intel MAX 10 devices. The tables list the steady-state voltage values expected from Intel MAX 10 devices. Power supply ramps must all be strictly monotonic, without plateaus.

Single Supply Devices Power Supplies Recommended Operating Conditions

Table 6. Power Supplies Recommended Operating Conditions for Intel MAX 10 Single Supply Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CC_ONE}(1)	Supply voltage for core and periphery through on-die voltage regulator	—	2.85/3.135	3.0/3.3	3.15/3.465	V
V_{CCIO}(2)	Supply voltage for input and output buffers	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V

continued...

(1) V_{CCA} must be connected to V_{CC_ONE} through a filter.

(2) V_{CCIO} for all I/O banks must be powered up during user mode because V_{CCIO} I/O banks are used for the ADC and I/O functionalities.

Table 11. ADC_VREF Pin Leakage Current for Intel MAX 10 Devices

Symbol	Parameter	Condition	Min	Max	Unit
I_{adc_vref}	ADC_VREF pin leakage current	Single supply mode	—	10	µA
		Dual supply mode	—	20	µA

Bus Hold Parameters

Bus hold retains the last valid logic state after the source driving it either enters the high impedance state or is removed. Each I/O pin has an option to enable bus hold in user mode. Bus hold is always disabled in configuration mode.

Table 12. Bus Hold Parameters for Intel MAX 10 Devices

Parameter	Condition	V_{CCIO} (V)												Unit
		1.2		1.5		1.8		2.5		3.0		3.3		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold low, sustaining current	$V_{IN} > V_{IL}$ (maximum)	8	—	12	—	30	—	50	—	70	—	70	—	µA
Bus-hold high, sustaining current	$V_{IN} < V_{IH}$ (minimum)	–8	—	–12	—	–30	—	–50	—	–70	—	–70	—	µA
Bus-hold low, overdrive current	$0 V < V_{IN} < V_{CCIO}$	—	125	—	175	—	200	—	300	—	500	—	500	µA
Bus-hold high, overdrive current	$0 V < V_{IN} < V_{CCIO}$	—	–125	—	–175	—	–200	—	–300	—	–500	—	–500	µA
Bus-hold trip point	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

Table 21. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Intel MAX 10 Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V) (14)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	1.19	1.25	1.31	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.7	1.8	1.9	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-135 Class I, II	1.283	1.35	1.45	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	0.85	0.9	0.95
HSTL-15 Class I, II	1.425	1.5	1.575	0.71	0.75	0.79	0.71	0.75	0.79
HSTL-12 Class I, II	1.14	1.2	1.26	0.48 × V_{CCIO} (15)	0.5 × V_{CCIO} (15)	0.52 × V_{CCIO} (15)	—	0.5 × V_{CCIO}	—
				0.47 × V_{CCIO} (16)	0.5 × V_{CCIO} (16)	0.53 × V_{CCIO} (16)			
HSUL-12	1.14	1.2	1.3	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	—	—	—

(14) V_{TT} of transmitting device must track V_{REF} of the receiving device.

(15) Value shown refers to DC input reference voltage, $V_{REF(DC)}$.

(16) Value shown refers to AC input reference voltage, $V_{REF(AC)}$.

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)		$V_{IH(AC)}$ (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Max	Min	Max	Min	Max	Min	Max	Max	Min		
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	–0.24	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.24	0.25 × V_{CCIO}	0.75 × V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	–0.24	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.24	0.25 × V_{CCIO}	0.75 × V_{CCIO}	14	–14
HSUL-12	—	V_{REF} – 0.13	V_{REF} + 0.13	—	—	V_{REF} – 0.22	V_{REF} + 0.22	—	0.1 × V_{CCIO}	0.9 × V_{CCIO}	—	—

Differential SSTL I/O Standards Specifications

Differential SSTL requires a V_{REF} input.

Table 23. Differential SSTL I/O Standards Specifications for Intel MAX 10 Devices

I/O Standard	V_{CCIO} (V)			$V_{Swing(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{Swing(AC)}$ (V)	
	Min	Typ	Max	Min	Max[17]	Min	Typ	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.36	V_{CCIO}	$V_{CCIO}/2$ – 0.2	—	V_{CCIO}/ 2+ 0.2	0.7	V_{CCIO}
SSTL-18 Class I, II	1.7	1.8	1.9	0.25	V_{CCIO}	$V_{CCIO}/2$ – 0.175	—	V_{CCIO}/ 2+ 0.175	0.5	V_{CCIO}
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	$V_{CCIO}/2$ – 0.15	—	$V_{CCIO}/2$ + 0.15	$2(V_{IH(AC)} – V_{REF})$	$2(V_{IL(AC)} – V_{REF})$
SSTL-135	1.283	1.35	1.45	0.18	—	V_{REF} – 0.135	0.5 × V_{CCIO}	V_{REF} + 0.135	$2(V_{IH(AC)} – V_{REF})$	$2(V_{IL(AC)} – V_{REF})$

Differential HSTL and HSUL I/O Standards Specifications

Differential HSTL requires a V_{REF} input.

(17) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)		V_{ICM} (V) (18)			V_{OD} (mV) (19)(20)			V_{OS} (V) (19)		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
HiSpi	2.375	2.5	2.625	100	—	0.05	D_{MAX} ≤ 500 Mbps	1.8	—	—	—	—	—	—
						0.55	500 Mbps ≤ D_{MAX} ≤ 700 Mbps	1.8						
						1.05	D_{MAX} > 700 Mbps	1.55						

Related Information

Intel MAX 10 LVDS SERDES I/O Standards Support, Intel MAX 10 High-Speed LVDS I/O User Guide
Provides the list of I/O standards supported in single supply and dual supply devices.

Switching Characteristics

This section provides the performance characteristics of Intel MAX 10 core and periphery blocks.

(18) V_{IN} range: 0 V ≤ V_{IN} ≤ 1.85 V.
(19) R_L range: 90 ≤ R_L ≤ 110 Ω.
(20) Low V_{OD} setting is only supported for RSDS standard.

(22) No fixed V_{IN} , V_{OD} , and V_{OS} specifications for Bus LVDS (BLVDS). They are dependent on the system topology.

(23) Mini-LVDS, RSDS, and Point-to-Point Differential Signaling (PPDS) standards are only supported at the output pins for Intel MAX 10 devices.

(24) Supported with requirement of an external level shift

(25) Sub-LVDS input buffer is using 2.5 V differential buffer.

(26) Differential output depends on the values of the external termination resistors.

(27) Differential output offset voltage depends on the values of the external termination resistors.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{VCO} (29)	PLL internal voltage-controlled oscillator (VCO) operating range	—	600	—	1300	MHz
f_{INDUTY}	Input clock duty cycle	—	40	—	60	%
$t_{INJITTER\_CCJ}$ (30)	Input clock cycle-to-cycle jitter	F_{INPFD} ≥ 100 MHz	—	—	0.15	UI
		F_{INPFD} < 100 MHz	—	—	±750	ps
f_{OUT_EXT} (28)	PLL output frequency for external clock output	—	—	—	472.5	MHz
f_{OUT}	PLL output frequency to global clock	–6 speed grade	—	—	472.5	MHz
		–7 speed grade	—	—	450	MHz
		–8 speed grade	—	—	402.5	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output	Duty cycle set to 50%	45	50	55	%
t_{LOCK}	Time required to lock from end of device configuration	—	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically	After switchover, reconfiguring any non-post-scale counters or delays, or when `areset` is deasserted	—	—	1	ms
$t_{OUTJITTER\_PERIOD\_IO}$ (31)	Regular I/O period jitter	F_{OUT} ≥ 100 MHz	—	—	650	ps
		F_{OUT} < 100 MHz	—	—	75	mUI
$t_{OUTJITTER\_CCJ\_IO}$ (31)	Regular I/O cycle-to-cycle jitter	F_{OUT} ≥ 100 MHz	—	—	650	ps
		F_{OUT} < 100 MHz	—	—	75	mUI

continued...

(29) The VCO frequency reported by the Intel Quartus Prime software in the PLL summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

(30) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source, which is less than 200 ps.

(31) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied.

True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications

Table 36. True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

True **PPDS** transmitter is only supported at bottom I/O banks. Emulated **PPDS** transmitter is supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	—	155	5	—	155	5	—	155	MHz
		×8	5	—	155	5	—	155	5	—	155	MHz
		×7	5	—	155	5	—	155	5	—	155	MHz
		×4	5	—	155	5	—	155	5	—	155	MHz
		×2	5	—	155	5	—	155	5	—	155	MHz
		×1	5	—	310	5	—	310	5	—	310	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	—	310	100	—	310	100	—	310	Mbps
		×8	80	—	310	80	—	310	80	—	310	Mbps
		×7	70	—	310	70	—	310	70	—	310	Mbps
		×4	40	—	310	40	—	310	40	—	310	Mbps
		×2	20	—	310	20	—	310	20	—	310	Mbps
		×1	10	—	310	10	—	310	10	—	310	Mbps
f_{HSCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	—	150	5	—	150	5	—	150	MHz
		×8	5	—	150	5	—	150	5	—	150	MHz
		×7	5	—	150	5	—	150	5	—	150	MHz
		×4	5	—	150	5	—	150	5	—	150	MHz
		×2	5	—	150	5	—	150	5	—	150	MHz
		×1	5	—	300	5	—	300	5	—	300	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	—	300	100	—	300	100	—	300	Mbps
		×8	80	—	300	80	—	300	80	—	300	Mbps
		×7	70	—	300	70	—	300	70	—	300	Mbps

continued...

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×4	40	—	300	40	—	300	40	—	300	Mbps
		×2	20	—	300	20	—	300	20	—	300	Mbps
		×1	10	—	300	10	—	300	10	—	300	Mbps
t_{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS[53]	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
$t_{x\ Jitter}$[54]	Output jitter (high-speed I/O performance pin)	—	—	—	425	—	—	425	—	—	425	ps
	Output jitter (low-speed I/O performance pin)	—	—	—	470	—	—	470	—	—	470	ps
t_{RISE}	Rise time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	Fall time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

(53) TCCS specifications apply to I/O banks from the same side only.

(54) TX jitter is the jitter induced from core noise and I/O switching noise.

True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications

Single Supply Devices True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications

Table 37. True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices

True **RSDS** transmitter is only supported at bottom I/O banks. Emulated **RSDS** transmitter is supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	—	50	5	—	50	5	—	50	MHz
		×8	5	—	50	5	—	50	5	—	50	MHz
		×7	5	—	50	5	—	50	5	—	50	MHz
		×4	5	—	50	5	—	50	5	—	50	MHz
		×2	5	—	50	5	—	50	5	—	50	MHz
		×1	5	—	100	5	—	100	5	—	100	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	—	100	100	—	100	100	—	100	Mbps
		×8	80	—	100	80	—	100	80	—	100	Mbps
		×7	70	—	100	70	—	100	70	—	100	Mbps
		×4	40	—	100	40	—	100	40	—	100	Mbps
		×2	20	—	100	20	—	100	20	—	100	Mbps
		×1	10	—	100	10	—	100	10	—	100	Mbps
f_{HSCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	—	50	5	—	50	5	—	50	MHz
		×8	5	—	50	5	—	50	5	—	50	MHz
		×7	5	—	50	5	—	50	5	—	50	MHz
		×4	5	—	50	5	—	50	5	—	50	MHz
		×2	5	—	50	5	—	50	5	—	50	MHz
		×1	5	—	100	5	—	100	5	—	100	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	—	100	100	—	100	100	—	100	Mbps

continued...

Dual Supply Devices True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications

Table 38. True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

True **RSDS** transmitter is only supported at bottom I/O banks. Emulated **RSDS** transmitter is supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	—	155	5	—	155	5	—	155	MHz
		×8	5	—	155	5	—	155	5	—	155	MHz
		×7	5	—	155	5	—	155	5	—	155	MHz
		×4	5	—	155	5	—	155	5	—	155	MHz
		×2	5	—	155	5	—	155	5	—	155	MHz
		×1	5	—	310	5	—	310	5	—	310	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	—	310	100	—	310	100	—	310	Mbps
		×8	80	—	310	80	—	310	80	—	310	Mbps
		×7	70	—	310	70	—	310	70	—	310	Mbps
		×4	40	—	310	40	—	310	40	—	310	Mbps
		×2	20	—	310	20	—	310	20	—	310	Mbps
		×1	10	—	310	10	—	310	10	—	310	Mbps
f_{HSCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	—	150	5	—	150	5	—	150	MHz
		×8	5	—	150	5	—	150	5	—	150	MHz
		×7	5	—	150	5	—	150	5	—	150	MHz
		×4	5	—	150	5	—	150	5	—	150	MHz
		×2	5	—	150	5	—	150	5	—	150	MHz
		×1	5	—	300	5	—	300	5	—	300	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	—	300	100	—	300	100	—	300	Mbps
		×8	80	—	300	80	—	300	80	—	300	Mbps
		×7	70	—	300	70	—	300	70	—	300	Mbps

continued...

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×4	40	—	300	40	—	300	40	—	300	Mbps
		×2	20	—	300	20	—	300	20	—	300	Mbps
		×1	10	—	300	10	—	300	10	—	300	Mbps
t_{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS[57]	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
$t_{x\ Jitter}$[58]	Output jitter (high-speed I/O performance pin)	—	—	—	425	—	—	425	—	—	425	ps
	Output jitter (low-speed I/O performance pin)	—	—	—	470	—	—	470	—	—	470	ps
t_{RISE}	Rise time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	Fall time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

(57) TCCS specifications apply to I/O banks from the same side only.

(58) TX jitter is the jitter induced from core noise and I/O switching noise.

True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications

Table 40. True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

True **mini-LVDS** transmitter is only supported at the bottom I/O banks. Emulated **mini-LVDS_E_3R** transmitter is supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	—	155	5	—	155	5	—	155	MHz
		×8	5	—	155	5	—	155	5	—	155	MHz
		×7	5	—	155	5	—	155	5	—	155	MHz
		×4	5	—	155	5	—	155	5	—	155	MHz
		×2	5	—	155	5	—	155	5	—	155	MHz
		×1	5	—	310	5	—	310	5	—	310	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	—	310	100	—	310	100	—	310	Mbps
		×8	80	—	310	80	—	310	80	—	310	Mbps
		×7	70	—	310	70	—	310	70	—	310	Mbps
		×4	40	—	310	40	—	310	40	—	310	Mbps
		×2	20	—	310	20	—	310	20	—	310	Mbps
		×1	10	—	310	10	—	310	10	—	310	Mbps
f_{HSCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	—	150	5	—	150	5	—	150	MHz
		×8	5	—	150	5	—	150	5	—	150	MHz
		×7	5	—	150	5	—	150	5	—	150	MHz
		×4	5	—	150	5	—	150	5	—	150	MHz
		×2	5	—	150	5	—	150	5	—	150	MHz
		×1	5	—	300	5	—	300	5	—	300	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	—	300	100	—	300	100	—	300	Mbps
		×8	80	—	300	80	—	300	80	—	300	Mbps

continued...

True LVDS Transmitter Timing

Single Supply Devices True LVDS Transmitter Timing Specifications

Table 41. True LVDS Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices

True **LVDS** transmitter is only supported at the bottom I/O banks.

Symbol	Parameter	Mode	–C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	Input clock frequency	×10	5	—	145	5	—	100	5	—	100	MHz
		×8	5	—	145	5	—	100	5	—	100	MHz
		×7	5	—	145	5	—	100	5	—	100	MHz
		×4	5	—	145	5	—	100	5	—	100	MHz
		×2	5	—	145	5	—	100	5	—	100	MHz
		×1	5	—	290	5	—	200	5	—	200	MHz
HSIODR	Data rate	×10	100	—	290	100	—	200	100	—	200	Mbps
		×8	80	—	290	80	—	200	80	—	200	Mbps
		×7	70	—	290	70	—	200	70	—	200	Mbps
		×4	40	—	290	40	—	200	40	—	200	Mbps
		×2	20	—	290	20	—	200	20	—	200	Mbps
		×1	10	—	290	10	—	200	10	—	200	Mbps
t_{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS(63)	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
$t_{x\ Jitter}$(64)	Output jitter	—	—	—	1,000	—	—	1,000	—	—	1,000	ps

continued...

(63) TCCS specifications apply to I/O banks from the same side only.

(64) TX jitter is the jitter induced from core noise and I/O switching noise.

Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications

Single Supply Devices Emulated LVDS_E_3R Transmitter Timing Specifications

Table 43. Emulated LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices

Emulated **LVDS_E_3R** transmitters are supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	–C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	—	142.5	5	—	100	5	—	100	MHz
		×8	5	—	142.5	5	—	100	5	—	100	MHz
		×7	5	—	142.5	5	—	100	5	—	100	MHz
		×4	5	—	142.5	5	—	100	5	—	100	MHz
		×2	5	—	142.5	5	—	100	5	—	100	MHz
		×1	5	—	285	5	—	200	5	—	200	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	—	285	100	—	200	100	—	200	Mbps
		×8	80	—	285	80	—	200	80	—	200	Mbps
		×7	70	—	285	70	—	200	70	—	200	Mbps
		×4	40	—	285	40	—	200	40	—	200	Mbps
		×2	20	—	285	20	—	200	20	—	200	Mbps
		×1	10	—	285	10	—	200	10	—	200	Mbps
f_{HSCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	—	100	5	—	100	5	—	100	MHz
		×8	5	—	100	5	—	100	5	—	100	MHz
		×7	5	—	100	5	—	100	5	—	100	MHz
		×4	5	—	100	5	—	100	5	—	100	MHz
		×2	5	—	100	5	—	100	5	—	100	MHz
		×1	5	—	200	5	—	200	5	—	200	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	—	200	100	—	200	100	—	200	Mbps

continued...

Table 56. I/O Timing for Intel MAX 10 Devices

These I/O timing parameters are for the 3.3-V LVTTL I/O standard with the maximum drive strength and fast slew rate for 10M08DAF484 device.

Symbol	Parameter	–C7, –I7	–C8	Unit
T_{su}	Global clock setup time	–0.750	–0.808	ns
T_h	Global clock hold time	1.180	1.215	ns
T_{co}	Global clock to output delay	5.131	5.575	ns
T_{pd}	Best case pin-to-pin propagation delay through one LUT	4.907	5.467	ns

Programmable IOE Delay

Programmable IOE Delay On Row Pins

Table 57. IOE Programmable Delay on Row Pins for Intel MAX 10 Devices

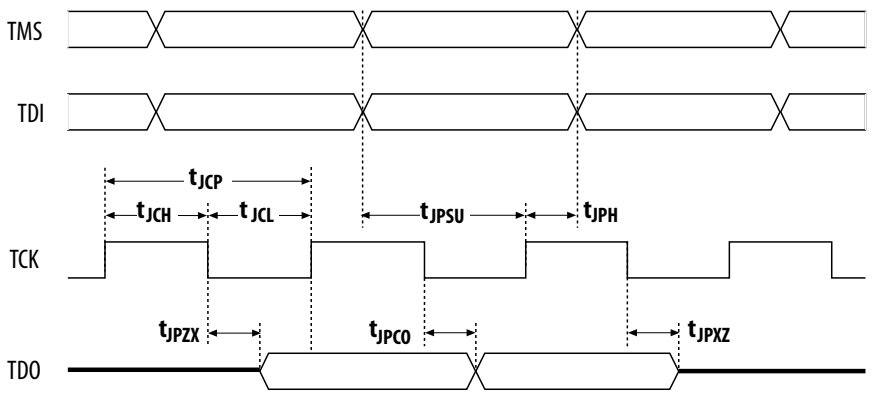
The incremental values for the settings are generally linear. For exact values of each setting, refer to the **Assignment Name** column in the latest version of the Intel Quartus Prime software.

The minimum and maximum offset timing numbers are in reference to setting '0' as available in the Intel Quartus Prime software.

Parameter	Paths Affected	Number of Settings	Minimum Offset	Maximum Offset							Unit
				Fast Corner		Slow Corner					
				–I7	–C8	–A6	–C7	–C8	–I7	–A7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	0.815	0.873	1.831	1.811	1.874	1.871	1.922	ns
Input delay from pin to input register	Pad to I/O input register	8	0	0.924	0.992	2.081	2.055	2.125	2.127	2.185	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.479	0.514	1.069	1.070	1.117	1.105	1.134	ns

Glossary

Table 59. Glossary

Term	Definition
JTAG Timing Specifications	
R_L	Receiver differential input discrete resistor (external to Intel MAX 10 devices).
RSKM (Receiver input skew margin)	HIGH-SPEED I/O block: The total margin left after accounting for the sampling window and TCCS. RSKM = (TUI – SW – TCCS) / 2.
Sampling window (SW)	HIGH-SPEED I/O Block: The period of time during which the data must be valid to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window.
Single-ended voltage referenced I/O standard	The AC input signal values indicate the voltage levels at which the receiver must meet its timing specifications. The DC input signal values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input crosses the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing.
t_C	High-speed receiver/transmitter input and output clock period.
TCCS (Channel-to- channel-skew)	HIGH-SPEED I/O block: The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
t_{cin}	Delay from clock pad to I/O input register.
t_{CO}	Delay from clock pad to I/O output.
t_{cout}	Delay from clock pad to I/O output register.

continued...

Date	Version	Changes
December 2017	2017.12.15	• Removed the units for "Input resistance" and "Input capacitance" parameters in the following tables: — *ADC Performance Specifications for Intel MAX 10 Single Supply Devices* — *ADC Performance Specifications for Intel MAX 10 Dual Supply Devices* • Removed the specification with memory initialization for 10M02 device in the *Uncompressed .rbf Sizes for Intel MAX 10 Devices* table.
June 2017	2017.06.16	• Added notes for T_J for Industrial and Automotive devices in Recommended Operating Conditions for Intel MAX 10 Devices table. • Updated the parameter in Internal Weak Pull-Up Resistor for Intel MAX 10 Devices table. • Changed "Performance" to "Frequency" in UFM Performance Specifications for Intel MAX 10 Devices table. • Removed PowerPlay text from tool name.
February 2017	2017.02.21	• Rebranded as Intel.
October 2016	2016.10.31	• Updated the note to the Intel MAX 10 Device Grades and Speed Grades Supported table. • Updated the Memory Standards Supported by the Soft Memory Controller for Intel MAX 10 Devices table.
May 2016	2016.05.02	• Updated t_{RAMP} specifications in Recommended Operating Conditions for Intel MAX 10 Devices table. — Removed standard POR and fast POR specifications. — Updated maximum value from 3 ms to 10 ms and added a not for the minimum value. • Added Supply Current and Power Consumption section. • Added the following tables: — Memory Standards Supported by the Soft Memory Controller for Intel MAX 10 Devices — Internal Configuration Timing Parameter for Intel MAX 10 Devices • Removed POR Delay Specifications for Intel MAX 10 Devices table. • Updated the description in the Internal Configuration Time section. • Updated the following tables: — Internal Configuration Time for Intel MAX 10 Devices (Uncompressed `.rbf`) — Internal Configuration Time for Intel MAX 10 Devices (Compressed `.rbf`)

continued...

Date	Version	Changes
January 2016	2016.01.22	• Added description about automotive temperature devices in the Programming/Erasure Specifications table. • Changed the pin capacitance to maximum values. • Updated maximum TCCS specifications from 410 ps to 300 ps in the following tables: — True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — Emulated RSDS_E_1R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True LVDS Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices — True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — Emulated LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices — Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices • Added new table: True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices. • Updated maximum f_{HSCLK} and HSIODR specifications for –A6, –C7, and –I7 speed grades in True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices table. • Updated SW specifications in the following tables: — LVDS Receiver Timing Specifications for Intel MAX 10 Single Supply Devices — LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices • Updated maximum f_{HSCLK} and HSIODR (high-speed I/O performance pin) specifications for –I6, –A6, –C7, –I7 speed grades in LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices table. • Removed Internal Configuration Time information in the Uncompressed .rbf Sizes for Intel MAX 10 Devices table. • Added Internal Configuration Time tables for uncompressed `.rbf` files and compressed `.rbf` files. • Removed Preliminary tags for all tables.
November 2015	2015.11.02	• Added description to *Maximum Allowed Overshoot During Transitions over a 11.4-Year Time Frame* topic. • Added ADC_VREF Pin Leakage Current for Intel MAX 10 Devices table. • Updated the condition for "Bus-hold high, sustaining current" parameter from "$V_{IN} < V_{IL}$ (minimum)" to "$V_{IN} < V_{IH}$ (minimum)" in Bus Hold Parameters table.

continued...

Date	Version	Changes
May 2015	2015.05.04	• Updated a note to V_{CCIO} for both single supply and dual supply power supplies recommended operating conditions tables. Note updated: V_{CCIO} for all I/O banks must be powered up during user mode because V_{CCIO} I/O banks are used for the ADC and I/O functionalities. • Updated Example for OCT Resistance Calculation after Calibration at Device Power-Up. • Removed a note to BLVDS in Differential I/O Standards Specifications for Intel MAX 10 Devices table. BLVDS is now supported in Intel MAX 10 single supply devices. Note removed: BLVDS TX is not supported in single supply devices. • Updated ADC Performance Specifications for both single supply and dual supply devices. — Changed the symbol for Operating junction temperature range parameter from T_A to T_J. — Edited sampling rate maximum value from 1000 kSPS to 1 MSPS. — Added a note to analog input voltage parameter. — Removed input frequency, f_{IN} specification. — Updated the condition for DNL specification: External V_{REF}, no missing code. Added DNL specification for condition: Internal V_{REF}, no missing code. — Added notes to AC accuracy specifications that the value with prescalar enabled is 6dB less than the specification. — Added a note to On-Chip Temperature Sensor (absolute accuracy) parameter about the averaging calculation. • Updated ADC Performance Specifications for Intel MAX 10 Single Supply Devices table. — Added condition for On-Chip Temperature Sensor (absolute accuracy) parameter: with 64 samples averaging. • Updated ADC Performance Specifications for Intel MAX 10 Dual Supply Devices table. — Updated Digital Supply Voltage minimum value from 1.14 V to 1.15 V and maximum value from 1.26 V to 1.25 V. • Updated f_{HSCLK} and HSIODR specifications for –A7 speed grade in the following tables: — True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True LVDS Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices — True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — Emulated LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices — Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — LVDS Receiver Timing Specifications for Intel MAX 10 Single Supply Devices — LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices

continued...