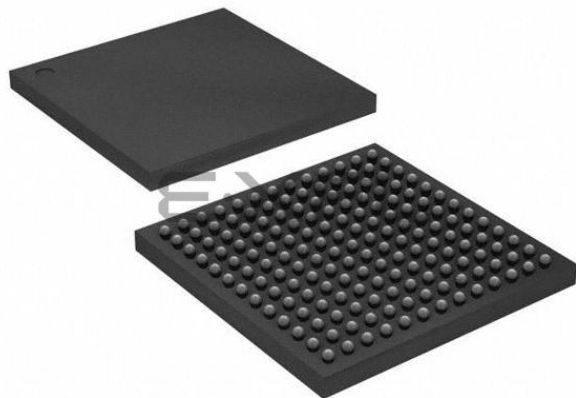




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

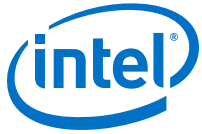
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	1000
Number of Logic Elements/Cells	16000
Total RAM Bits	562176
Number of I/O	130
Number of Gates	-
Voltage - Supply	2.85V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	169-LFBGA
Supplier Device Package	169-UBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10m16sau169c8g



Operating Conditions

Intel MAX 10 devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Intel MAX 10 devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions for Intel MAX 10 devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Caution: Conditions outside the range listed in the absolute maximum ratings tables may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Single Supply Devices Absolute Maximum Ratings

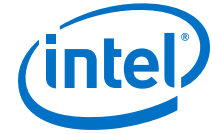
Table 2. Absolute Maximum Ratings for Intel MAX 10 Single Supply Devices

Symbol	Parameter	Min	Max	Unit
V _{CC_ONE}	Supply voltage for core and periphery through on-die voltage regulator	-0.5	3.9	V
V _{CCIO}	Supply voltage for input and output buffers	-0.5	3.9	V
V _{CCA}	Supply voltage for phase-locked loop (PLL) regulator and analog-to-digital converter (ADC) block (analog)	-0.5	3.9	V

Dual Supply Devices Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings for Intel MAX 10 Dual Supply Devices

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply voltage for core and periphery	-0.5	1.63	V
V _{CCIO}	Supply voltage for input and output buffers	-0.5	3.9	V
V _{CCA}	Supply voltage for PLL regulator (analog)	-0.5	3.41	V
continued...				



Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{CCA}^{(1)}$	Supply voltage for PLL regulator and ADC block (analog)	1.35 V	1.2825	1.35	1.4175	V
		1.2 V	1.14	1.2	1.26	V
		—	2.85/3.135	3.0/3.3	3.15/3.465	V

Dual Supply Devices Power Supplies Recommended Operating Conditions

Table 7. Power Supplies Recommended Operating Conditions for Intel MAX 10 Dual Supply Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CC}	Supply voltage for core and periphery	—	1.15	1.2	1.25	V
$V_{CCIO}^{(3)}$	Supply voltage for input and output buffers	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.35 V	1.2825	1.35	1.4175	V
		1.2 V	1.14	1.2	1.26	V
$V_{CCA}^{(4)}$	Supply voltage for PLL regulator (analog)	—	2.375	2.5	2.625	V
$V_{CCD_PLL}^{(5)}$	Supply voltage for PLL regulator (digital)	—	1.15	1.2	1.25	V
V_{CCA_ADC}	Supply voltage for ADC analog block	—	2.375	2.5	2.625	V
V_{CCINT}	Supply voltage for ADC digital block	—	1.15	1.2	1.25	V

⁽³⁾ V_{CCIO} for all I/O banks must be powered up during user mode because V_{CCIO} I/O banks are used for the ADC and I/O functionalities.

⁽⁴⁾ All V_{CCA} pins must be powered to 2.5 V (even when PLLs are not used), and must be powered up and powered down at the same time.

⁽⁵⁾ V_{CCD_PLL} must always be connected to V_{CC} through a decoupling capacitor and ferrite bead.

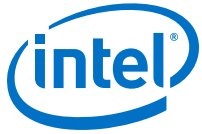


Table 15. OCT Variation after Calibration at Device Power-Up for Intel MAX 10 Devices

This table lists the change percentage of the OCT resistance with voltage and temperature.

Description	Nominal Voltage	dR/dT (%/°C)	dR/dV (%/mV)
OCT variation after calibration at device power-up	3.00	0.25	-0.027
	2.50	0.245	-0.04
	1.80	0.242	-0.079
	1.50	0.235	-0.125
	1.35	0.229	-0.16
	1.20	0.197	-0.208

Figure 1. Equation for OCT Resistance after Calibration at Device Power-Up

$$\Delta R_V = (V_2 - V_1) \times 1000 \times dR/dV$$

$$\Delta R_T = (T_2 - T_1) \times dR/dT$$

$$\text{For } \Delta R_X < 0; MF_X = 1/(|\Delta R_X|/100 + 1)$$

$$\text{For } \Delta R_X > 0; MF_X = \Delta R_X/100 + 1$$

$$MF = MF_V \times MF_T$$

$$R_{final} = R_{initial} \times MF$$

The definitions for equation are as follows:

- T_1 is the initial temperature.
- T_2 is the final temperature.
- MF is multiplication factor.
- $R_{initial}$ is initial resistance.
- R_{final} is final resistance.

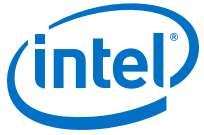
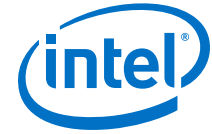


Table 19. Hysteresis Specifications for Schmitt Trigger Input for Intel MAX 10 Devices

Symbol	Parameter	Condition	Minimum	Unit
V _{HYS}	Hysteresis for Schmitt trigger input	V _{CCIO} = 3.3 V	180	mV
		V _{CCIO} = 2.5 V	150	mV
		V _{CCIO} = 1.8 V	120	mV
		V _{CCIO} = 1.5 V	110	mV

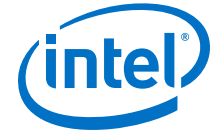


Single-Ended I/O Standards Specifications

Table 20. Single-Ended I/O Standards Specifications for Intel MAX 10 Devices

To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the 3.3-V LVTTTL specification (4 mA), you should set the current strength settings to 4 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3 V LVTTTL	3.135	3.3	3.465	-0.3	0.8	1.7	3.6	0.45	2.4	4	-4
3.3 V LVCMOS	3.135	3.3	3.465	-0.3	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	2	-2
3.0 V LVTTTL	2.85	3	3.15	-0.3	0.8	1.7	$V_{CCIO} + 0.3$	0.45	2.4	4	-4
3.0 V LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	$V_{CCIO} + 0.3$	0.2	$V_{CCIO} - 0.2$	0.1	-0.1
2.5 V LVTTTL and LVCMOS	2.375	2.5	2.625	-0.3	0.7	1.7	$V_{CCIO} + 0.3$	0.4	2	1	-1
1.8 V LVTTTL and LVCMOS	1.71	1.8	1.89	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	2.25	0.45	$V_{CCIO} - 0.45$	2	-2
1.5 V LVCMOS	1.425	1.5	1.575	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2
1.2 V LVCMOS	1.14	1.2	1.26	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2
3.3 V Schmitt Trigger	3.135	3.3	3.465	-0.3	0.8	1.7	$V_{CCIO} + 0.3$	—	—	—	—
2.5 V Schmitt Trigger	2.375	2.5	2.625	-0.3	0.7	1.7	$V_{CCIO} + 0.3$	—	—	—	—
1.8 V Schmitt Trigger	1.71	1.8	1.89	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	—	—	—	—
1.5 V Schmitt Trigger	1.425	1.5	1.575	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	—	—	—	—
3.0 V PCI	2.85	3	3.15	—	$0.3 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	1.5	-0.5



Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications

Table 22. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Intel MAX 10 Devices

To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL-15 Class I specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	$V_{IL(DC)} (V)$		$V_{IH(DC)} (V)$		$V_{IL(AC)} (V)$		$V_{IH(AC)} (V)$		$V_{OL} (V)$	$V_{OH} (V)$	$I_{OL} (mA)$	$I_{OH} (mA)$
	Min	Max	Min	Max	Min	Max	Min	Max	Max	Min		
SSTL-2 Class I	—	$V_{REF} - 0.18$	$V_{REF} + 0.18$	—	—	$V_{REF} - 0.31$	$V_{REF} + 0.31$	—	$V_{TT} - 0.57$	$V_{TT} + 0.57$	8.1	-8.1
SSTL-2 Class II	—	$V_{REF} - 0.18$	$V_{REF} + 0.18$	—	—	$V_{REF} - 0.31$	$V_{REF} + 0.31$	—	$V_{TT} - 0.76$	$V_{TT} + 0.76$	16.4	-16.4
SSTL-18 Class I	—	$V_{REF} - 0.125$	$V_{REF} + 0.125$	—	—	$V_{REF} - 0.25$	$V_{REF} + 0.25$	—	$V_{TT} - 0.475$	$V_{TT} + 0.475$	6.7	-6.7
SSTL-18 Class II	—	$V_{REF} - 0.125$	$V_{REF} + 0.125$	—	—	$V_{REF} - 0.25$	$V_{REF} + 0.25$	—	0.28	$V_{CCIO} - 0.28$	13.4	-13.4
SSTL-15 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	—	$V_{REF} - 0.175$	$V_{REF} + 0.175$	—	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	8	-8
SSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	—	$V_{REF} - 0.175$	$V_{REF} + 0.175$	—	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	16	-16
SSTL-135	—	$V_{REF} - 0.09$	$V_{REF} + 0.09$	—	—	$V_{REF} - 0.16$	$V_{REF} + 0.16$	—	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	—	—
HSTL-18 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	—	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-18 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	—	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-15 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	—	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	—	0.4	$V_{CCIO} - 0.4$	16	-16

continued...



I/O Standard	V _{IL(DC)} (V)		V _{IH(DC)} (V)		V _{IL(AC)} (V)		V _{IH(AC)} (V)		V _{OL} (V)	V _{OH} (V)	I _{OL} (mA)	I _{OH} (mA)
	Min	Max	Min	Max	Min	Max	Min	Max	Max	Min		
HSTL-12 Class I	-0.15	V _{REF} - 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	-0.24	V _{REF} - 0.15	V _{REF} + 0.15	V _{CCIO} + 0.24	0.25 × V _{CCIO}	0.75 × V _{CCIO}	8	-8
HSTL-12 Class II	-0.15	V _{REF} - 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	-0.24	V _{REF} - 0.15	V _{REF} + 0.15	V _{CCIO} + 0.24	0.25 × V _{CCIO}	0.75 × V _{CCIO}	14	-14
HSUL-12	—	V _{REF} - 0.13	V _{REF} + 0.13	—	—	V _{REF} - 0.22	V _{REF} + 0.22	—	0.1 × V _{CCIO}	0.9 × V _{CCIO}	—	—

Differential SSTL I/O Standards Specifications

Differential SSTL requires a V_{REF} input.

Table 23. Differential SSTL I/O Standards Specifications for Intel MAX 10 Devices

I/O Standard	V _{CCIO} (V)			V _{Swing(DC)} (V)		V _{X(AC)} (V)			V _{Swing(AC)} (V)	
	Min	Typ	Max	Min	Max ⁽¹⁷⁾	Min	Typ	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.36	V _{CCIO}	V _{CCIO} /2 - 0.2	—	V _{CCIO} /2 + 0.2	0.7	V _{CCIO}
SSTL-18 Class I, II	1.7	1.8	1.9	0.25	V _{CCIO}	V _{CCIO} /2 - 0.175	—	V _{CCIO} /2 + 0.175	0.5	V _{CCIO}
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	V _{CCIO} /2 - 0.15	—	V _{CCIO} /2 + 0.15	2(V _{IH(AC)} - V _{REF})	2(V _{IL(AC)} - V _{REF})
SSTL-135	1.283	1.35	1.45	0.18	—	V _{REF} - 0.135	0.5 × V _{CCIO}	V _{REF} + 0.135	2(V _{IH(AC)} - V _{REF})	2(V _{IL(AC)} - V _{REF})

Differential HSTL and HSUL I/O Standards Specifications

Differential HSTL requires a V_{REF} input.

⁽¹⁷⁾ The maximum value for V_{SWING(DC)} is not defined. However, each single-ended signal needs to be within the respective single-ended limits (V_{IH(DC)} and V_{IL(DC)}).

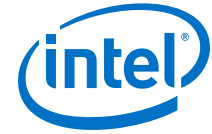


Table 24. Differential HSTL and HSUL I/O Standards Specifications for Intel MAX 10 Devices

I/O Standard	V _{CCIO} (V)			V _{DIF(DC)} (V)		V _{X(AC)} (V)			V _{CM(DC)} (V)			V _{DIF(AC)} (V)
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.85	—	0.95	0.85	—	0.95	0.4
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.71	—	0.79	0.71	—	0.79	0.4
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V _{CCIO}	$0.48 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.52 \times V_{CCIO}$	$0.48 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.52 \times V_{CCIO}$	0.3
HSUL-12	1.14	1.2	1.3	0.26	—	$0.5 \times V_{CCIO} - 0.12$	$0.5 \times V_{CCIO}$	$0.5 \times V_{CCIO} + 0.12$	$0.4 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.6 \times V_{CCIO}$	0.44

Differential I/O Standards Specifications

Table 25. Differential I/O Standards Specifications for Intel MAX 10 Devices

I/O Standard	V _{CCIO} (V)			V _{ID} (mV)		V _{ICM} (V) ⁽¹⁸⁾			V _{OD} (mV) ⁽¹⁹⁾⁽²⁰⁾			V _{OS} (V) ⁽¹⁹⁾		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVPECL ⁽²¹⁾	2.375	2.5	2.625	100	—	0.05	D _{MAX} ≤ 500 Mbps	1.8	—	—	—	—	—	—
						0.55	500 Mbps ≤ D _{MAX} ≤ 700 Mbps	1.8						
						1.05	D _{MAX} > 700 Mbps	1.55						
LVDS	2.375	2.5	2.625	100	—	0.05	D _{MAX} ≤ 500 Mbps	1.8	247	—	600	1.125	1.25	1.375
						0.55	500 Mbps ≤ D _{MAX} ≤ 700 Mbps	1.8						

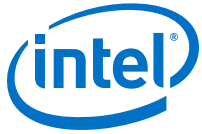
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⁽¹⁸⁾ V_{IN} range: 0 V ≤ V_{IN} ≤ 1.85 V.

⁽¹⁹⁾ R_L range: 90 ≤ R_L ≤ 110 Ω.

⁽²⁰⁾ Low V_{OD} setting is only supported for RSDS standard.

⁽²¹⁾ LVPECL input standard is only supported at clock input. Output standard is not supported.



Internal Oscillator Specifications

Table 32. Internal Oscillator Frequencies for Intel MAX 10 Devices

You can access to the internal oscillator frequencies in this table. The duty cycle of internal oscillator is approximately 45%–55%.

Device	Frequency			Unit
	Minimum	Typical	Maximum	
10M02	55	82	116	MHz
10M04				
10M08				
10M16				
10M25				
10M40	35	52	77	MHz
10M50				

UFM Performance Specifications

Table 33. UFM Performance Specifications for Intel MAX 10 Devices

Block	Mode	Interface	Device	Frequency		Unit
				Minimum	Maximum	
UFM	Avalon®-MM slave	Parallel ⁽³³⁾	10M02 ⁽³⁴⁾	3.43	7.25	MHz
			10M04, 10M08, 10M16, 10M25, 10M40, 10M50	5	116	MHz
		Serial ⁽³⁴⁾	10M02, 10M04, 10M08, 10M16, 10M25	3.43	7.25	MHz
			10M40, 10M50	2.18	4.81	MHz

⁽³³⁾ Clock source is derived from user, except for 10M02 device.

⁽³⁴⁾ Clock source is derived from 1/16 of the frequency of the internal oscillator.



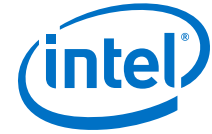
True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications

Table 36. True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

True **PPDS** transmitter is only supported at bottom I/O banks. Emulated **PPDS** transmitter is supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	-I6, -A6, -C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{HCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	—	155	5	—	155	5	—	155	MHz
		×8	5	—	155	5	—	155	5	—	155	MHz
		×7	5	—	155	5	—	155	5	—	155	MHz
		×4	5	—	155	5	—	155	5	—	155	MHz
		×2	5	—	155	5	—	155	5	—	155	MHz
		×1	5	—	310	5	—	310	5	—	310	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	—	310	100	—	310	100	—	310	Mbps
		×8	80	—	310	80	—	310	80	—	310	Mbps
		×7	70	—	310	70	—	310	70	—	310	Mbps
		×4	40	—	310	40	—	310	40	—	310	Mbps
		×2	20	—	310	20	—	310	20	—	310	Mbps
		×1	10	—	310	10	—	310	10	—	310	Mbps
f _{HCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	—	150	5	—	150	5	—	150	MHz
		×8	5	—	150	5	—	150	5	—	150	MHz
		×7	5	—	150	5	—	150	5	—	150	MHz
		×4	5	—	150	5	—	150	5	—	150	MHz
		×2	5	—	150	5	—	150	5	—	150	MHz
		×1	5	—	300	5	—	300	5	—	300	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	—	300	100	—	300	100	—	300	Mbps
		×8	80	—	300	80	—	300	80	—	300	Mbps
		×7	70	—	300	70	—	300	70	—	300	Mbps

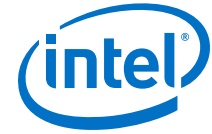
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Symbol	Parameter	Mode	-I6, -A6, -C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×4	40	—	300	40	—	300	40	—	300	Mbps
		×2	20	—	300	20	—	300	20	—	300	Mbps
		×1	10	—	300	10	—	300	10	—	300	Mbps
t _{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS ⁽⁵⁷⁾	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
t _{x Jitter} ⁽⁵⁸⁾	Output jitter (high-speed I/O performance pin)	—	—	—	425	—	—	425	—	—	425	ps
	Output jitter (low-speed I/O performance pin)	—	—	—	470	—	—	470	—	—	470	ps
t _{RISE}	Rise time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{FALL}	Fall time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

⁽⁵⁷⁾ TCCS specifications apply to I/O banks from the same side only.

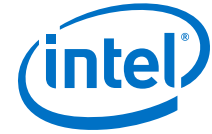
⁽⁵⁸⁾ TX jitter is the jitter induced from core noise and I/O switching noise.



Symbol	Parameter	Mode	-I6, -A6, -C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×4	40	—	170	40	—	170	40	—	170	Mbps
		×2	20	—	170	20	—	170	20	—	170	Mbps
		×1	10	—	170	10	—	170	10	—	170	Mbps
t _{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS ⁽⁵⁹⁾	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
t _{x Jitter} ⁽⁶⁰⁾	Output jitter (high-speed I/O performance pin)	—	—	—	425	—	—	425	—	—	425	ps
	Output jitter (low-speed I/O performance pin)	—	—	—	470	—	—	470	—	—	470	ps
t _{RISE}	Rise time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{FALL}	Fall time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

⁽⁵⁹⁾ TCCS specifications apply to I/O banks from the same side only.

⁽⁶⁰⁾ TX jitter is the jitter induced from core noise and I/O switching noise.



Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications

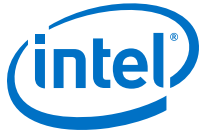
Single Supply Devices Emulated LVDS_E_3R Transmitter Timing Specifications

Table 43. Emulated LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices

Emulated LVDS_E_3R transmitters are supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	-C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{HCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	—	142.5	5	—	100	5	—	100	MHz
		×8	5	—	142.5	5	—	100	5	—	100	MHz
		×7	5	—	142.5	5	—	100	5	—	100	MHz
		×4	5	—	142.5	5	—	100	5	—	100	MHz
		×2	5	—	142.5	5	—	100	5	—	100	MHz
		×1	5	—	285	5	—	200	5	—	200	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	—	285	100	—	200	100	—	200	Mbps
		×8	80	—	285	80	—	200	80	—	200	Mbps
		×7	70	—	285	70	—	200	70	—	200	Mbps
		×4	40	—	285	40	—	200	40	—	200	Mbps
		×2	20	—	285	20	—	200	20	—	200	Mbps
		×1	10	—	285	10	—	200	10	—	200	Mbps
f _{HCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	—	100	5	—	100	5	—	100	MHz
		×8	5	—	100	5	—	100	5	—	100	MHz
		×7	5	—	100	5	—	100	5	—	100	MHz
		×4	5	—	100	5	—	100	5	—	100	MHz
		×2	5	—	100	5	—	100	5	—	100	MHz
		×1	5	—	200	5	—	200	5	—	200	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	—	200	100	—	200	100	—	200	Mbps

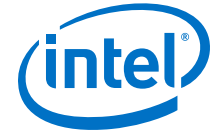
continued...



Symbol	Parameter	Mode	-I6, -A6, -C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×7	70	—	300	70	—	300	70	—	300	Mbps
		×4	40	—	300	40	—	300	40	—	300	Mbps
		×2	20	—	300	20	—	300	20	—	300	Mbps
		×1	10	—	300	10	—	300	10	—	300	Mbps
t _{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS ⁽⁶⁹⁾	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
t _{x jitter} ⁽⁷⁰⁾	Output jitter (high-speed I/O performance pin)	—	—	—	425	—	—	425	—	—	425	ps
	Output jitter (low-speed I/O performance pin)	—	—	—	470	—	—	470	—	—	470	ps
t _{RISE}	Rise time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{FALL}	Fall time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

⁽⁶⁹⁾ TCCS specifications apply to I/O banks from the same side only.

⁽⁷⁰⁾ TX jitter is the jitter induced from core noise and I/O switching noise.



LVDS, TMDs, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications

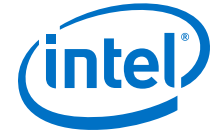
Single Supply Devices LVDS Receiver Timing Specifications

Table 45. LVDS Receiver Timing Specifications for Intel MAX 10 Single Supply Devices

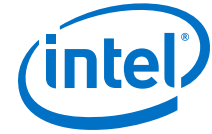
LVDS receivers are supported at all banks.

Symbol	Parameter	Mode	-C7, -I7		-A7		-C8		Unit
			Min	Max	Min	Max	Min	Max	
f_{HCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	145	5	100	5	100	MHz
		×8	5	145	5	100	5	100	MHz
		×7	5	145	5	100	5	100	MHz
		×4	5	145	5	100	5	100	MHz
		×2	5	145	5	100	5	100	MHz
		×1	5	290	5	200	5	200	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	290	100	200	100	200	Mbps
		×8	80	290	80	200	80	200	Mbps
		×7	70	290	70	200	70	200	Mbps
		×4	40	290	40	200	40	200	Mbps
		×2	20	290	20	200	20	200	Mbps
		×1	10	290	10	200	10	200	Mbps
f_{HCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	100	5	100	5	100	MHz
		×8	5	100	5	100	5	100	MHz
		×7	5	100	5	100	5	100	MHz
		×4	5	100	5	100	5	100	MHz
		×2	5	100	5	100	5	100	MHz
		×1	5	200	5	200	5	200	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	200	100	200	100	200	Mbps

continued...



Symbol	Parameter	Mode	-I6, -A6, -C7, -I7		-A7		-C8		Unit
			Min	Max	Min	Max	Min	Max	
		×2	5	360	5	320	5	320	MHz
		×1	5	360	5	320	5	320	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	700	100	640	100	640	Mbps
		×8	80	720	80	640	80	640	Mbps
		×7	70	700	70	640	70	640	Mbps
		×4	40	720	40	640	40	640	Mbps
		×2	20	720	20	640	20	640	Mbps
		×1	10	360	10	320	10	320	Mbps
f _{HSCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	150	5	150	5	150	MHz
		×8	5	150	5	150	5	150	MHz
		×7	5	150	5	150	5	150	MHz
		×4	5	150	5	150	5	150	MHz
		×2	5	150	5	150	5	150	MHz
		×1	5	300	5	300	5	300	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	300	100	300	100	300	Mbps
		×8	80	300	80	300	80	300	Mbps
		×7	70	300	70	300	70	300	Mbps
		×4	40	300	40	300	40	300	Mbps
		×2	20	300	20	300	20	300	Mbps
		×1	10	300	10	300	10	300	Mbps
SW	Sampling window (high-speed I/O performance pin)	—	—	510	—	510	—	510	ps
continued...									



Memory Output Clock Jitter Specifications

Intel MAX 10 devices support external memory interfaces up to 303 MHz. The external memory interfaces for Intel MAX 10 devices calibrate automatically.

The memory output clock jitter measurements are for 200 consecutive clock cycles.

The clock jitter specification applies to memory output clock pins generated using DDIO circuits clocked by a PLL output routed on a PHY clock network.

DDR3 and LPDDR2 SDRAM memory interfaces are only supported on the fast speed grade device.

Table 48. Memory Output Clock Jitter Specifications for Intel MAX 10 Devices

Parameter	Symbol	–6 Speed Grade		–7 Speed Grade		Unit
		Min	Max	Min	Max	
Clock period jitter	$t_{JIT(per)}$	–127	127	–215	215	ps
Cycle-to-cycle period jitter	$t_{JIT(cc)}$	—	242	—	360	ps

Related Information

[Literature: External Memory Interfaces](#)

Provides more information about external memory system performance specifications, board design guidelines, timing analysis, simulation, and debugging information.

Configuration Specifications

This section provides configuration specifications and timing for Intel MAX 10 devices.

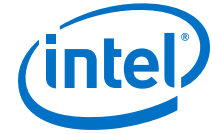


Table 54. Internal Configuration Time for Intel MAX 10 Devices (Compressed .rbf)

Compression ratio depends on design complexity. The minimum value is based on the best case (25% of original .rbf sizes) and the maximum value is based on the typical case (70% of original .rbf sizes).

Device	Internal Configuration Time (ms)			
	Unencrypted/Encrypted			
	Without Memory Initialization		With Memory Initialization	
	Min	Max	Min	Max
10M02	0.3	5.2	—	—
10M04	0.6	10.7	1.0	13.9
10M08	0.6	10.7	1.0	13.9
10M16	1.1	17.9	1.4	22.3
10M25	1.1	26.9	1.4	32.2
10M40	2.6	66.1	3.2	82.2
10M50	2.6	66.1	3.2	82.2

Internal Configuration Timing Parameter

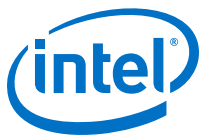
Table 55. Internal Configuration Timing Parameter for Intel MAX 10 Devices

Symbol	Parameter	Device	Minimum	Maximum	Unit
t_{CD2UM}	CONF_DONE high to user mode	10M02, 10M04, 10M08, 10M16, 10M25	182.8	385.5	μs
		10M40, 10M50	275.3	605.7	μs

I/O Timing

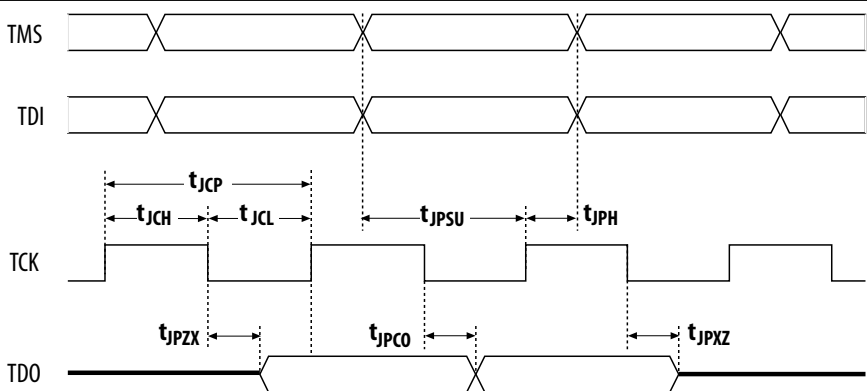
The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

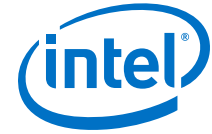
The Intel Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specific device and design after you complete place-and-route.



Glossary

Table 59. Glossary

Term	Definition
JTAG Timing Specifications	 The diagram illustrates the JTAG timing specifications. It shows four signals: TMS, TDI, TCK, and TDO. TMS and TDI are shown as square waves. TCK is a clock signal. TDO is a data signal. Various timing parameters are labeled: t_{JCP} (JTAG capture period), t_{JCH} (JTAG capture high), t_{JCL} (JTAG capture low), t_{JPSU} (JTAG setup), t_{JPH} (JTAG high), t_{JPZX} (JTAG pull-up to high-Z), and t_{JPCO} (JTAG pull-down to low-Z).
R_L	Receiver differential input discrete resistor (external to Intel MAX 10 devices).
RSKM (Receiver input skew margin)	HIGH-SPEED I/O block: The total margin left after accounting for the sampling window and TCCS. $RSKM = (TUI - SW - TCCS) / 2$.
Sampling window (SW)	HIGH-SPEED I/O Block: The period of time during which the data must be valid to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window.
Single-ended voltage referenced I/O standard	The AC input signal values indicate the voltage levels at which the receiver must meet its timing specifications. The DC input signal values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input crosses the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing.
t_c	High-speed receiver/transmitter input and output clock period.
TCCS (Channel-to- channel-skew)	HIGH-SPEED I/O block: The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
t_{cin}	Delay from clock pad to I/O input register.
t_{CO}	Delay from clock pad to I/O output.
t_{cout}	Delay from clock pad to I/O output register.
continued...	



Date	Version	Changes
		- Added –A6 speed grade in the following tables: - Intel MAX 10 Device Grades and Speed Grades Supported - Series OCT without Calibration Specifications for Intel MAX 10 Devices - Clock Tree Specifications for Intel MAX 10 Devices - Embedded Multiplier Specifications for Intel MAX 10 Devices - Memory Block Performance Specifications for Intel MAX 10 Devices - True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices - True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices - Emulated RSDS_E_1R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices - True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices - True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices - Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices - LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices - IOE Programmable Delay on Row Pins for Intel MAX 10 Devices - IOE Programmable Delay on Column Pins for Intel MAX 10 Devices - Updated the maximum value for input clock cycle-to-cycle jitter ($t_{INJITTER_CCJ}$) with $F_{INPFD} < 100$ MHz condition from 750 ps to ± 750 ps in PLL Specifications for Intel MAX 10 Devices table. - Updated the dual supply mode performance in Embedded Multiplier Specifications for Intel MAX 10 Devices table. - Updated the dual supply mode performance in Memory Block Performance Specifications for Intel MAX 10 Devices table. - Added typical specifications in Internal Oscillator Frequencies for Intel MAX 10 Devices table. - Updated specifications in UFM Performance Specifications for Intel MAX 10 Devices table. - Updated sampling window specifications in LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices table. - Updated IOE programmable delay for row and column pins. - Changed instances of <i>Quartus II</i> to <i>Quartus Prime</i>.
June 2015	2015.06.12	- Updated the maximum values in Internal Weak Pull-Up Resistor for Intel MAX 10 Devices table. - Removed Internal Weak Pull-Up Resistor equation. - Updated the note for input resistance and input capacitance parameters in the ADC Performance Specifications table for both single supply and dual supply devices. Note: Download the SPICE models for simulation. - Added a note to AC Accuracy - THD, SNR, and SINAD parameters in the ADC Performance Specifications for Intel MAX 10 Dual Supply Devices table. Note: When using internal V_{REF}, THD = 66 dB, SNR = 58 dB and SINAD = 57.5 dB for dedicated ADC input channels. - Updated clock period jitter and cycle-to-cycle period jitter parameters in the Memory Output Clock Jitter Specifications for Intel MAX 10 Devices table.
continued...		