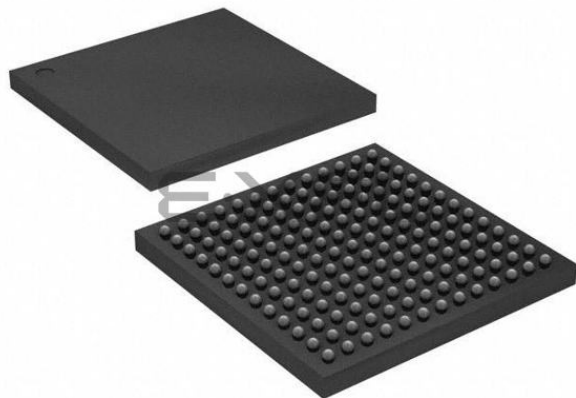




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

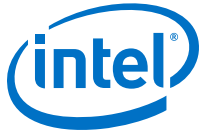
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	1000
Number of Logic Elements/Cells	16000
Total RAM Bits	562176
Number of I/O	130
Number of Gates	-
Voltage - Supply	2.85V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	169-LFBGA
Supplier Device Package	169-UBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10m16scu169a7g



Operating Conditions

Intel MAX 10 devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Intel MAX 10 devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions for Intel MAX 10 devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Caution: Conditions outside the range listed in the absolute maximum ratings tables may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Single Supply Devices Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings for Intel MAX 10 Single Supply Devices

Symbol	Parameter	Min	Max	Unit
V _{CC_ONE}	Supply voltage for core and periphery through on-die voltage regulator	-0.5	3.9	V
V _{CCIO}	Supply voltage for input and output buffers	-0.5	3.9	V
V _{CCA}	Supply voltage for phase-locked loop (PLL) regulator and analog-to-digital converter (ADC) block (analog)	-0.5	3.9	V

Dual Supply Devices Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings for Intel MAX 10 Dual Supply Devices

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply voltage for core and periphery	-0.5	1.63	V
V _{CCIO}	Supply voltage for input and output buffers	-0.5	3.9	V
V _{CCA}	Supply voltage for PLL regulator (analog)	-0.5	3.41	V
continued...				

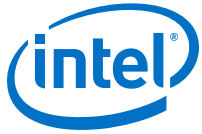


Table 11. ADC_VREF Pin Leakage Current for Intel MAX 10 Devices

Symbol	Parameter	Condition	Min	Max	Unit
$I_{\text{adc_vref}}$	ADC_VREF pin leakage current	Single supply mode	—	10	μA
		Dual supply mode	—	20	μA

Bus Hold Parameters

Bus hold retains the last valid logic state after the source driving it either enters the high impedance state or is removed. Each I/O pin has an option to enable bus hold in user mode. Bus hold is always disabled in configuration mode.

Table 12. Bus Hold Parameters for Intel MAX 10 Devices

Parameter	Condition	V _{CCIO} (V)												Unit
		1.2		1.5		1.8		2.5		3.0		3.3		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold low, sustaining current	V _{IN} > V _{IL} (maximum)	8	—	12	—	30	—	50	—	70	—	70	—	μA
Bus-hold high, sustaining current	V _{IN} < V _{IH} (minimum)	–8	—	–12	—	–30	—	–50	—	–70	—	–70	—	μA
Bus-hold low, overdrive current	0 V < V _{IN} < V _{CCIO}	—	125	—	175	—	200	—	300	—	500	—	500	μA
Bus-hold high, overdrive current	0 V < V _{IN} < V _{CCIO}	—	–125	—	–175	—	–200	—	–300	—	–500	—	–500	μA
Bus-hold trip point	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

Table 15. OCT Variation after Calibration at Device Power-Up for Intel MAX 10 Devices

This table lists the change percentage of the OCT resistance with voltage and temperature.

Description	Nominal Voltage	dR/dT (%/°C)	dR/dV (%/mV)
OCT variation after calibration at device power-up	3.00	0.25	-0.027
	2.50	0.245	-0.04
	1.80	0.242	-0.079
	1.50	0.235	-0.125
	1.35	0.229	-0.16
	1.20	0.197	-0.208

Figure 1. Equation for OCT Resistance after Calibration at Device Power-Up

$$\Delta R_V = (V_2 - V_1) \times 1000 \times dR/dV$$

$$\Delta R_T = (T_2 - T_1) \times dR/dT$$

$$\text{For } \Delta R_X < 0; MF_X = 1/(|\Delta R_X|/100 + 1)$$

$$\text{For } \Delta R_X > 0; MF_X = \Delta R_X/100 + 1$$

$$MF = MF_V \times MF_T$$

$$R_{final} = R_{initial} \times MF$$

The definitions for equation are as follows:

- T_1 is the initial temperature.
- T_2 is the final temperature.
- MF is multiplication factor.
- $R_{initial}$ is initial resistance.
- R_{final} is final resistance.



- Subscript x refers to both V and T.
- ΔR_V is variation of resistance with voltage.
- ΔR_T is variation of resistance with temperature.
- dR/dT is the change percentage of resistance with temperature after calibration at device power-up.
- dR/dV is the change percentage of resistance with voltage after calibration at device power-up.
- V_1 is the initial voltage.
- V_2 is final voltage.

The following figure shows the example to calculate the change of 50 Ω I/O impedance from 25°C at 3.0 V to 85°C at 3.15 V.

Figure 2. Example for OCT Resistance Calculation after Calibration at Device Power-Up

$$\Delta R_V = (3.15 - 3) \times 1000 \times -0.027 = -4.05$$

$$\Delta R_T = (85 - 25) \times 0.25 = 15$$

Because ΔR_V is negative,

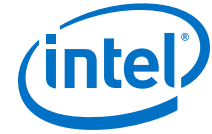
$$MF_V = 1/(4.05/100 + 1) = 0.961$$

Because ΔR_T is positive,

$$MF_T = 15/100 + 1 = 1.15$$

$$MF = 0.961 \times 1.15 = 1.105$$

$$R_{final} = 50 \times 1.105 = 55.25\Omega$$



I/O Standard	V _{CCIO} (V)			V _{ID} (mV)		V _{ICM} (V) ⁽¹⁸⁾			V _{OD} (mV) ⁽¹⁹⁾⁽²⁰⁾			V _{OS} (V) ⁽¹⁹⁾		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
HiSpi	2.375	2.5	2.625	100	—	0.05	D _{MAX} ≤ 500 Mbps	1.8	—	—	—	—	—	—
						0.55	500 Mbps ≤ D _{MAX} ≤ 700 Mbps	1.8						
						1.05	D _{MAX} > 700 Mbps	1.55						

Related Information

[Intel MAX 10 LVDS SERDES I/O Standards Support, Intel MAX 10 High-Speed LVDS I/O User Guide](#)
Provides the list of I/O standards supported in single supply and dual supply devices.

Switching Characteristics

This section provides the performance characteristics of Intel MAX 10 core and periphery blocks.

⁽¹⁸⁾ V_{IN} range: 0 V ≤ V_{IN} ≤ 1.85 V.

⁽¹⁹⁾ R_L range: 90 Ω ≤ R_L ≤ 110 Ω.

⁽²⁰⁾ Low V_{OD} setting is only supported for RSDS standard.

⁽²²⁾ No fixed V_{IN}, V_{OD}, and V_{OS} specifications for Bus LVDS (BLVDS). They are dependent on the system topology.

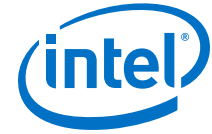
⁽²³⁾ Mini-LVDS, RSDS, and Point-to-Point Differential Signaling (PPDS) standards are only supported at the output pins for Intel MAX 10 devices.

⁽²⁴⁾ Supported with requirement of an external level shift

⁽²⁵⁾ Sub-LVDS input buffer is using 2.5 V differential buffer.

⁽²⁶⁾ Differential output depends on the values of the external termination resistors.

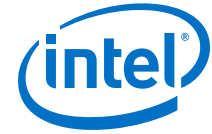
⁽²⁷⁾ Differential output offset voltage depends on the values of the external termination resistors.



Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{VCO} ⁽²⁹⁾	PLL internal voltage-controlled oscillator (VCO) operating range	—	600	—	1300	MHz
f_{INDUTY}	Input clock duty cycle	—	40	—	60	%
$t_{INJITTER_CCJ}$ ⁽³⁰⁾	Input clock cycle-to-cycle jitter	$F_{INPFD} \geq 100$ MHz	—	—	0.15	UI
		$F_{INPFD} < 100$ MHz	—	—	±750	ps
f_{OUT_EXT} ⁽²⁸⁾	PLL output frequency for external clock output	—	—	—	472.5	MHz
f_{OUT}	PLL output frequency to global clock	–6 speed grade	—	—	472.5	MHz
		–7 speed grade	—	—	450	MHz
		–8 speed grade	—	—	402.5	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output	Duty cycle set to 50%	45	50	55	%
t_{LOCK}	Time required to lock from end of device configuration	—	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically	After switchover, reconfiguring any non-post-scale counters or delays, or when areset is deasserted	—	—	1	ms
$t_{OUTJITTER_PERIOD_IO}$ ⁽³¹⁾	Regular I/O period jitter	$F_{OUT} \geq 100$ MHz	—	—	650	ps
		$F_{OUT} < 100$ MHz	—	—	75	mUI
$t_{OUTJITTER_CCJ_IO}$ ⁽³¹⁾	Regular I/O cycle-to-cycle jitter	$F_{OUT} \geq 100$ MHz	—	—	650	ps
		$F_{OUT} < 100$ MHz	—	—	75	mUI

continued...

- ⁽²⁹⁾ The VCO frequency reported by the Intel Quartus Prime software in the PLL summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.
- ⁽³⁰⁾ A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source, which is less than 200 ps.
- ⁽³¹⁾ Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied.



Embedded Multiplier Specifications

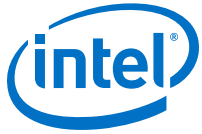
Table 30. Embedded Multiplier Specifications for Intel MAX 10 Devices

Mode	Number of Multipliers	Power Supply Mode	Performance			Unit
			-I6	-A6, -C7, -I7, -A7	-C8	
9 × 9-bit multiplier	1	Single supply mode	198	183	160	MHz
		Dual supply mode	310	260	210	MHz
18 × 18-bit multiplier	1	Single supply mode	198	183	160	MHz
		Dual supply mode	265	240	190	MHz

Memory Block Performance Specifications

Table 31. Memory Block Performance Specifications for Intel MAX 10 Devices

Memory	Mode	Resources Used		Power Supply Mode	Performance			Unit
		LEs	M9K Memory		-I6	-A6, -C7, -I7, -A7	-C8	
M9K Block	FIFO 256 × 36	47	1	Single supply mode	232	219	204	MHz
				Dual supply mode	330	300	250	MHz
	Single-port 256 × 36	0	1	Single supply mode	232	219	204	MHz
				Dual supply mode	330	300	250	MHz
	Simple dual-port 256 × 36 CLK	0	1	Single supply mode	232	219	204	MHz
				Dual supply mode	330	300	250	MHz
	True dual port 512 × 18 single CLK	0	1	Single supply mode	232	219	204	MHz
				Dual supply mode	330	300	250	MHz



Parameter		Symbol	Condition	Min	Typ	Max	Unit
	Integral non linearity	INL	—	–2	—	2	LSB
AC Accuracy	Total harmonic distortion	THD	$F_{IN} = 50 \text{ kHz}$, $F_S = 1 \text{ MHz}$, PLL	–65 ⁽³⁷⁾	—	—	dB
	Signal-to-noise ratio	SNR	$F_{IN} = 50 \text{ kHz}$, $F_S = 1 \text{ MHz}$, PLL	54 ⁽³⁸⁾	—	—	dB
	Signal-to-noise and distortion	SINAD	$F_{IN} = 50 \text{ kHz}$, $F_S = 1 \text{ MHz}$, PLL	53 ⁽³⁹⁾	—	—	dB
On-Chip Temperature Sensor	Temperature sampling rate	T_S	—	—	—	50	kSPS
	Absolute accuracy	—	–40 to 125°C, with 64 samples averaging ⁽⁴⁰⁾	—	—	±10	°C
Conversion Rate ⁽⁴¹⁾	Conversion time	—	Single measurement	—	—	1	Cycle
			Continuous measurement	—	—	1	Cycle
			Temperature measurement	—	—	1	Cycle

Related Information

[SPICE Models for Intel FPGAs](#)

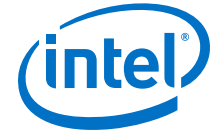
⁽³⁷⁾ THD with prescaler enabled is 6dB less than the specification.

⁽³⁸⁾ SNR with prescaler enabled is 6dB less than the specification.

⁽³⁹⁾ SINAD with prescaler enabled is 6dB less than the specification.

⁽⁴⁰⁾ For the Intel Quartus Prime software version 15.0 and later, Modular ADC Core Intel FPGA IP and Modular Dual ADC Core Intel FPGA IP cores handle the 64 samples averaging. For the Intel Quartus Prime software versions prior to 14.1, you need to implement your own averaging calculation.

⁽⁴¹⁾ For more detailed description, refer to the Timing section in the *Intel MAX 10 Analog-to-Digital Converter User Guide*.



Dual Supply Devices ADC Performance Specifications

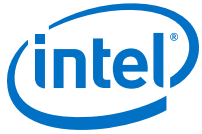
Table 35. ADC Performance Specifications for Intel MAX 10 Dual Supply Devices

Parameter		Symbol	Condition	Min	Typ	Max	Unit
ADC resolution		—	—	—	—	12	bits
Analog supply voltage		V_{CCA_ADC}	—	2.375	2.5	2.625	V
Digital supply voltage		V_{CCINT}	—	1.15	1.2	1.25	V
External reference voltage		V_{REF}	—	$V_{CCA_ADC} - 0.5$	—	V_{CCA_ADC}	V
Sampling rate		F_S	Accumulative sampling rate	—	—	1	MSPS
Operating junction temperature range		T_J	—	-40	25	125	°C
Analog input voltage		V_{IN}	Prescaler disabled	0	—	V_{REF}	V
			Prescaler enabled ⁽⁴²⁾	0	—	3	V
Analog supply current (DC)		I_{ACC_ADC}	Average current	—	275	450	μA
Digital supply current (DC)		I_{CCINT}	Average current	—	65	150	μA
Input resistance		R_{IN}	—	—	⁽⁴³⁾	—	—
Input capacitance		C_{IN}	—	—	⁽⁴³⁾	—	—
DC Accuracy	Offset error and drift	E_{offset}	Prescaler disabled	-0.2	—	0.2	%FS
			Prescaler enabled	-0.5	—	0.5	%FS
	Gain error and drift	E_{gain}	Prescaler disabled	-0.5	—	0.5	%FS
			Prescaler enabled	-0.75	—	0.75	%FS
	Differential non linearity	DNL	External V_{REF} , no missing code	-0.9	—	0.9	LSB

continued...

⁽⁴²⁾ Prescaler function divides the analog input voltage by half. The analog input handles up to 3 V input for the Intel MAX 10 dual supply devices.

⁽⁴³⁾ Download the SPICE models for simulation.



Parameter	Symbol	Condition	Min	Typ	Max	Unit
		Internal V_{REF} , no missing code	-1	—	1.7	LSB
	INL	—	-2	—	2	LSB
AC Accuracy	Total harmonic distortion	$F_{IN} = 50 \text{ kHz}$, $F_S = 1 \text{ MHz}$, PLL	-70 ⁽⁴⁴⁾⁽⁴⁵⁾ (46)	—	—	dB
	Signal-to-noise ratio	$F_{IN} = 50 \text{ kHz}$, $F_S = 1 \text{ MHz}$, PLL	62 ⁽⁴⁷⁾⁽⁴⁸⁾ (46)	—	—	dB
	Signal-to-noise and distortion	$F_{IN} = 50 \text{ kHz}$, $F_S = 1 \text{ MHz}$, PLL	61.5 ⁽⁴⁹⁾ (50)(46)	—	—	dB
On-Chip Temperature Sensor	Temperature sampling rate	T_S	—	—	50	kSPS
	Absolute accuracy	—	-40 to 125°C, with 64 samples averaging (51)	—	±5	°C
continued...						

(44) Total harmonic distortion is -65 dB for dual function pin.

(45) THD with prescaler enabled is 6dB less than the specification.

(46) When using internal V_{REF} , THD = 66 dB, SNR = 58 dB and SINAD = 57.5 dB for dedicated ADC input channels.

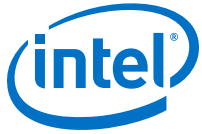
(47) Signal-to-noise ratio is 54 dB for dual function pin.

(48) SNR with prescaler enabled is 6dB less than the specification.

(49) Signal-to-noise and distortion is 53 dB for dual function pin.

(50) SINAD with prescaler enabled is 6dB less than the specification.

(51) For the Intel Quartus Prime software version 15.0 and later, Modular ADC Core and Modular Dual ADC Core IP cores handle the 64 samples averaging. For the Intel Quartus Prime software versions prior to 14.1, you need to implement your own averaging calculation.



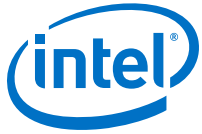
True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications

Table 36. True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

True **PPDS** transmitter is only supported at bottom I/O banks. Emulated **PPDS** transmitter is supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	-I6, -A6, -C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{HCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	—	155	5	—	155	5	—	155	MHz
		×8	5	—	155	5	—	155	5	—	155	MHz
		×7	5	—	155	5	—	155	5	—	155	MHz
		×4	5	—	155	5	—	155	5	—	155	MHz
		×2	5	—	155	5	—	155	5	—	155	MHz
		×1	5	—	310	5	—	310	5	—	310	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	—	310	100	—	310	100	—	310	Mbps
		×8	80	—	310	80	—	310	80	—	310	Mbps
		×7	70	—	310	70	—	310	70	—	310	Mbps
		×4	40	—	310	40	—	310	40	—	310	Mbps
		×2	20	—	310	20	—	310	20	—	310	Mbps
		×1	10	—	310	10	—	310	10	—	310	Mbps
f _{HCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	—	150	5	—	150	5	—	150	MHz
		×8	5	—	150	5	—	150	5	—	150	MHz
		×7	5	—	150	5	—	150	5	—	150	MHz
		×4	5	—	150	5	—	150	5	—	150	MHz
		×2	5	—	150	5	—	150	5	—	150	MHz
		×1	5	—	300	5	—	300	5	—	300	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	—	300	100	—	300	100	—	300	Mbps
		×8	80	—	300	80	—	300	80	—	300	Mbps
		×7	70	—	300	70	—	300	70	—	300	Mbps

continued...



Emulated RSDS_E_1R Transmitter Timing Specifications

Table 39. Emulated RSDS_E_1R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

Emulated **RSDS_E_1R** transmitter is supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{HCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	—	85	5	—	85	5	—	85	MHz
		×8	5	—	85	5	—	85	5	—	85	MHz
		×7	5	—	85	5	—	85	5	—	85	MHz
		×4	5	—	85	5	—	85	5	—	85	MHz
		×2	5	—	85	5	—	85	5	—	85	MHz
		×1	5	—	170	5	—	170	5	—	170	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	—	170	100	—	170	100	—	170	Mbps
		×8	80	—	170	80	—	170	80	—	170	Mbps
		×7	70	—	170	70	—	170	70	—	170	Mbps
		×4	40	—	170	40	—	170	40	—	170	Mbps
		×2	20	—	170	20	—	170	20	—	170	Mbps
		×1	10	—	170	10	—	170	10	—	170	Mbps
f _{HCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	—	85	5	—	85	5	—	85	MHz
		×8	5	—	85	5	—	85	5	—	85	MHz
		×7	5	—	85	5	—	85	5	—	85	MHz
		×4	5	—	85	5	—	85	5	—	85	MHz
		×2	5	—	85	5	—	85	5	—	85	MHz
		×1	5	—	170	5	—	170	5	—	170	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	—	170	100	—	170	100	—	170	Mbps
		×8	80	—	170	80	—	170	80	—	170	Mbps
		×7	70	—	170	70	—	170	70	—	170	Mbps

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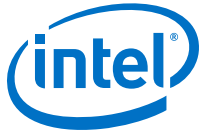
True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications

Table 40. True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

True **mini-LVDS** transmitter is only supported at the bottom I/O banks. Emulated **mini-LVDS_E_3R** transmitter is supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	-I6, -A6, -C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{HCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	—	155	5	—	155	5	—	155	MHz
		×8	5	—	155	5	—	155	5	—	155	MHz
		×7	5	—	155	5	—	155	5	—	155	MHz
		×4	5	—	155	5	—	155	5	—	155	MHz
		×2	5	—	155	5	—	155	5	—	155	MHz
		×1	5	—	310	5	—	310	5	—	310	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	—	310	100	—	310	100	—	310	Mbps
		×8	80	—	310	80	—	310	80	—	310	Mbps
		×7	70	—	310	70	—	310	70	—	310	Mbps
		×4	40	—	310	40	—	310	40	—	310	Mbps
		×2	20	—	310	20	—	310	20	—	310	Mbps
		×1	10	—	310	10	—	310	10	—	310	Mbps
f _{HCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	—	150	5	—	150	5	—	150	MHz
		×8	5	—	150	5	—	150	5	—	150	MHz
		×7	5	—	150	5	—	150	5	—	150	MHz
		×4	5	—	150	5	—	150	5	—	150	MHz
		×2	5	—	150	5	—	150	5	—	150	MHz
		×1	5	—	300	5	—	300	5	—	300	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	—	300	100	—	300	100	—	300	Mbps
		×8	80	—	300	80	—	300	80	—	300	Mbps

continued...



True LVDS Transmitter Timing

Single Supply Devices True LVDS Transmitter Timing Specifications

Table 41. True LVDS Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices

True LVDS transmitter is only supported at the bottom I/O banks.

Symbol	Parameter	Mode	-C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{HCLK}	Input clock frequency	×10	5	—	145	5	—	100	5	—	100	MHz
		×8	5	—	145	5	—	100	5	—	100	MHz
		×7	5	—	145	5	—	100	5	—	100	MHz
		×4	5	—	145	5	—	100	5	—	100	MHz
		×2	5	—	145	5	—	100	5	—	100	MHz
		×1	5	—	290	5	—	200	5	—	200	MHz
HSIODR	Data rate	×10	100	—	290	100	—	200	100	—	200	Mbps
		×8	80	—	290	80	—	200	80	—	200	Mbps
		×7	70	—	290	70	—	200	70	—	200	Mbps
		×4	40	—	290	40	—	200	40	—	200	Mbps
		×2	20	—	290	20	—	200	20	—	200	Mbps
		×1	10	—	290	10	—	200	10	—	200	Mbps
t _{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS ⁽⁶³⁾	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
t _{x jitter} ⁽⁶⁴⁾	Output jitter	—	—	—	1,000	—	—	1,000	—	—	1,000	ps

continued...

⁽⁶³⁾ TCCS specifications apply to I/O banks from the same side only.

⁽⁶⁴⁾ TX jitter is the jitter induced from core noise and I/O switching noise.



Symbol	Parameter	Mode	-C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×8	80	—	200	80	—	200	80	—	200	Mbps
		×7	70	—	200	70	—	200	70	—	200	Mbps
		×4	40	—	200	40	—	200	40	—	200	Mbps
		×2	20	—	200	20	—	200	20	—	200	Mbps
		×1	10	—	200	10	—	200	10	—	200	Mbps
t _{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS ⁽⁶⁷⁾	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
t _{x jitter} ⁽⁶⁸⁾	Output jitter	—	—	—	1,000	—	—	1,000	—	—	1,000	ps
t _{RISE}	Rise time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{FALL}	Fall time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

⁽⁶⁷⁾ TCCS specifications apply to I/O banks from the same side only.

⁽⁶⁸⁾ TX jitter is the jitter induced from core noise and I/O switching noise.



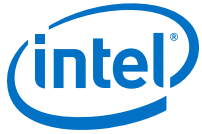
Dual Supply Devices Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications

Table 44. Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

Emulated **LVDS_E_3R**, **SLVS**, and **Sub-LVDS** transmitters are supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	-I6, -A6, -C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{HCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	—	300	5	—	275	5	—	275	MHz
		×8	5	—	300	5	—	275	5	—	275	MHz
		×7	5	—	300	5	—	275	5	—	275	MHz
		×4	5	—	300	5	—	275	5	—	275	MHz
		×2	5	—	300	5	—	275	5	—	275	MHz
		×1	5	—	300	5	—	275	5	—	275	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	—	600	100	—	550	100	—	550	Mbps
		×8	80	—	600	80	—	550	80	—	550	Mbps
		×7	70	—	600	70	—	550	70	—	550	Mbps
		×4	40	—	600	40	—	550	40	—	550	Mbps
		×2	20	—	600	20	—	550	20	—	550	Mbps
		×1	10	—	300	10	—	275	10	—	275	Mbps
f _{HCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	—	150	5	—	150	5	—	150	MHz
		×8	5	—	150	5	—	150	5	—	150	MHz
		×7	5	—	150	5	—	150	5	—	150	MHz
		×4	5	—	150	5	—	150	5	—	150	MHz
		×2	5	—	150	5	—	150	5	—	150	MHz
		×1	5	—	300	5	—	300	5	—	300	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	—	300	100	—	300	100	—	300	Mbps
		×8	80	—	300	80	—	300	80	—	300	Mbps

continued...



Symbol	Parameter	Mode	-C7, -I7		-A7		-C8		Unit
			Min	Max	Min	Max	Min	Max	
		×8	80	200	80	200	80	200	Mbps
		×7	70	200	70	200	70	200	Mbps
		×4	40	200	40	200	40	200	Mbps
		×2	20	200	20	200	20	200	Mbps
		×1	10	200	10	200	10	200	Mbps
SW	Sampling window (high-speed I/O performance pin)	—	—	910	—	910	—	910	ps
	Sampling window (low-speed I/O performance pin)	—	—	1,110	—	1,110	—	1,110	ps
$t_{x \text{ jitter}}^{(71)}$	Input jitter	—	—	1,000	—	1,000	—	1,000	ps
t_{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	1	—	1	—	1	ms

Dual Supply Devices LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications

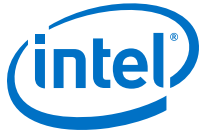
Table 46. LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices

LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS receivers are supported at all banks.

Symbol	Parameter	Mode	-I6, -A6, -C7, -I7		-A7		-C8		Unit
			Min	Max	Min	Max	Min	Max	
f_{HCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	350	5	320	5	320	MHz
		×8	5	360	5	320	5	320	MHz
		×7	5	350	5	320	5	320	MHz
		×4	5	360	5	320	5	320	MHz

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⁽⁷¹⁾ TX jitter is the jitter induced from core noise and I/O switching noise.



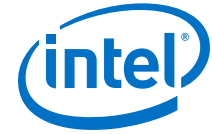
Device	CFM Data Size (bits)	
	Without Memory Initialization	With Memory Initialization
10M25	4,140,000	4,780,000
10M40	7,840,000	9,670,000
10M50	7,840,000	9,670,000

Internal Configuration Time

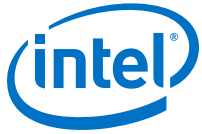
The internal configuration time measurement is from the rising edge of nSTATUS signal to the rising edge of CONF_DONE signal.

Table 53. Internal Configuration Time for Intel MAX 10 Devices (Uncompressed .rbf)

Device	Internal Configuration Time (ms)							
	Unencrypted				Encrypted			
	Without Memory Initialization		With Memory Initialization		Without Memory Initialization		With Memory Initialization	
	Min	Max	Min	Max	Min	Max	Min	Max
10M02	0.3	1.7	—	—	1.7	5.4	—	—
10M04	0.6	2.7	1.0	3.4	5.0	15.0	6.8	19.6
10M08	0.6	2.7	1.0	3.4	5.0	15.0	6.8	19.6
10M16	1.1	3.7	1.4	4.5	9.3	25.3	11.7	31.5
10M25	1.0	3.7	1.3	4.4	14.0	38.1	16.9	45.7
10M40	2.6	6.9	3.2	9.8	41.5	112.1	51.7	139.6
10M50	2.6	6.9	3.2	9.8	41.5	112.1	51.7	139.6



Date	Version	Changes
December 2017	2017.12.15	- Removed the units for "Input resistance" and "Input capacitance" parameters in the following tables: - ADC Performance Specifications for Intel MAX 10 Single Supply Devices - ADC Performance Specifications for Intel MAX 10 Dual Supply Devices - Removed the specification with memory initialization for 10M02 device in the <i>Uncompressed .rbf Sizes for Intel MAX 10 Devices</i> table.
June 2017	2017.06.16	- Added notes for T_J for Industrial and Automotive devices in Recommended Operating Conditions for Intel MAX 10 Devices table. - Updated the parameter in Internal Weak Pull-Up Resistor for Intel MAX 10 Devices table. - Changed "Performance" to "Frequency" in UFM Performance Specifications for Intel MAX 10 Devices table. - Removed PowerPlay text from tool name.
February 2017	2017.02.21	Rebranded as Intel.
October 2016	2016.10.31	- Updated the note to the Intel MAX 10 Device Grades and Speed Grades Supported table. - Updated the Memory Standards Supported by the Soft Memory Controller for Intel MAX 10 Devices table.
May 2016	2016.05.02	- Updated t_{RAMP} specifications in Recommended Operating Conditions for Intel MAX 10 Devices table. - Removed standard POR and fast POR specifications. - Updated maximum value from 3 ms to 10 ms and added a not for the minimum value. - Added Supply Current and Power Consumption section. - Added the following tables: - Memory Standards Supported by the Soft Memory Controller for Intel MAX 10 Devices - Internal Configuration Timing Parameter for Intel MAX 10 Devices - Removed POR Delay Specifications for Intel MAX 10 Devices table. - Updated the description in the Internal Configuration Time section. - Updated the following tables: - Internal Configuration Time for Intel MAX 10 Devices (Uncompressed .rbf) - Internal Configuration Time for Intel MAX 10 Devices (Compressed .rbf)
continued...		



Date	Version	Changes
May 2015	2015.05.04	• Updated a note to V_{CCIO} for both single supply and dual supply power supplies recommended operating conditions tables. Note updated: V_{CCIO} for all I/O banks must be powered up during user mode because V_{CCIO} I/O banks are used for the ADC and I/O functionalities. • Updated Example for OCT Resistance Calculation after Calibration at Device Power-Up. • Removed a note to BLVDS in Differential I/O Standards Specifications for Intel MAX 10 Devices table. BLVDS is now supported in Intel MAX 10 single supply devices. Note removed: BLVDS TX is not supported in single supply devices. • Updated ADC Performance Specifications for both single supply and dual supply devices. — Changed the symbol for Operating junction temperature range parameter from T_A to T_J. — Edited sampling rate maximum value from 1000 kSPS to 1 MSPS. — Added a note to analog input voltage parameter. — Removed input frequency, f_{IN} specification. — Updated the condition for DNL specification: External V_{REF}, no missing code. Added DNL specification for condition: Internal V_{REF}, no missing code. — Added notes to AC accuracy specifications that the value with prescaler enabled is 6dB less than the specification. — Added a note to On-Chip Temperature Sensor (absolute accuracy) parameter about the averaging calculation. • Updated ADC Performance Specifications for Intel MAX 10 Single Supply Devices table. — Added condition for On-Chip Temperature Sensor (absolute accuracy) parameter: with 64 samples averaging. • Updated ADC Performance Specifications for Intel MAX 10 Dual Supply Devices table. — Updated Digital Supply Voltage minimum value from 1.14 V to 1.15 V and maximum value from 1.26 V to 1.25 V. • Updated f_{HCLK} and HSIODR specifications for –A7 speed grade in the following tables: — True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True LVDS Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices — True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — Emulated LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices — Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — LVDS Receiver Timing Specifications for Intel MAX 10 Single Supply Devices — LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices

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