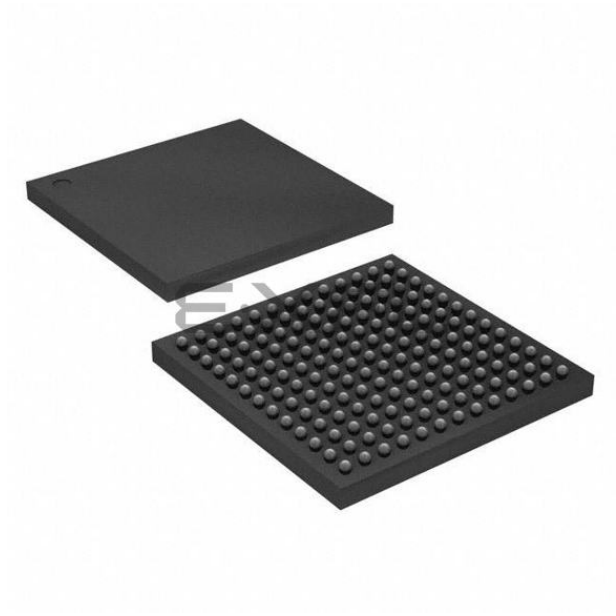

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 1000 |
| Number of Logic Elements/Cells | 16000 |
| Total RAM Bits | 562176 |
| Number of I/O | 130 |
| Number of Gates | - |
| Voltage - Supply | 2.85V ~ 3.465V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 169-LFBGA |
| Supplier Device Package | 169-UBGA (11x11) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/10m16scu169i7g |

# Intel® MAX® 10 FPGA Device Datasheet

This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and timing for Intel MAX® 10 devices.

**Table 1. Intel MAX 10 Device Grades and Speed Grades Supported**

| Device Grade | Speed Grade Supported |
|---|---|
| Commercial | • –C7<br>• –C8 (slowest) |
| Industrial | • –I6 (fastest)<br>• –I7 |
| Automotive | • –A6<br>• –A7 |

*Note:* The –I6 and –A6 speed grades of the Intel MAX 10 FPGA devices are not available by default in the Intel Quartus® Prime software. Contact your local Intel sales representatives for support.

### Related Information

Device Ordering Information, Intel MAX 10 FPGA Device Overview
Provides more information about the densities and packages of devices in the Intel MAX 10.

## Electrical Characteristics

The following sections describe the operating conditions and power consumption of Intel MAX 10 devices.

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CCD\_PLL}$ | Supply voltage for PLL regulator (digital) | –0.5 | 1.63 | V |
| $V_{CCA\_ADC}$ | Supply voltage for ADC analog block | –0.5 | 3.41 | V |
| $V_{CCINT}$ | Supply voltage for ADC digital block | –0.5 | 1.63 | V |

## Absolute Maximum Ratings

### Table 4. Absolute Maximum Ratings for Intel MAX 10 Devices

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_I$ | DC input voltage | –0.5 | 4.12 | V |
| $I_{OUT}$ | DC output current per pin | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | –65 | 150 | °C |
| $T_J$ | Operating junction temperature | –40 | 125 | °C |

## Maximum Allowed Overshoot During Transitions over a 11.4-Year Time Frame

During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 4.17 V can only be at 4.17 V for ~11.7% over the lifetime of the device; for a device lifetime of 11.4 years, this amounts to 1.33 years.

### Table 5. Maximum Allowed Overshoot During Transitions over a 11.4-Year Time Frame for Intel MAX 10 Devices

| Condition (V) | Overshoot Duration as % of High Time | Unit |
|---|---|---|
| 4.12 | 100.0 | % |
| 4.17 | 11.7 | % |
| 4.22 | 7.1 | % |
| 4.27 | 4.3 | % |

*continued...*

**Table 15. OCT Variation after Calibration at Device Power-Up for Intel MAX 10 Devices**

This table lists the change percentage of the OCT resistance with voltage and temperature.

| Description | Nominal Voltage | dR/dT (%/°C) | dR/dV (%/mV) |
|---|---|---|---|
| OCT variation after calibration at device power-up | 3.00 | 0.25 | –0.027 |
| | 2.50 | 0.245 | –0.04 |
| | 1.80 | 0.242 | –0.079 |
| | 1.50 | 0.235 | –0.125 |
| | 1.35 | 0.229 | –0.16 |
| | 1.20 | 0.197 | –0.208 |

**Figure 1. Equation for OCT Resistance after Calibration at Device Power-Up**

$$\Delta R_V = (V_2 - V_1) \times 1000 \times dR/dV$$

$$\Delta R_T = (T_2 - T_1) \times dR/dT$$

$$\text{For } \Delta R_X < 0; MF_X = 1/(|\Delta R_X|/100 + 1)$$

$$\text{For } \Delta R_X > 0; MF_X = \Delta R_X/100 + 1$$

$$MF = MF_V \times MF_T$$

$$R_{final} = R_{initial} \times MF$$

The definitions for equation are as follows:

- $T_1$ is the initial temperature.
- $T_2$ is the final temperature.
- MF is multiplication factor.
- $R_{initial}$ is initial resistance.
- $R_{final}$ is final resistance.

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{VCO}$ (29) | PLL internal voltage-controlled oscillator (VCO) operating range | — | 600 | — | 1300 | MHz |
| $f_{INDUTY}$ | Input clock duty cycle | — | 40 | — | 60 | % |
| $t_{INJITTER\_CCJ}$ (30) | Input clock cycle-to-cycle jitter | $F_{INPFD}$ ≥ 100 MHz | — | — | 0.15 | UI |
| | | $F_{INPFD}$ < 100 MHz | — | — | ±750 | ps |
| $f_{OUT\_EXT}$ (28) | PLL output frequency for external clock output | — | — | — | 472.5 | MHz |
| $f_{OUT}$ | PLL output frequency to global clock | –6 speed grade | — | — | 472.5 | MHz |
| | | –7 speed grade | — | — | 450 | MHz |
| | | –8 speed grade | — | — | 402.5 | MHz |
| $t_{OUTDUTY}$ | Duty cycle for external clock output | Duty cycle set to 50% | 45 | 50 | 55 | % |
| $t_{LOCK}$ | Time required to lock from end of device configuration | — | — | — | 1 | ms |
| $t_{DLOCK}$ | Time required to lock dynamically | After switchover, reconfiguring any non-post-scale counters or delays, or when `areset` is deasserted | — | — | 1 | ms |
| $t_{OUTJITTER\_PERIOD\_IO}$ (31) | Regular I/O period jitter | $F_{OUT}$ ≥ 100 MHz | — | — | 650 | ps |
| | | $F_{OUT}$ < 100 MHz | — | — | 75 | mUI |
| $t_{OUTJITTER\_CCJ\_IO}$ (31) | Regular I/O cycle-to-cycle jitter | $F_{OUT}$ ≥ 100 MHz | — | — | 650 | ps |
| | | $F_{OUT}$ < 100 MHz | — | — | 75 | mUI |

***continued...***

(29) The VCO frequency reported by the Intel Quartus Prime software in the PLL summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the $f_{VCO}$ specification.

(30) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source, which is less than 200 ps.

(31) Peak-to-peak jitter with a probability level of $10^{-12}$ (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied.

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{PLL\_PSERR}$ | Accuracy of PLL phase shift | — | — | — | ±50 | ps |
| $t_{ARESET}$ | Minimum pulse width on areset signal. | — | 10 | — | — | ns |
| $t_{CONFIGPLL}$ | Time required to reconfigure scan chains for PLLs | — | — | 3.5 (32) | — | SCANCLK cycles |
| $f_{SCANCLK}$ | scanclk frequency | — | — | — | 100 | MHz |

## Table 28. PLL Specifications for Intel MAX 10 Single Supply Devices

For V36 package, the PLL specification is based on single supply devices.

| Symbol | Parameter | Condition | Max | Unit |
|---|---|---|---|---|
| $t_{OUTJITTER\_PERIOD\_DEDCLK}$ (31) | Dedicated clock output period jitter | $F_{OUT} \geq 100$ MHz | 660 | ps |
| | | $F_{OUT} < 100$ MHz | 66 | mUI |
| $t_{OUTJITTER\_CCJ\_DEDCLK}$ (31) | Dedicated clock output cycle-to-cycle jitter | $F_{OUT} \geq 100$ MHz | 660 | ps |
| | | $F_{OUT} < 100$ MHz | 66 | mUI |

## Table 29. PLL Specifications for Intel MAX 10 Dual Supply Devices

| Symbol | Parameter | Condition | Max | Unit |
|---|---|---|---|---|
| $t_{OUTJITTER\_PERIOD\_DEDCLK}$ (31) | Dedicated clock output period jitter | $F_{OUT} \geq 100$ MHz | 300 | ps |
| | | $F_{OUT} < 100$ MHz | 30 | mUI |
| $t_{OUTJITTER\_CCJ\_DEDCLK}$ (31) | Dedicated clock output cycle-to-cycle jitter | $F_{OUT} \geq 100$ MHz | 300 | ps |
| | | $F_{OUT} < 100$ MHz | 30 | mUI |

(32) With 100 MHz scanclk frequency.

## Internal Oscillator Specifications

### Table 32. Internal Oscillator Frequencies for Intel MAX 10 Devices

You can access to the internal oscillator frequencies in this table. The duty cycle of internal oscillator is approximately 45%–55%.

| Device | Frequency | | | Unit |
|---|---|---|---|---|
| | Minimum | Typical | Maximum | |
| 10M02 | 55 | 82 | 116 | MHz |
| 10M04 | | | | |
| 10M08 | | | | |
| 10M16 | | | | |
| 10M25 | | | | |
| 10M40 | 35 | 52 | 77 | MHz |
| 10M50 | | | | |

## UFM Performance Specifications

### Table 33. UFM Performance Specifications for Intel MAX 10 Devices

| Block | Mode | Interface | Device | Frequency | | Unit |
|---|---|---|---|---|---|---|
| | | | | Minimum | Maximum | |
| UFM | Avalon®-MM slave | Parallel (33) | 10M02 (34) | 3.43 | 7.25 | MHz |
| | | | 10M04, 10M08, 10M16, 10M25, 10M40, 10M50 | 5 | 116 | MHz |
| | | Serial (34) | 10M02, 10M04, 10M08, 10M16, 10M25 | 3.43 | 7.25 | MHz |
| | | | 10M40, 10M50 | 2.18 | 4.81 | MHz |

(33) Clock source is derived from user, except for 10M02 device.

(34) Clock source is derived from 1/16 of the frequency of the internal oscillator.

| Parameter | | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| | Integral non linearity | INL | — | –2 | — | 2 | LSB |
| AC Accuracy | Total harmonic distortion | THD | $F_{IN}$ = 50 kHz, $F_S$ = 1 MHz, PLL | –65 (37) | — | — | dB |
| | Signal-to-noise ratio | SNR | $F_{IN}$ = 50 kHz, $F_S$ = 1 MHz, PLL | 54 (38) | — | — | dB |
| | Signal-to-noise and distortion | SINAD | $F_{IN}$ = 50 kHz, $F_S$ = 1 MHz, PLL | 53 (39) | — | — | dB |
| On-Chip Temperature Sensor | Temperature sampling rate | $T_S$ | — | — | — | 50 | kSPS |
| | Absolute accuracy | — | –40 to 125°C, with 64 samples averaging (40) | — | — | ±10 | °C |
| Conversion Rate (41) | Conversion time | — | Single measurement | — | — | 1 | Cycle |
| | | | Continuous measurement | — | — | 1 | Cycle |
| | | | Temperature measurement | — | — | 1 | Cycle |

**Related Information**

SPICE Models for Intel FPGAs

(37) THD with prescalar enabled is 6dB less than the specification.

(38) SNR with prescalar enabled is 6dB less than the specification.

(39) SINAD with prescalar enabled is 6dB less than the specification.

(40) For the Intel Quartus Prime software version 15.0 and later, Modular ADC Core Intel FPGA IP and Modular Dual ADC Core Intel FPGA IP cores handle the 64 samples averaging. For the Intel Quartus Prime software versions prior to 14.1, you need to implement your own averaging calculation.

(41) For more detailed description, refer to the Timing section in the *Intel MAX 10 Analog-to-Digital Converter User Guide*.

## Dual Supply Devices ADC Performance Specifications

### Table 35. ADC Performance Specifications for Intel MAX 10 Dual Supply Devices

| Parameter | | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| ADC resolution | | — | — | — | — | 12 | bits |
| Analog supply voltage | | $V_{CCA\_ADC}$ | — | 2.375 | 2.5 | 2.625 | V |
| Digital supply voltage | | $V_{CCINT}$ | — | 1.15 | 1.2 | 1.25 | V |
| External reference voltage | | $V_{REF}$ | — | $V_{CCA\_ADC}$ – 0.5 | — | $V_{CCA\_ADC}$ | V |
| Sampling rate | | $F_S$ | Accumulative sampling rate | — | — | 1 | MSPS |
| Operating junction temperature range | | $T_J$ | — | –40 | 25 | 125 | °C |
| Analog input voltage | | $V_{IN}$ | Prescalar disabled | 0 | — | $V_{REF}$ | V |
| | | | Prescalar enabled (42) | 0 | — | 3 | V |
| Analog supply current (DC) | | $I_{ACC\_ADC}$ | Average current | — | 275 | 450 | µA |
| Digital supply current (DC) | | $I_{CCINT}$ | Average current | — | 65 | 150 | µA |
| Input resistance | | $R_{IN}$ | — | — | (43) | — | — |
| Input capacitance | | $C_{IN}$ | — | — | (43) | — | — |
| DC Accuracy | Offset error and drift | $E_{offset}$ | Prescalar disabled | –0.2 | — | 0.2 | %FS |
| | | | Prescalar enabled | –0.5 | — | 0.5 | %FS |
| | Gain error and drift | $E_{gain}$ | Prescalar disabled | –0.5 | — | 0.5 | %FS |
| | | | Prescalar enabled | –0.75 | — | 0.75 | %FS |
| | Differential non linearity | DNL | External $V_{REF}$, no missing code | –0.9 | — | 0.9 | LSB |

***continued...***

(42) Prescalar function divides the analog input voltage by half. The analog input handles up to 3 V input for the Intel MAX 10 dual supply devices.

(43) Download the SPICE models for simulation.

| Parameter | | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| | | | Internal $V_{REF}$, no missing code | –1 | — | 1.7 | LSB |
| | Integral non linearity | INL | — | –2 | — | 2 | LSB |
| AC Accuracy | Total harmonic distortion | THD | $F_{IN}$ = 50 kHz, $F_S$ = 1 MHz, PLL | –70 (44)(45)(46) | — | — | dB |
| | Signal-to-noise ratio | SNR | $F_{IN}$ = 50 kHz, $F_S$ = 1 MHz, PLL | 62 (47)(48)(46) | — | — | dB |
| | Signal-to-noise and distortion | SINAD | $F_{IN}$ = 50 kHz, $F_S$ = 1 MHz, PLL | 61.5 (49)(50)(46) | — | — | dB |
| On-Chip Temperature Sensor | Temperature sampling rate | $T_S$ | — | — | — | 50 | kSPS |
| | Absolute accuracy | — | –40 to 125°C, with 64 samples averaging (51) | — | — | ±5 | °C |

*continued...*

(44) Total harmonic distortion is –65 dB for dual function pin.

(45) THD with prescalar enabled is 6dB less than the specification.

(46) When using internal $V_{REF}$, THD = 66 dB, SNR = 58 dB and SINAD = 57.5 dB for dedicated ADC input channels.

(47) Signal-to-noise ratio is 54 dB for dual function pin.

(48) SNR with prescalar enabled is 6dB less than the specification.

(49) Signal-to-noise and distortion is 53 dB for dual function pin.

(50) SINAD with prescalar enabled is 6dB less than the specification.

(51) For the Intel Quartus Prime software version 15.0 and later, Modular ADC Core and Modular Dual ADC Core IP cores handle the 64 samples averaging. For the Intel Quartus Prime software versions prior to 14.1, you need to implement your own averaging calculation.

| Parameter | | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Conversion Rate [52] | Conversion time | — | Single measurement | — | — | 1 | Cycle |
| | | | Continuous measurement | — | — | 1 | Cycle |
| | | | Temperature measurement | — | — | 1 | Cycle |

**Related Information**

SPICE Models for Intel FPGAs

## Periphery Performance Specifications

This section describes the periphery performance, high-speed I/O, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

## High-Speed I/O Specifications

For more information about the high-speed and low-speed I/O performance pins, refer to the respective device pin-out files.

**Related Information**

Documentation: Pin-Out Files for Intel FPGAs

[52] For more detailed description, refer to the Timing section in the *Intel MAX 10 Analog-to-Digital Converter User Guide*.

| Symbol | Parameter | Mode | –I6, –A6, –C7, –I7 | | | –A7 | | | –C8 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| | | ×4 | 40 | — | 300 | 40 | — | 300 | 40 | — | 300 | Mbps |
| | | ×2 | 20 | — | 300 | 20 | — | 300 | 20 | — | 300 | Mbps |
| | | ×1 | 10 | — | 300 | 10 | — | 300 | 10 | — | 300 | Mbps |
| $t_{DUTY}$ | Duty cycle on transmitter output clock | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| TCCS[53] | Transmitter channel-to-channel skew | — | — | — | 300 | — | — | 300 | — | — | 300 | ps |
| $t_{x\ Jitter}$[54] | Output jitter (high-speed I/O performance pin) | — | — | — | 425 | — | — | 425 | — | — | 425 | ps |
| | Output jitter (low-speed I/O performance pin) | — | — | — | 470 | — | — | 470 | — | — | 470 | ps |
| $t_{RISE}$ | Rise time | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{FALL}$ | Fall time | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{LOCK}$ | Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration | — | — | — | 1 | — | — | 1 | — | — | 1 | ms |

(53) TCCS specifications apply to I/O banks from the same side only.

(54) TX jitter is the jitter induced from core noise and I/O switching noise.

## True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications

### Single Supply Devices True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications

### Table 37. True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices

True **RSDS** transmitter is only supported at bottom I/O banks. Emulated **RSDS** transmitter is supported at the output pin of all I/O banks.

| Symbol | Parameter | Mode | –I6, –A6, –C7, –I7 | | | –A7 | | | –C8 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK}$ | Input clock frequency (high-speed I/O performance pin) | ×10 | 5 | — | 50 | 5 | — | 50 | 5 | — | 50 | MHz |
| | | ×8 | 5 | — | 50 | 5 | — | 50 | 5 | — | 50 | MHz |
| | | ×7 | 5 | — | 50 | 5 | — | 50 | 5 | — | 50 | MHz |
| | | ×4 | 5 | — | 50 | 5 | — | 50 | 5 | — | 50 | MHz |
| | | ×2 | 5 | — | 50 | 5 | — | 50 | 5 | — | 50 | MHz |
| | | ×1 | 5 | — | 100 | 5 | — | 100 | 5 | — | 100 | MHz |
| HSIODR | Data rate (high-speed I/O performance pin) | ×10 | 100 | — | 100 | 100 | — | 100 | 100 | — | 100 | Mbps |
| | | ×8 | 80 | — | 100 | 80 | — | 100 | 80 | — | 100 | Mbps |
| | | ×7 | 70 | — | 100 | 70 | — | 100 | 70 | — | 100 | Mbps |
| | | ×4 | 40 | — | 100 | 40 | — | 100 | 40 | — | 100 | Mbps |
| | | ×2 | 20 | — | 100 | 20 | — | 100 | 20 | — | 100 | Mbps |
| | | ×1 | 10 | — | 100 | 10 | — | 100 | 10 | — | 100 | Mbps |
| $f_{HSCLK}$ | Input clock frequency (low-speed I/O performance pin) | ×10 | 5 | — | 50 | 5 | — | 50 | 5 | — | 50 | MHz |
| | | ×8 | 5 | — | 50 | 5 | — | 50 | 5 | — | 50 | MHz |
| | | ×7 | 5 | — | 50 | 5 | — | 50 | 5 | — | 50 | MHz |
| | | ×4 | 5 | — | 50 | 5 | — | 50 | 5 | — | 50 | MHz |
| | | ×2 | 5 | — | 50 | 5 | — | 50 | 5 | — | 50 | MHz |
| | | ×1 | 5 | — | 100 | 5 | — | 100 | 5 | — | 100 | MHz |
| HSIODR | Data rate (low-speed I/O performance pin) | ×10 | 100 | — | 100 | 100 | — | 100 | 100 | — | 100 | Mbps |

*continued...*

| Symbol | Parameter | Mode | –I6, –A6, –C7, –I7 | | | –A7 | | | –C8 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| | | ×7 | 70 | — | 300 | 70 | — | 300 | 70 | — | 300 | Mbps |
| | | ×4 | 40 | — | 300 | 40 | — | 300 | 40 | — | 300 | Mbps |
| | | ×2 | 20 | — | 300 | 20 | — | 300 | 20 | — | 300 | Mbps |
| | | ×1 | 10 | — | 300 | 10 | — | 300 | 10 | — | 300 | Mbps |
| $t_{DUTY}$ | Duty cycle on transmitter output clock | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| TCCS[61] | Transmitter channel-to-channel skew | — | — | — | 300 | — | — | 300 | — | — | 300 | ps |
| $t_{x\ Jitter}$[62] | Output jitter (high-speed I/O performance pin) | — | — | — | 425 | — | — | 425 | — | — | 425 | ps |
| | Output jitter (low-speed I/O performance pin) | — | — | — | 470 | — | — | 470 | — | — | 470 | ps |
| $t_{RISE}$ | Rise time | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{FALL}$ | Fall time | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{LOCK}$ | Time required for the PLL to lock, after `CONF_DONE` signal goes high, indicating the completion of device configuration | — | — | — | 1 | — | — | 1 | — | — | 1 | ms |

(61) TCCS specifications apply to I/O banks from the same side only.

(62) TX jitter is the jitter induced from core noise and I/O switching noise.

| Symbol | Parameter | Mode | –I6 | | | –A6, –C7, –I7 | | | –A7 | | | –C8 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| | | ×1 | 10 | — | 360 | 10 | — | 350 | 10 | — | 320 | 10 | — | 320 | Mbps |
| $t_{DUTY}$ | Duty cycle on transmitter output clock | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| TCCS(65) | Transmitter channel-to-channel skew | — | — | — | 300 | — | — | 300 | — | — | 300 | — | — | 300 | ps |
| $t_{x\ Jitter}$(66) | Output jitter | — | — | — | 380 | — | — | 380 | — | — | 380 | — | — | 380 | ps |
| $t_{RISE}$ | Rise time | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{FALL}$ | Fall time | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{LOCK}$ | Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration | — | — | — | 1 | — | — | 1 | — | — | 1 | — | — | 1 | ms |

(65) TCCS specifications apply to I/O banks from the same side only.

(66) TX jitter is the jitter induced from core noise and I/O switching noise.

## LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications

### Single Supply Devices LVDS Receiver Timing Specifications

### Table 45. LVDS Receiver Timing Specifications for Intel MAX 10 Single Supply Devices

**LVDS** receivers are supported at all banks.

| Symbol | Parameter | Mode | –C7, –I7 | | –A7 | | –C8 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| $f_{HSCLK}$ | Input clock frequency (high-speed I/O performance pin) | ×10 | 5 | 145 | 5 | 100 | 5 | 100 | MHz |
| | | ×8 | 5 | 145 | 5 | 100 | 5 | 100 | MHz |
| | | ×7 | 5 | 145 | 5 | 100 | 5 | 100 | MHz |
| | | ×4 | 5 | 145 | 5 | 100 | 5 | 100 | MHz |
| | | ×2 | 5 | 145 | 5 | 100 | 5 | 100 | MHz |
| | | ×1 | 5 | 290 | 5 | 200 | 5 | 200 | MHz |
| HSIODR | Data rate (high-speed I/O performance pin) | ×10 | 100 | 290 | 100 | 200 | 100 | 200 | Mbps |
| | | ×8 | 80 | 290 | 80 | 200 | 80 | 200 | Mbps |
| | | ×7 | 70 | 290 | 70 | 200 | 70 | 200 | Mbps |
| | | ×4 | 40 | 290 | 40 | 200 | 40 | 200 | Mbps |
| | | ×2 | 20 | 290 | 20 | 200 | 20 | 200 | Mbps |
| | | ×1 | 10 | 290 | 10 | 200 | 10 | 200 | Mbps |
| $f_{HSCLK}$ | Input clock frequency (low-speed I/O performance pin) | ×10 | 5 | 100 | 5 | 100 | 5 | 100 | MHz |
| | | ×8 | 5 | 100 | 5 | 100 | 5 | 100 | MHz |
| | | ×7 | 5 | 100 | 5 | 100 | 5 | 100 | MHz |
| | | ×4 | 5 | 100 | 5 | 100 | 5 | 100 | MHz |
| | | ×2 | 5 | 100 | 5 | 100 | 5 | 100 | MHz |
| | | ×1 | 5 | 200 | 5 | 200 | 5 | 200 | MHz |
| HSIODR | Data rate (low-speed I/O performance pin) | ×10 | 100 | 200 | 100 | 200 | 100 | 200 | Mbps |

*continued...*

### Table 54. Internal Configuration Time for Intel MAX 10 Devices (Compressed .rbf)

Compression ratio depends on design complexity. The minimum value is based on the best case (25% of original `.rbf` sizes) and the maximum value is based on the typical case (70% of original `.rbf` sizes).

| Device | Internal Configuration Time (ms) | | | |
|---|---|---|---|---|
| | Unencrypted/Encrypted | | | |
| | Without Memory Initialization | | With Memory Initialization | |
| | Min | Max | Min | Max |
| 10M02 | 0.3 | 5.2 | — | — |
| 10M04 | 0.6 | 10.7 | 1.0 | 13.9 |
| 10M08 | 0.6 | 10.7 | 1.0 | 13.9 |
| 10M16 | 1.1 | 17.9 | 1.4 | 22.3 |
| 10M25 | 1.1 | 26.9 | 1.4 | 32.2 |
| 10M40 | 2.6 | 66.1 | 3.2 | 82.2 |
| 10M50 | 2.6 | 66.1 | 3.2 | 82.2 |

## Internal Configuration Timing Parameter

### Table 55. Internal Configuration Timing Parameter for Intel MAX 10 Devices

| Symbol | Parameter | Device | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| $t_{CD2UM}$ | `CONF_DONE` high to user mode | 10M02, 10M04, 10M08, 10M16, 10M25 | 182.8 | 385.5 | µs |
| | | 10M40, 10M50 | 275.3 | 605.7 | µs |

# I/O Timing

The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

The Intel Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specific device and design after you complete place-and-route.

# Programmable IOE Delay for Column Pins

## Table 58. IOE Programmable Delay on Column Pins for Intel MAX 10 Devices

The incremental values for the settings are generally linear. For exact values of each setting, refer to the **Assignment Name** column in the latest version of the Intel Quartus Prime software.

The minimum and maximum offset timing numbers are in reference to setting '0' as available in the Intel Quartus Prime software.

| Parameter | Paths Affected | Number of Settings | Minimum Offset | Maximum Offset | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Fast Corner | | Slow Corner | | | | | |
| | | | | –I7 | –C8 | –A6 | –C7 | –C8 | –I7 | –A7 | |
| Input delay from pin to internal cells | Pad to I/O dataout to core | 7 | 0 | 0.81 | 0.868 | 1.823 | 1.802 | 1.864 | 1.862 | 1.912 | ns |
| Input delay from pin to input register | Pad to I/O input register | 8 | 0 | 0.914 | 0.981 | 2.06 | 2.032 | 2.101 | 2.102 | 2.161 | ns |
| Delay from output register to output pin | I/O output register to pad | 2 | 0 | 0.435 | 0.466 | 0.971 | 0.97 | 1.013 | 1.001 | 1.028 | ns |

| Date | Version | Changes |
|---|---|---|
| January 2016 | 2016.01.22 | • Added description about automotive temperature devices in the Programming/Erasure Specifications table.<br>• Changed the pin capacitance to maximum values.<br>• Updated maximum TCCS specifications from 410 ps to 300 ps in the following tables:<br>— True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— Emulated RSDS_E_1R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— True LVDS Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices<br>— True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— Emulated LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices<br>— Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>• Added new table: True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices.<br>• Updated maximum $f_{HSCLK}$ and HSIODR specifications for –A6, –C7, and –I7 speed grades in True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices table.<br>• Updated SW specifications in the following tables:<br>— LVDS Receiver Timing Specifications for Intel MAX 10 Single Supply Devices<br>— LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices<br>• Updated maximum $f_{HSCLK}$ and HSIODR (high-speed I/O performance pin) specifications for –I6, –A6, –C7, –I7 speed grades in LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices table.<br>• Removed Internal Configuration Time information in the Uncompressed .rbf Sizes for Intel MAX 10 Devices table.<br>• Added Internal Configuration Time tables for uncompressed `.rbf` files and compressed `.rbf` files.<br>• Removed Preliminary tags for all tables. |
| November 2015 | 2015.11.02 | • Added description to *Maximum Allowed Overshoot During Transitions over a 11.4-Year Time Frame* topic.<br>• Added ADC_VREF Pin Leakage Current for Intel MAX 10 Devices table.<br>• Updated the condition for "Bus-hold high, sustaining current" parameter from "$V_{IN} < V_{IL}$ (minimum)" to "$V_{IN} < V_{IH}$ (minimum)" in Bus Hold Parameters table. |

***continued...***

| Date | Version | Changes |
|---|---|---|
| | | • Updated TCCS specifications in the following tables:<br>— True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— Emulated RSDS_E_1R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— True LVDS Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices<br>— True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— Emulated LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices<br>— Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>• Updated $t_{x\ Jitter}$ specifications in the following tables:<br>— True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— Emulated RSDS_E_1R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>• Updated SW specifications in LVDS Receiver Timing Specifications for Intel MAX 10 Single Supply Devices table.<br>• Added a note to $t_{x\ Jitter}$ for all LVDS tables. Note: TX jitter is the jitter induced from core noise and I/O switching noise.<br>• Updated the description for $t_{LOCK}$ for all LVDS tables: Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration.<br>• Updated Memory Output Clock Jitter Specifications section.<br>— Updated maximum external memory interfaces frequency from 300 MHz to 303 MHz.<br>— Updated PLL output routing from global clock network to PHY clock network.<br>• Added I/O Timing for Intel MAX 10 Devices table.<br>• Added $V_{HYS}$ in the Glossary table. |
| January 2015 | 2015.01.23 | • Removed a note to $V_{CCA}$ in Power Supplies Recommended Operating Conditions for Intel MAX 10 Dual Supply Devices table. This note is not valid: All $V_{CCA}$ pins must be connected together for EQFP package.<br>• Corrected the maximum value for $t_{OUTJITTER\_CCJ\_IO}$ ($F_{OUT} \geq 100$ MHz) from 60 ps to 650 ps in PLL Specifications for Intel MAX 10 Devices table. |
| December 2014 | 2014.12.15 | • Restructured Programming/Erasure Specifications for Intel MAX 10 Devices table to add temperature specifications that affect the data retention duration.<br>• Added statements in the I/O Pin Leakage Current section: Input channel leakage of ADC I/O pins due to hot socket is up to maximum of 1.8 mA. The input channel leakage occurs when the ADC IP core is enabled or disabled. This is applicable to all Intel MAX 10 devices with ADC IP core, which are 10M04, 10M08, 10M16, 10M25, 10M40, and 10M50 devices. The ADC I/O pins are in Bank 1A.<br>• Added a statement in the I/O Standards Specifications section: You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards. |

***continued...***

| Date | Version | Changes |
|---|---|---|
| | | • Updated SSTL-2 Class I and II I/O standard specifications for JEDEC compliance as follows:<br>— VIL(AC) Max: Updated from $V_{REF}$ – 0.35 to $V_{REF}$ – 0.31<br>— VIH(AC) Min: Updated from $V_{REF}$ + 0.35 to $V_{REF}$ + 0.31<br>• Added a note to BLVDS in Differential I/O Standards Specifications for Intel MAX 10 Devices table: BLVDS TX is not supported in single supply devices.<br>• Added a link to MAX 10 High-Speed LVDS I/O User Guide for the list of I/O standards supported in single supply and dual supply devices.<br>• Added a statement in PLL Specifications for Intel MAX 10 Single Supply Device table: For V36 package, the PLL specification is based on single supply devices.<br>• Added Internal Oscillator Specifications from Intel MAX 10 Clocking and PLL User Guide.<br>• Added UFM specifications for serial interface.<br>• Updated total harmonic distortion (THD) specifications as follows:<br>— Single supply devices: Updated from 65 dB to –65 dB<br>— Dual supply devices: Updated from 70 dB to –70 dB (updated from 65 dB to –65 dB for dual function pin)<br>• Added condition for On-Chip Temperature Sensor—Absolute accuracy parameter in ADC Performance Specifications for Intel MAX 10 Dual Supply Devices table. The condition is: with 64 samples averaging.<br>• Updated the description in Periphery Performance Specifications to mention that proper timing closure is required in design.<br>• Updated HSIODR and $f_{HSCLK}$ specifications for x10 and x7 modes in True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices.<br>• Added specifications for low-speed I/O performance pin sampling window in LVDS Receiver Timing Specifications for Intel MAX 10 Single Supply Devices table: Max = 900 ps for –C7, –I7, –A7, and –C8 speed grades.<br>• Added $t_{RU\_nCONFIG}$ and $t_{RU\_nRSTIMER}$ specifications for different devices in Remote System Upgrade Circuitry Timing Specifications for Intel MAX 10 Devices table.<br>• Removed the word "internal oscillator" in User Watchdog Timer Specifications for Intel MAX 10 Devices table to avoid confusion.<br>• Added IOE programmable delay specifications. |
| September 2014 | 2014.09.22 | Initial release. |