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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

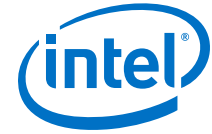
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	2500
Number of Logic Elements/Cells	40000
Total RAM Bits	1290240
Number of I/O	178
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10m40daf256c8g



Symbol	Parameter	Min	Max	Unit
V _{CCD_PLL}	Supply voltage for PLL regulator (digital)	-0.5	1.63	V
V _{CCA_ADC}	Supply voltage for ADC analog block	-0.5	3.41	V
V _{CCINT}	Supply voltage for ADC digital block	-0.5	1.63	V

Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings for Intel MAX 10 Devices

Symbol	Parameter	Min	Max	Unit
V _I	DC input voltage	-0.5	4.12	V
I _{OUT}	DC output current per pin	-25	25	mA
T _{STG}	Storage temperature	-65	150	°C
T _J	Operating junction temperature	-40	125	°C

Maximum Allowed Overshoot During Transitions over a 11.4-Year Time Frame

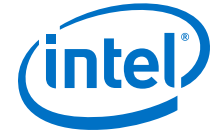
During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 4.17 V can only be at 4.17 V for ~11.7% over the lifetime of the device; for a device lifetime of 11.4 years, this amounts to 1.33 years.

Table 5. Maximum Allowed Overshoot During Transitions over a 11.4-Year Time Frame for Intel MAX 10 Devices

Condition (V)	Overshoot Duration as % of High Time	Unit
4.12	100.0	%
4.17	11.7	%
4.22	7.1	%
4.27	4.3	%
<i>continued...</i>		



Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{CCA}^{(1)}$	Supply voltage for PLL regulator and ADC block (analog)	1.35 V	1.2825	1.35	1.4175	V
		1.2 V	1.14	1.2	1.26	V
		—	2.85/3.135	3.0/3.3	3.15/3.465	V

Dual Supply Devices Power Supplies Recommended Operating Conditions

Table 7. Power Supplies Recommended Operating Conditions for Intel MAX 10 Dual Supply Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CC}	Supply voltage for core and periphery	—	1.15	1.2	1.25	V
$V_{CCIO}^{(3)}$	Supply voltage for input and output buffers	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.35 V	1.2825	1.35	1.4175	V
		1.2 V	1.14	1.2	1.26	V
$V_{CCA}^{(4)}$	Supply voltage for PLL regulator (analog)	—	2.375	2.5	2.625	V
$V_{CCD_PLL}^{(5)}$	Supply voltage for PLL regulator (digital)	—	1.15	1.2	1.25	V
V_{CCA_ADC}	Supply voltage for ADC analog block	—	2.375	2.5	2.625	V
V_{CCINT}	Supply voltage for ADC digital block	—	1.15	1.2	1.25	V

⁽³⁾ V_{CCIO} for all I/O banks must be powered up during user mode because V_{CCIO} I/O banks are used for the ADC and I/O functionalities.

⁽⁴⁾ All V_{CCA} pins must be powered to 2.5 V (even when PLLs are not used), and must be powered up and powered down at the same time.

⁽⁵⁾ V_{CCD_PLL} must always be connected to V_{CC} through a decoupling capacitor and ferrite bead.

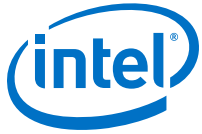


Table 15. OCT Variation after Calibration at Device Power-Up for Intel MAX 10 Devices

This table lists the change percentage of the OCT resistance with voltage and temperature.

Description	Nominal Voltage	dR/dT (%/°C)	dR/dV (%/mV)
OCT variation after calibration at device power-up	3.00	0.25	-0.027
	2.50	0.245	-0.04
	1.80	0.242	-0.079
	1.50	0.235	-0.125
	1.35	0.229	-0.16
	1.20	0.197	-0.208

Figure 1. Equation for OCT Resistance after Calibration at Device Power-Up

$$\Delta R_V = (V_2 - V_1) \times 1000 \times dR/dV$$

$$\Delta R_T = (T_2 - T_1) \times dR/dT$$

$$\text{For } \Delta R_X < 0; MF_X = 1/(|\Delta R_X|/100 + 1)$$

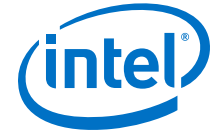
$$\text{For } \Delta R_X > 0; MF_X = \Delta R_X/100 + 1$$

$$MF = MF_V \times MF_T$$

$$R_{final} = R_{initial} \times MF$$

The definitions for equation are as follows:

- T_1 is the initial temperature.
- T_2 is the final temperature.
- MF is multiplication factor.
- $R_{initial}$ is initial resistance.
- R_{final} is final resistance.



Single-Ended I/O Standards Specifications

Table 20. Single-Ended I/O Standards Specifications for Intel MAX 10 Devices

To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the 3.3-V LVTTTL specification (4 mA), you should set the current strength settings to 4 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3 V LVTTTL	3.135	3.3	3.465	-0.3	0.8	1.7	3.6	0.45	2.4	4	-4
3.3 V LVCMOS	3.135	3.3	3.465	-0.3	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	2	-2
3.0 V LVTTTL	2.85	3	3.15	-0.3	0.8	1.7	$V_{CCIO} + 0.3$	0.45	2.4	4	-4
3.0 V LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	$V_{CCIO} + 0.3$	0.2	$V_{CCIO} - 0.2$	0.1	-0.1
2.5 V LVTTTL and LVCMOS	2.375	2.5	2.625	-0.3	0.7	1.7	$V_{CCIO} + 0.3$	0.4	2	1	-1
1.8 V LVTTTL and LVCMOS	1.71	1.8	1.89	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	2.25	0.45	$V_{CCIO} - 0.45$	2	-2
1.5 V LVCMOS	1.425	1.5	1.575	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2
1.2 V LVCMOS	1.14	1.2	1.26	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2
3.3 V Schmitt Trigger	3.135	3.3	3.465	-0.3	0.8	1.7	$V_{CCIO} + 0.3$	—	—	—	—
2.5 V Schmitt Trigger	2.375	2.5	2.625	-0.3	0.7	1.7	$V_{CCIO} + 0.3$	—	—	—	—
1.8 V Schmitt Trigger	1.71	1.8	1.89	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	—	—	—	—
1.5 V Schmitt Trigger	1.425	1.5	1.575	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	—	—	—	—
3.0 V PCI	2.85	3	3.15	—	$0.3 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	1.5	-0.5



I/O Standard	V _{IL(DC)} (V)		V _{IH(DC)} (V)		V _{IL(AC)} (V)		V _{IH(AC)} (V)		V _{OL} (V)	V _{OH} (V)	I _{OL} (mA)	I _{OH} (mA)
	Min	Max	Min	Max	Min	Max	Min	Max	Max	Min		
HSTL-12 Class I	-0.15	V _{REF} - 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	-0.24	V _{REF} - 0.15	V _{REF} + 0.15	V _{CCIO} + 0.24	0.25 × V _{CCIO}	0.75 × V _{CCIO}	8	-8
HSTL-12 Class II	-0.15	V _{REF} - 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	-0.24	V _{REF} - 0.15	V _{REF} + 0.15	V _{CCIO} + 0.24	0.25 × V _{CCIO}	0.75 × V _{CCIO}	14	-14
HSUL-12	—	V _{REF} - 0.13	V _{REF} + 0.13	—	—	V _{REF} - 0.22	V _{REF} + 0.22	—	0.1 × V _{CCIO}	0.9 × V _{CCIO}	—	—

Differential SSTL I/O Standards Specifications

Differential SSTL requires a V_{REF} input.

Table 23. Differential SSTL I/O Standards Specifications for Intel MAX 10 Devices

I/O Standard	V _{CCIO} (V)			V _{Swing(DC)} (V)		V _{X(AC)} (V)			V _{Swing(AC)} (V)	
	Min	Typ	Max	Min	Max ⁽¹⁷⁾	Min	Typ	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.36	V _{CCIO}	V _{CCIO} /2 - 0.2	—	V _{CCIO} /2 + 0.2	0.7	V _{CCIO}
SSTL-18 Class I, II	1.7	1.8	1.9	0.25	V _{CCIO}	V _{CCIO} /2 - 0.175	—	V _{CCIO} /2 + 0.175	0.5	V _{CCIO}
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	V _{CCIO} /2 - 0.15	—	V _{CCIO} /2 + 0.15	2(V _{IH(AC)} - V _{REF})	2(V _{IL(AC)} - V _{REF})
SSTL-135	1.283	1.35	1.45	0.18	—	V _{REF} - 0.135	0.5 × V _{CCIO}	V _{REF} + 0.135	2(V _{IH(AC)} - V _{REF})	2(V _{IL(AC)} - V _{REF})

Differential HSTL and HSUL I/O Standards Specifications

Differential HSTL requires a V_{REF} input.

⁽¹⁷⁾ The maximum value for V_{SWING(DC)} is not defined. However, each single-ended signal needs to be within the respective single-ended limits (V_{IH(DC)} and V_{IL(DC)}).

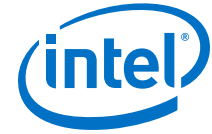


Table 24. Differential HSTL and HSUL I/O Standards Specifications for Intel MAX 10 Devices

I/O Standard	V _{CCIO} (V)			V _{DIF(DC)} (V)		V _{X(AC)} (V)			V _{CM(DC)} (V)			V _{DIF(AC)} (V)
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.85	—	0.95	0.85	—	0.95	0.4
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.71	—	0.79	0.71	—	0.79	0.4
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V _{CCIO}	0.48 × V _{CCIO}	0.5 × V _{CCIO}	0.52 × V _{CCIO}	0.48 × V _{CCIO}	0.5 × V _{CCIO}	0.52 × V _{CCIO}	0.3
HSUL-12	1.14	1.2	1.3	0.26	—	0.5 × V _{CCIO} – 0.12	0.5 × V _{CCIO}	0.5 × V _{CCIO} + 0.12	0.4 × V _{CCIO}	0.5 × V _{CCIO}	0.6 × V _{CCIO}	0.44

Differential I/O Standards Specifications

Table 25. Differential I/O Standards Specifications for Intel MAX 10 Devices

I/O Standard	V _{CCIO} (V)			V _{ID} (mV)		V _{ICM} (V) ⁽¹⁸⁾			V _{OD} (mV) ⁽¹⁹⁾⁽²⁰⁾			V _{OS} (V) ⁽¹⁹⁾		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVPECL ⁽²¹⁾	2.375	2.5	2.625	100	—	0.05	D _{MAX} ≤ 500 Mbps	1.8	—	—	—	—	—	—
						0.55	500 Mbps ≤ D _{MAX} ≤ 700 Mbps	1.8						
						1.05	D _{MAX} > 700 Mbps	1.55						
LVDS	2.375	2.5	2.625	100	—	0.05	D _{MAX} ≤ 500 Mbps	1.8	247	—	600	1.125	1.25	1.375
						0.55	500 Mbps ≤ D _{MAX} ≤ 700 Mbps	1.8						

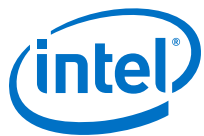
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⁽¹⁸⁾ V_{IN} range: 0 V ≤ V_{IN} ≤ 1.85 V.

⁽¹⁹⁾ R_L range: 90 ≤ R_L ≤ 110 Ω.

⁽²⁰⁾ Low V_{OD} setting is only supported for RSDS standard.

⁽²¹⁾ LVPECL input standard is only supported at clock input. Output standard is not supported.

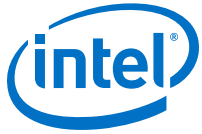


I/O Standard	V _{CCIO} (V)			V _{ID} (mV)		V _{ICM} (V) ⁽¹⁸⁾			V _{OD} (mV) ⁽¹⁹⁾⁽²⁰⁾			V _{OS} (V) ⁽¹⁹⁾		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
						1.05	D _{MAX} > 700 Mbps	1.55						
BLVDS ⁽²²⁾	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—
mini-LVDS ⁽²³⁾	2.375	2.5	2.625	—	—	—	—	—	300	—	600	1	1.2	1.4
RSDS ⁽²³⁾	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.5
PPDS (Row I/Os) ⁽²³⁾	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.4
TMDS ⁽²⁴⁾	2.375	2.5	2.625	100	—	0.05	D _{MAX} ≤ 500 Mbps	1.8	—	—	—	—	—	—
						0.55	500 Mbps ≤ D _{MAX} ≤ 700 Mbps	1.8						
						1.05	D _{MAX} > 700 Mbps	1.55						
Sub-LVDS ⁽²⁵⁾	1.71	1.8	1.89	100	—	0.55	—	1.25	⁽²⁶⁾			0.8	0.9	1
SLVS	2.375	2.5	2.625	100	—	0.05	—	1.1	⁽²⁶⁾			⁽²⁷⁾		
continued..														

⁽¹⁸⁾ V_{IN} range: 0 V ≤ V_{IN} ≤ 1.85 V.

⁽¹⁹⁾ R_L range: 90 ≤ R_L ≤ 110 Ω.

⁽²⁰⁾ Low V_{OD} setting is only supported for RSBS standard.



Core Performance Specifications

Clock Tree Specifications

Table 26. Clock Tree Specifications for Intel MAX 10 Devices

Device	Performance					Unit
	-I6	-A6, -C7	-I7	-A7	-C8	
10M02	450	416	416	382	402	MHz
10M04	450	416	416	382	402	MHz
10M08	450	416	416	382	402	MHz
10M16	450	416	416	382	402	MHz
10M25	450	416	416	382	402	MHz
10M40	450	416	416	382	402	MHz
10M50	450	416	416	382	402	MHz

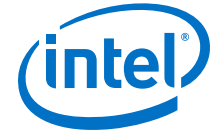
PLL Specifications

Table 27. PLL Specifications for Intel MAX 10 Devices

V_{CCD_PLL} should always be connected to V_{CCINT} through decoupling capacitor and ferrite bead.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{IN}^{(28)}$	Input clock frequency	—	5	—	472.5	MHz
f_{INPFD}	Phase frequency detector (PFD) input frequency	—	5	—	325	MHz
continued...						

(28) This parameter is limited in the Intel Quartus Prime software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.



Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{VCO} ⁽²⁹⁾	PLL internal voltage-controlled oscillator (VCO) operating range	—	600	—	1300	MHz
f_{INDUTY}	Input clock duty cycle	—	40	—	60	%
$t_{INJITTER_CCJ}$ ⁽³⁰⁾	Input clock cycle-to-cycle jitter	$F_{INPFD} \geq 100$ MHz	—	—	0.15	UI
		$F_{INPFD} < 100$ MHz	—	—	±750	ps
f_{OUT_EXT} ⁽²⁸⁾	PLL output frequency for external clock output	—	—	—	472.5	MHz
f_{OUT}	PLL output frequency to global clock	–6 speed grade	—	—	472.5	MHz
		–7 speed grade	—	—	450	MHz
		–8 speed grade	—	—	402.5	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output	Duty cycle set to 50%	45	50	55	%
t_{LOCK}	Time required to lock from end of device configuration	—	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically	After switchover, reconfiguring any non-post-scale counters or delays, or when areset is deasserted	—	—	1	ms
$t_{OUTJITTER_PERIOD_IO}$ ⁽³¹⁾	Regular I/O period jitter	$F_{OUT} \geq 100$ MHz	—	—	650	ps
		$F_{OUT} < 100$ MHz	—	—	75	mUI
$t_{OUTJITTER_CCJ_IO}$ ⁽³¹⁾	Regular I/O cycle-to-cycle jitter	$F_{OUT} \geq 100$ MHz	—	—	650	ps
		$F_{OUT} < 100$ MHz	—	—	75	mUI

continued...

- ⁽²⁹⁾ The VCO frequency reported by the Intel Quartus Prime software in the PLL summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.
- ⁽³⁰⁾ A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source, which is less than 200 ps.
- ⁽³¹⁾ Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied.



ADC Performance Specifications

Single Supply Devices ADC Performance Specifications

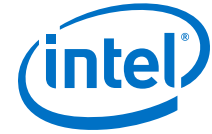
Table 34. ADC Performance Specifications for Intel MAX 10 Single Supply Devices

Parameter		Symbol	Condition	Min	Typ	Max	Unit
ADC resolution		—	—	—	—	12	bits
ADC supply voltage		V_{CC_ONE}	—	2.85	3.0/3.3	3.465	V
External reference voltage		V_{REF}	—	$V_{CC_ONE} - 0.5$	—	V_{CC_ONE}	V
Sampling rate		F_S	Accumulative sampling rate	—	—	1	MSPS
Operating junction temperature range		T_J	—	−40	25	125	°C
Analog input voltage		V_{IN}	Prescaler disabled	0	—	V_{REF}	V
			Prescaler enabled ⁽³⁵⁾	0	—	3.6	V
Input resistance		R_{IN}	—	—	⁽³⁶⁾	—	—
Input capacitance		C_{IN}	—	—	⁽³⁶⁾	—	—
DC Accuracy	Offset error and drift	E_{offset}	Prescaler disabled	−0.2	—	0.2	%FS
			Prescaler enabled	−0.5	—	0.5	%FS
	Gain error and drift	E_{gain}	Prescaler disabled	−0.5	—	0.5	%FS
			Prescaler enabled	−0.75	—	0.75	%FS
	Differential non linearity	DNL	External V_{REF} , no missing code	−0.9	—	0.9	LSB
			Internal V_{REF} , no missing code	−1	—	1.7	LSB

continued...

⁽³⁵⁾ Prescaler function divides the analog input voltage by half. The analog input handles up to 3.6 V for the Intel MAX 10 single supply devices.

⁽³⁶⁾ Download the SPICE models for simulation.



Parameter		Symbol	Condition	Min	Typ	Max	Unit
Conversion Rate ⁽⁵²⁾	Conversion time	—	Single measurement	—	—	1	Cycle
			Continuous measurement	—	—	1	Cycle
			Temperature measurement	—	—	1	Cycle

Related Information

[SPICE Models for Intel FPGAs](#)

Periphery Performance Specifications

This section describes the periphery performance, high-speed I/O, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

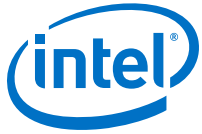
High-Speed I/O Specifications

For more information about the high-speed and low-speed I/O performance pins, refer to the respective device pin-out files.

Related Information

[Documentation: Pin-Out Files for Intel FPGAs](#)

⁽⁵²⁾ For more detailed description, refer to the Timing section in the *Intel MAX 10 Analog-to-Digital Converter User Guide*.



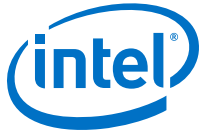
Dual Supply Devices True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications

Table 38. True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

True **RSDS** transmitter is only supported at bottom I/O banks. Emulated **RSDS** transmitter is supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	-I6, -A6, -C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{HCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	—	155	5	—	155	5	—	155	MHz
		×8	5	—	155	5	—	155	5	—	155	MHz
		×7	5	—	155	5	—	155	5	—	155	MHz
		×4	5	—	155	5	—	155	5	—	155	MHz
		×2	5	—	155	5	—	155	5	—	155	MHz
		×1	5	—	310	5	—	310	5	—	310	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	—	310	100	—	310	100	—	310	Mbps
		×8	80	—	310	80	—	310	80	—	310	Mbps
		×7	70	—	310	70	—	310	70	—	310	Mbps
		×4	40	—	310	40	—	310	40	—	310	Mbps
		×2	20	—	310	20	—	310	20	—	310	Mbps
		×1	10	—	310	10	—	310	10	—	310	Mbps
f _{HCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	—	150	5	—	150	5	—	150	MHz
		×8	5	—	150	5	—	150	5	—	150	MHz
		×7	5	—	150	5	—	150	5	—	150	MHz
		×4	5	—	150	5	—	150	5	—	150	MHz
		×2	5	—	150	5	—	150	5	—	150	MHz
		×1	5	—	300	5	—	300	5	—	300	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	—	300	100	—	300	100	—	300	Mbps
		×8	80	—	300	80	—	300	80	—	300	Mbps
		×7	70	—	300	70	—	300	70	—	300	Mbps

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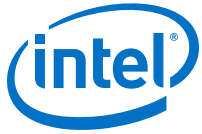
Emulated RSDS_E_1R Transmitter Timing Specifications

Table 39. Emulated RSDS_E_1R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

Emulated **RSDS_E_1R** transmitter is supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{HCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	—	85	5	—	85	5	—	85	MHz
		×8	5	—	85	5	—	85	5	—	85	MHz
		×7	5	—	85	5	—	85	5	—	85	MHz
		×4	5	—	85	5	—	85	5	—	85	MHz
		×2	5	—	85	5	—	85	5	—	85	MHz
		×1	5	—	170	5	—	170	5	—	170	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	—	170	100	—	170	100	—	170	Mbps
		×8	80	—	170	80	—	170	80	—	170	Mbps
		×7	70	—	170	70	—	170	70	—	170	Mbps
		×4	40	—	170	40	—	170	40	—	170	Mbps
		×2	20	—	170	20	—	170	20	—	170	Mbps
		×1	10	—	170	10	—	170	10	—	170	Mbps
f _{HCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	—	85	5	—	85	5	—	85	MHz
		×8	5	—	85	5	—	85	5	—	85	MHz
		×7	5	—	85	5	—	85	5	—	85	MHz
		×4	5	—	85	5	—	85	5	—	85	MHz
		×2	5	—	85	5	—	85	5	—	85	MHz
		×1	5	—	170	5	—	170	5	—	170	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	—	170	100	—	170	100	—	170	Mbps
		×8	80	—	170	80	—	170	80	—	170	Mbps
		×7	70	—	170	70	—	170	70	—	170	Mbps

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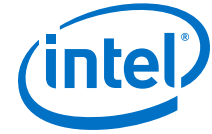
True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications

Table 40. True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

True **mini-LVDS** transmitter is only supported at the bottom I/O banks. Emulated **mini-LVDS_E_3R** transmitter is supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	-I6, -A6, -C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{HCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	—	155	5	—	155	5	—	155	MHz
		×8	5	—	155	5	—	155	5	—	155	MHz
		×7	5	—	155	5	—	155	5	—	155	MHz
		×4	5	—	155	5	—	155	5	—	155	MHz
		×2	5	—	155	5	—	155	5	—	155	MHz
		×1	5	—	310	5	—	310	5	—	310	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	—	310	100	—	310	100	—	310	Mbps
		×8	80	—	310	80	—	310	80	—	310	Mbps
		×7	70	—	310	70	—	310	70	—	310	Mbps
		×4	40	—	310	40	—	310	40	—	310	Mbps
		×2	20	—	310	20	—	310	20	—	310	Mbps
		×1	10	—	310	10	—	310	10	—	310	Mbps
f _{HCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	—	150	5	—	150	5	—	150	MHz
		×8	5	—	150	5	—	150	5	—	150	MHz
		×7	5	—	150	5	—	150	5	—	150	MHz
		×4	5	—	150	5	—	150	5	—	150	MHz
		×2	5	—	150	5	—	150	5	—	150	MHz
		×1	5	—	300	5	—	300	5	—	300	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	—	300	100	—	300	100	—	300	Mbps
		×8	80	—	300	80	—	300	80	—	300	Mbps

continued...



Symbol	Parameter	Mode	-C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t _{RISE}	Rise time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{FALL}	Fall time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

Dual Supply Devices True LVDS Transmitter Timing Specifications

Table 42. True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

True LVDS transmitter is only supported at the bottom I/O banks.

Symbol	Parameter	Mode	-I6			-A6, -C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{HSCLK}	Input clock frequency	×10	5	—	360	5	—	340	5	—	310	5	—	300	MHz
		×8	5	—	360	5	—	360	5	—	320	5	—	320	MHz
		×7	5	—	360	5	—	340	5	—	310	5	—	300	MHz
		×4	5	—	360	5	—	350	5	—	320	5	—	320	MHz
		×2	5	—	360	5	—	350	5	—	320	5	—	320	MHz
		×1	5	—	360	5	—	350	5	—	320	5	—	320	MHz
HSIODR	Data rate	×10	100	—	720	100	—	680	100	—	620	100	—	600	Mbps
		×8	80	—	720	80	—	720	80	—	640	80	—	640	Mbps
		×7	70	—	720	70	—	680	70	—	620	70	—	600	Mbps
		×4	40	—	720	40	—	700	40	—	640	40	—	640	Mbps
		×2	20	—	720	20	—	700	20	—	640	20	—	640	Mbps

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Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications

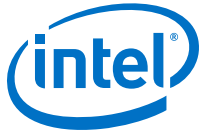
Single Supply Devices Emulated LVDS_E_3R Transmitter Timing Specifications

Table 43. Emulated LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices

Emulated **LVDS_E_3R** transmitters are supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	-C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{HCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	—	142.5	5	—	100	5	—	100	MHz
		×8	5	—	142.5	5	—	100	5	—	100	MHz
		×7	5	—	142.5	5	—	100	5	—	100	MHz
		×4	5	—	142.5	5	—	100	5	—	100	MHz
		×2	5	—	142.5	5	—	100	5	—	100	MHz
		×1	5	—	285	5	—	200	5	—	200	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	—	285	100	—	200	100	—	200	Mbps
		×8	80	—	285	80	—	200	80	—	200	Mbps
		×7	70	—	285	70	—	200	70	—	200	Mbps
		×4	40	—	285	40	—	200	40	—	200	Mbps
		×2	20	—	285	20	—	200	20	—	200	Mbps
		×1	10	—	285	10	—	200	10	—	200	Mbps
f _{HCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	—	100	5	—	100	5	—	100	MHz
		×8	5	—	100	5	—	100	5	—	100	MHz
		×7	5	—	100	5	—	100	5	—	100	MHz
		×4	5	—	100	5	—	100	5	—	100	MHz
		×2	5	—	100	5	—	100	5	—	100	MHz
		×1	5	—	200	5	—	200	5	—	200	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	—	200	100	—	200	100	—	200	Mbps

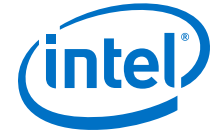
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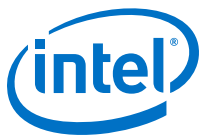
Symbol	Parameter	Mode	-I6, -A6, -C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×7	70	—	300	70	—	300	70	—	300	Mbps
		×4	40	—	300	40	—	300	40	—	300	Mbps
		×2	20	—	300	20	—	300	20	—	300	Mbps
		×1	10	—	300	10	—	300	10	—	300	Mbps
t _{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS ⁽⁶⁹⁾	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
t _{x jitter} ⁽⁷⁰⁾	Output jitter (high-speed I/O performance pin)	—	—	—	425	—	—	425	—	—	425	ps
	Output jitter (low-speed I/O performance pin)	—	—	—	470	—	—	470	—	—	470	ps
t _{RISE}	Rise time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{FALL}	Fall time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

⁽⁶⁹⁾ TCCS specifications apply to I/O banks from the same side only.

⁽⁷⁰⁾ TX jitter is the jitter induced from core noise and I/O switching noise.



Symbol	Parameter	Mode	-I6, -A6, -C7, -I7		-A7		-C8		Unit
			Min	Max	Min	Max	Min	Max	
		×2	5	360	5	320	5	320	MHz
		×1	5	360	5	320	5	320	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	700	100	640	100	640	Mbps
		×8	80	720	80	640	80	640	Mbps
		×7	70	700	70	640	70	640	Mbps
		×4	40	720	40	640	40	640	Mbps
		×2	20	720	20	640	20	640	Mbps
		×1	10	360	10	320	10	320	Mbps
f _{HSCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	150	5	150	5	150	MHz
		×8	5	150	5	150	5	150	MHz
		×7	5	150	5	150	5	150	MHz
		×4	5	150	5	150	5	150	MHz
		×2	5	150	5	150	5	150	MHz
		×1	5	300	5	300	5	300	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	300	100	300	100	300	Mbps
		×8	80	300	80	300	80	300	Mbps
		×7	70	300	70	300	70	300	Mbps
		×4	40	300	40	300	40	300	Mbps
		×2	20	300	20	300	20	300	Mbps
		×1	10	300	10	300	10	300	Mbps
SW	Sampling window (high-speed I/O performance pin)	—	—	510	—	510	—	510	ps
continued...									



Glossary

Table 59. Glossary

Term	Definition
JTAG Timing Specifications	
R_L	Receiver differential input discrete resistor (external to Intel MAX 10 devices).
RSKM (Receiver input skew margin)	HIGH-SPEED I/O block: The total margin left after accounting for the sampling window and TCCS. $RSKM = (TUI - SW - TCCS) / 2$.
Sampling window (SW)	HIGH-SPEED I/O Block: The period of time during which the data must be valid to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window.
Single-ended voltage referenced I/O standard	The AC input signal values indicate the voltage levels at which the receiver must meet its timing specifications. The DC input signal values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input crosses the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing.
t_c	High-speed receiver/transmitter input and output clock period.
TCCS (Channel-to- channel-skew)	HIGH-SPEED I/O block: The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
t_{cin}	Delay from clock pad to I/O input register.
t_{CO}	Delay from clock pad to I/O output.
t_{cout}	Delay from clock pad to I/O output register.
continued...	



Term	Definition
V _{OCM}	Output common mode voltage: The common mode of the differential signal at the transmitter.
V _{OD}	Output differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission line at the transmitter. $V_{OD} = V_{OH} - V_{OL}$.
V _{OH}	Voltage output high: The maximum positive voltage from an output which the device considers is accepted as the minimum positive high level.
V _{OL}	Voltage output low: The maximum positive voltage from an output which the device considers is accepted as the maximum positive low level.
V _{OS}	Output offset voltage: $V_{OS} = (V_{OH} + V_{OL}) / 2$.
V _{OX (AC)}	AC differential Output cross point voltage: The voltage at which the differential output signals must cross.
V _{REF}	Reference voltage for SSTL, HSTL, and HSUL I/O Standards.
V _{REF(AC)}	AC input reference voltage for SSTL, HSTL, and HSUL I/O Standards. $V_{REF(AC)} = V_{REF(DC)} + \text{noise}$. The peak-to-peak AC noise on V _{REF} should not exceed 2% of V _{REF(DC)} .
V _{REF(DC)}	DC input reference voltage for SSTL, HSTL, and HSUL I/O Standards.
V _{SWING (AC)}	AC differential input voltage: AC Input differential voltage required for switching.
V _{SWING (DC)}	DC differential input voltage: DC Input differential voltage required for switching.
V _{TT}	Termination voltage for SSTL, HSTL, and HSUL I/O Standards.
V _{X (AC)}	AC differential Input cross point voltage: The voltage at which the differential input signals must cross.

Document Revision History for the Intel MAX 10 FPGA Device Datasheet

Document Version	Changes
2018.06.29	- Removed links on instant-on feature. - Added JTAG timing specifications term in <i>Glossary</i>. - Renamed the following IP cores as per Intel rebranding: - Renamed Altera Modular ADC IP core to Modular ADC core Intel FPGA IP core. - Renamed Altera Modular Dual ADC IP core to Modular Dual ADC core Intel FPGA IP core.