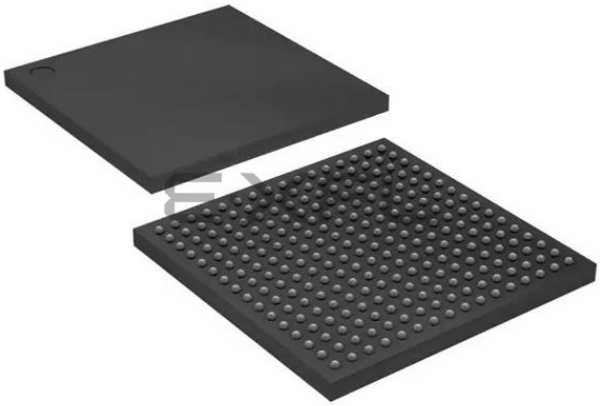

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Details	
Product Status	Active
Number of LABs/CLBs	2500
Number of Logic Elements/Cells	40000
Total RAM Bits	1290240
Number of I/O	178
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10m40dcf256c8g

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Symbol	Parameter	Condition	Min	Typ	Max	Unit
		1.35 V	1.2825	1.35	1.4175	V
		1.2 V	1.14	1.2	1.26	V
V_{CCA} (1)	Supply voltage for PLL regulator and ADC block (analog)	—	2.85/3.135	3.0/3.3	3.15/3.465	V

Dual Supply Devices Power Supplies Recommended Operating Conditions

Table 7. Power Supplies Recommended Operating Conditions for Intel MAX 10 Dual Supply Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CC}	Supply voltage for core and periphery	—	1.15	1.2	1.25	V
V_{CCIO} (3)	Supply voltage for input and output buffers	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.35 V	1.2825	1.35	1.4175	V
		1.2 V	1.14	1.2	1.26	V
V_{CCA}(4)	Supply voltage for PLL regulator (analog)	—	2.375	2.5	2.625	V
V_{CCD_PLL}(5)	Supply voltage for PLL regulator (digital)	—	1.15	1.2	1.25	V
V_{CCA_ADC}	Supply voltage for ADC analog block	—	2.375	2.5	2.625	V
V_{CCINT}	Supply voltage for ADC digital block	—	1.15	1.2	1.25	V

(3) V_{CCIO} for all I/O banks must be powered up during user mode because V_{CCIO} I/O banks are used for the ADC and I/O functionalities.

(4) All V_{CCA} pins must be powered to 2.5 V (even when PLLs are not used), and must be powered up and powered down at the same time.

(5) V_{CCD_PLL} must always be connected to V_{CC} through a decoupling capacitor and ferrite bead.

Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications

Table 22. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Intel MAX 10 Devices

To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL-15 Class I specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)		$V_{IH(AC)}$ (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Max	Min	Max	Min	Max	Min	Max	Max	Min		
SSTL-2 Class I	—	V_{REF} – 0.18	V_{REF} + 0.18	—	—	V_{REF} – 0.31	V_{REF} + 0.31	—	V_{TT} – 0.57	V_{TT} + 0.57	8.1	–8.1
SSTL-2 Class II	—	V_{REF} – 0.18	V_{REF} + 0.18	—	—	V_{REF} – 0.31	V_{REF} + 0.31	—	V_{TT} – 0.76	V_{TT} + 0.76	16.4	–16.4
SSTL-18 Class I	—	V_{REF} – 0.125	V_{REF} + 0.125	—	—	V_{REF} – 0.25	V_{REF} + 0.25	—	V_{TT} – 0.475	V_{TT} + 0.475	6.7	–6.7
SSTL-18 Class II	—	V_{REF} – 0.125	V_{REF} + 0.125	—	—	V_{REF} – 0.25	V_{REF} + 0.25	—	0.28	V_{CCIO} – 0.28	13.4	–13.4
SSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.175	V_{REF} + 0.175	—	0.2 × V_{CCIO}	0.8 × V_{CCIO}	8	–8
SSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.175	V_{REF} + 0.175	—	0.2 × V_{CCIO}	0.8 × V_{CCIO}	16	–16
SSTL-135	—	V_{REF} – 0.09	V_{REF} + 0.09	—	—	V_{REF} – 0.16	V_{REF} + 0.16	—	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—
HSTL-18 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	16	–16

continued...

Table 24. Differential HSTL and HSUL I/O Standards Specifications for Intel MAX 10 Devices

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.85	—	0.95	0.85	—	0.95	0.4
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.71	—	0.79	0.71	—	0.79	0.4
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO}	0.48 × V_{CCIO}	0.5 × V_{CCIO}	0.52 × V_{CCIO}	0.48 × V_{CCIO}	0.5 × V_{CCIO}	0.52 × V_{CCIO}	0.3
HSUL-12	1.14	1.2	1.3	0.26	—	0.5 × V_{CCIO} – 0.12	0.5 × V_{CCIO}	0.5 × V_{CCIO} + 0.12	0.4 × V_{CCIO}	0.5 × V_{CCIO}	0.6 × V_{CCIO}	0.44

Differential I/O Standards Specifications

Table 25. Differential I/O Standards Specifications for Intel MAX 10 Devices

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)		V_{ICM} (V) (18)			V_{OD} (mV) (19)(20)			V_{OS} (V) (19)		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVPECL (21)	2.375	2.5	2.625	100	—	0.05	D_{MAX} ≤ 500 Mbps	1.8	—	—	—	—	—	—
						0.55	500 Mbps ≤ D_{MAX} ≤ 700 Mbps	1.8						
						1.05	D_{MAX} > 700 Mbps	1.55						
LVDS	2.375	2.5	2.625	100	—	0.05	D_{MAX} ≤ 500 Mbps	1.8	247	—	600	1.125	1.25	1.375
						0.55	500 Mbps ≤ D_{MAX} ≤ 700 Mbps	1.8						

continued...

(18) V_{IN} range: 0 V ≤ V_{IN} ≤ 1.85 V.

(19) R_L range: 90 ≤ R_L ≤ 110 Ω.

(20) Low V_{OD} setting is only supported for RSDS standard.

(21) LVPECL input standard is only supported at clock input. Output standard is not supported.

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)		V_{ICM} (V) (18)			V_{OD} (mV) (19)(20)			V_{OS} (V) (19)		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
HiSpi	2.375	2.5	2.625	100	—	0.05	D_{MAX} ≤ 500 Mbps	1.8	—	—	—	—	—	—
						0.55	500 Mbps ≤ D_{MAX} ≤ 700 Mbps	1.8						
						1.05	D_{MAX} > 700 Mbps	1.55						

Related Information

Intel MAX 10 LVDS SERDES I/O Standards Support, Intel MAX 10 High-Speed LVDS I/O User Guide
Provides the list of I/O standards supported in single supply and dual supply devices.

Switching Characteristics

This section provides the performance characteristics of Intel MAX 10 core and periphery blocks.

(18) V_{IN} range: 0 V ≤ V_{IN} ≤ 1.85 V.
(19) R_L range: 90 ≤ R_L ≤ 110 Ω.
(20) Low V_{OD} setting is only supported for RSDS standard.

(22) No fixed V_{IN} , V_{OD} , and V_{OS} specifications for Bus LVDS (BLVDS). They are dependent on the system topology.

(23) Mini-LVDS, RSDS, and Point-to-Point Differential Signaling (PPDS) standards are only supported at the output pins for Intel MAX 10 devices.

(24) Supported with requirement of an external level shift

(25) Sub-LVDS input buffer is using 2.5 V differential buffer.

(26) Differential output depends on the values of the external termination resistors.

(27) Differential output offset voltage depends on the values of the external termination resistors.

ADC Performance Specifications

Single Supply Devices ADC Performance Specifications

Table 34. ADC Performance Specifications for Intel MAX 10 Single Supply Devices

Parameter		Symbol	Condition	Min	Typ	Max	Unit
ADC resolution		—	—	—	—	12	bits
ADC supply voltage		V_{CC_ONE}	—	2.85	3.0/3.3	3.465	V
External reference voltage		V_{REF}	—	V_{CC_ONE} – 0.5	—	V_{CC_ONE}	V
Sampling rate		F_S	Accumulative sampling rate	—	—	1	MSPS
Operating junction temperature range		T_J	—	–40	25	125	°C
Analog input voltage		V_{IN}	Prescalar disabled	0	—	V_{REF}	V
			Prescalar enabled (35)	0	—	3.6	V
Input resistance		R_{IN}	—	—	(36)	—	—
Input capacitance		C_{IN}	—	—	(36)	—	—
DC Accuracy	Offset error and drift	E_{offset}	Prescalar disabled	–0.2	—	0.2	%FS
			Prescalar enabled	–0.5	—	0.5	%FS
	Gain error and drift	E_{gain}	Prescalar disabled	–0.5	—	0.5	%FS
			Prescalar enabled	–0.75	—	0.75	%FS
	Differential non linearity	DNL	External V_{REF}, no missing code	–0.9	—	0.9	LSB
			Internal V_{REF}, no missing code	–1	—	1.7	LSB

continued...

(35) Prescalar function divides the analog input voltage by half. The analog input handles up to 3.6 V for the Intel MAX 10 single supply devices.

(36) Download the SPICE models for simulation.

Parameter		Symbol	Condition	Min	Typ	Max	Unit
			Internal V_{REF}, no missing code	–1	—	1.7	LSB
	Integral non linearity	INL	—	–2	—	2	LSB
AC Accuracy	Total harmonic distortion	THD	F_{IN} = 50 kHz, F_S = 1 MHz, PLL	–70 (44)(45)(46)	—	—	dB
	Signal-to-noise ratio	SNR	F_{IN} = 50 kHz, F_S = 1 MHz, PLL	62 (47)(48)(46)	—	—	dB
	Signal-to-noise and distortion	SINAD	F_{IN} = 50 kHz, F_S = 1 MHz, PLL	61.5 (49)(50)(46)	—	—	dB
On-Chip Temperature Sensor	Temperature sampling rate	T_S	—	—	—	50	kSPS
	Absolute accuracy	—	–40 to 125°C, with 64 samples averaging (51)	—	—	±5	°C

continued...

(44) Total harmonic distortion is –65 dB for dual function pin.

(45) THD with prescalar enabled is 6dB less than the specification.

(46) When using internal V_{REF}, THD = 66 dB, SNR = 58 dB and SINAD = 57.5 dB for dedicated ADC input channels.

(47) Signal-to-noise ratio is 54 dB for dual function pin.

(48) SNR with prescalar enabled is 6dB less than the specification.

(49) Signal-to-noise and distortion is 53 dB for dual function pin.

(50) SINAD with prescalar enabled is 6dB less than the specification.

(51) For the Intel Quartus Prime software version 15.0 and later, Modular ADC Core and Modular Dual ADC Core IP cores handle the 64 samples averaging. For the Intel Quartus Prime software versions prior to 14.1, you need to implement your own averaging calculation.

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×4	40	—	300	40	—	300	40	—	300	Mbps
		×2	20	—	300	20	—	300	20	—	300	Mbps
		×1	10	—	300	10	—	300	10	—	300	Mbps
t_{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS[53]	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
$t_{x\ Jitter}$[54]	Output jitter (high-speed I/O performance pin)	—	—	—	425	—	—	425	—	—	425	ps
	Output jitter (low-speed I/O performance pin)	—	—	—	470	—	—	470	—	—	470	ps
t_{RISE}	Rise time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	Fall time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

(53) TCCS specifications apply to I/O banks from the same side only.

(54) TX jitter is the jitter induced from core noise and I/O switching noise.

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×7	70	—	300	70	—	300	70	—	300	Mbps
		×4	40	—	300	40	—	300	40	—	300	Mbps
		×2	20	—	300	20	—	300	20	—	300	Mbps
		×1	10	—	300	10	—	300	10	—	300	Mbps
t_{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS[61]	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
$t_{x\ Jitter}$[62]	Output jitter (high-speed I/O performance pin)	—	—	—	425	—	—	425	—	—	425	ps
	Output jitter (low-speed I/O performance pin)	—	—	—	470	—	—	470	—	—	470	ps
t_{RISE}	Rise time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	Fall time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	Time required for the PLL to lock, after `CONF_DONE` signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

(61) TCCS specifications apply to I/O banks from the same side only.

(62) TX jitter is the jitter induced from core noise and I/O switching noise.

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×7	70	—	300	70	—	300	70	—	300	Mbps
		×4	40	—	300	40	—	300	40	—	300	Mbps
		×2	20	—	300	20	—	300	20	—	300	Mbps
		×1	10	—	300	10	—	300	10	—	300	Mbps
t_{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS[69]	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
$t_{x\ Jitter}$[70]	Output jitter (high-speed I/O performance pin)	—	—	—	425	—	—	425	—	—	425	ps
	Output jitter (low-speed I/O performance pin)	—	—	—	470	—	—	470	—	—	470	ps
t_{RISE}	Rise time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	Fall time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

(69) TCCS specifications apply to I/O banks from the same side only.

(70) TX jitter is the jitter induced from core noise and I/O switching noise.

LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications

Single Supply Devices LVDS Receiver Timing Specifications

Table 45. LVDS Receiver Timing Specifications for Intel MAX 10 Single Supply Devices

LVDS receivers are supported at all banks.

Symbol	Parameter	Mode	–C7, –I7		–A7		–C8		Unit
			Min	Max	Min	Max	Min	Max	
f_{HSCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	145	5	100	5	100	MHz
		×8	5	145	5	100	5	100	MHz
		×7	5	145	5	100	5	100	MHz
		×4	5	145	5	100	5	100	MHz
		×2	5	145	5	100	5	100	MHz
		×1	5	290	5	200	5	200	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	290	100	200	100	200	Mbps
		×8	80	290	80	200	80	200	Mbps
		×7	70	290	70	200	70	200	Mbps
		×4	40	290	40	200	40	200	Mbps
		×2	20	290	20	200	20	200	Mbps
		×1	10	290	10	200	10	200	Mbps
f_{HSCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	100	5	100	5	100	MHz
		×8	5	100	5	100	5	100	MHz
		×7	5	100	5	100	5	100	MHz
		×4	5	100	5	100	5	100	MHz
		×2	5	100	5	100	5	100	MHz
		×1	5	200	5	200	5	200	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	200	100	200	100	200	Mbps

continued...

Symbol	Parameter	Mode	–C7, –I7		–A7		–C8		Unit
			Min	Max	Min	Max	Min	Max	
		×8	80	200	80	200	80	200	Mbps
		×7	70	200	70	200	70	200	Mbps
		×4	40	200	40	200	40	200	Mbps
		×2	20	200	20	200	20	200	Mbps
		×1	10	200	10	200	10	200	Mbps
SW	Sampling window (high-speed I/O performance pin)	—	—	910	—	910	—	910	ps
	Sampling window (low-speed I/O performance pin)	—	—	1,110	—	1,110	—	1,110	ps
$t_{x\ Jitter}$(71)	Input jitter	—	—	1,000	—	1,000	—	1,000	ps
t_{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	1	—	1	—	1	ms

Dual Supply Devices LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications

Table 46. LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices

LVDS, **TMDS**, **HiSpi**, **SLVS**, and **Sub-LVDS** receivers are supported at all banks.

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7		–A7		–C8		Unit
			Min	Max	Min	Max	Min	Max	
f_{HSCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	350	5	320	5	320	MHz
		×8	5	360	5	320	5	320	MHz
		×7	5	350	5	320	5	320	MHz
		×4	5	360	5	320	5	320	MHz

continued...

(71) TX jitter is the jitter induced from core noise and I/O switching noise.

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7		–A7		–C8		Unit
			Min	Max	Min	Max	Min	Max	
	Sampling window (low-speed I/O performance pin)	—	—	910	—	910	—	910	ps
$t_{x\ Jitter}$[72]	Input jitter	—	—	500	—	500	—	500	ps
t_{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	1	—	1	—	1	ms

Memory Standards Supported by the Soft Memory Controller

Table 47. Memory Standards Supported by the Soft Memory Controller for Intel MAX 10 Devices

Contact your local sales representatives for access to the -I6 or -A6 speed grade devices in the Intel Quartus Prime software.

External Memory Interface Standard	Rate Support	Speed Grade	Voltage (V)	Max Frequency (MHz)
DDR3 SDRAM	Half	–I6	1.5	303
DDR3L SDRAM	Half	–I6	1.35	303
DDR2 SDRAM	Half	–I6	1.8	200
		–I7 and –C7		167
LPDDR2[73]	Half	–I6	1.2	200[74]

Related Information

External Memory Interface Spec Estimator
Provides the specific details of the memory standards supported.

(72) TX jitter is the jitter induced from core noise and I/O switching noise.

(73) Intel MAX 10 devices support only single-die LPDDR2.

(74) To achieve the specified performance, constrain the memory device I/O and core power supply variation to within ±3%. By default, the frequency is 167 MHz.

Table 54. Internal Configuration Time for Intel MAX 10 Devices (Compressed .rbf)

Compression ratio depends on design complexity. The minimum value is based on the best case (25% of original `.rbf` sizes) and the maximum value is based on the typical case (70% of original `.rbf` sizes).

Device	Internal Configuration Time (ms)			
	Unencrypted/Encrypted			
	Without Memory Initialization		With Memory Initialization	
	Min	Max	Min	Max
10M02	0.3	5.2	—	—
10M04	0.6	10.7	1.0	13.9
10M08	0.6	10.7	1.0	13.9
10M16	1.1	17.9	1.4	22.3
10M25	1.1	26.9	1.4	32.2
10M40	2.6	66.1	3.2	82.2
10M50	2.6	66.1	3.2	82.2

Internal Configuration Timing Parameter

Table 55. Internal Configuration Timing Parameter for Intel MAX 10 Devices

Symbol	Parameter	Device	Minimum	Maximum	Unit
t_{CD2UM}	`CONF_DONE` high to user mode	10M02, 10M04, 10M08, 10M16, 10M25	182.8	385.5	µs
		10M40, 10M50	275.3	605.7	µs

I/O Timing

The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

The Intel Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specific device and design after you complete place-and-route.

Table 56. I/O Timing for Intel MAX 10 Devices

These I/O timing parameters are for the 3.3-V LVTTL I/O standard with the maximum drive strength and fast slew rate for 10M08DAF484 device.

Symbol	Parameter	–C7, –I7	–C8	Unit
T_{su}	Global clock setup time	–0.750	–0.808	ns
T_h	Global clock hold time	1.180	1.215	ns
T_{co}	Global clock to output delay	5.131	5.575	ns
T_{pd}	Best case pin-to-pin propagation delay through one LUT	4.907	5.467	ns

Programmable IOE Delay

Programmable IOE Delay On Row Pins

Table 57. IOE Programmable Delay on Row Pins for Intel MAX 10 Devices

The incremental values for the settings are generally linear. For exact values of each setting, refer to the **Assignment Name** column in the latest version of the Intel Quartus Prime software.

The minimum and maximum offset timing numbers are in reference to setting '0' as available in the Intel Quartus Prime software.

Parameter	Paths Affected	Number of Settings	Minimum Offset	Maximum Offset							Unit
				Fast Corner		Slow Corner					
				–I7	–C8	–A6	–C7	–C8	–I7	–A7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	0.815	0.873	1.831	1.811	1.874	1.871	1.922	ns
Input delay from pin to input register	Pad to I/O input register	8	0	0.924	0.992	2.081	2.055	2.125	2.127	2.185	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.479	0.514	1.069	1.070	1.117	1.105	1.134	ns

Programmable IOE Delay for Column Pins

Table 58. IOE Programmable Delay on Column Pins for Intel MAX 10 Devices

The incremental values for the settings are generally linear. For exact values of each setting, refer to the **Assignment Name** column in the latest version of the Intel Quartus Prime software.

The minimum and maximum offset timing numbers are in reference to setting '0' as available in the Intel Quartus Prime software.

Parameter	Paths Affected	Number of Settings	Minimum Offset	Maximum Offset							Unit
				Fast Corner		Slow Corner					
				–I7	–C8	–A6	–C7	–C8	–I7	–A7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	0.81	0.868	1.823	1.802	1.864	1.862	1.912	ns
Input delay from pin to input register	Pad to I/O input register	8	0	0.914	0.981	2.06	2.032	2.101	2.102	2.161	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.435	0.466	0.971	0.97	1.013	1.001	1.028	ns

Term	Definition
V_{OCM}	Output common mode voltage: The common mode of the differential signal at the transmitter.
V_{OD}	Output differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission line at the transmitter. $V_{OD} = V_{OH} – V_{OL}$.
V_{OH}	Voltage output high: The maximum positive voltage from an output which the device considers is accepted as the minimum positive high level.
V_{OL}	Voltage output low: The maximum positive voltage from an output which the device considers is accepted as the maximum positive low level.
V_{OS}	Output offset voltage: $V_{OS} = (V_{OH} + V_{OL}) / 2$.
$V_{OX\ (AC)}$	AC differential Output cross point voltage: The voltage at which the differential output signals must cross.
V_{REF}	Reference voltage for SSTL, HSTL, and HSUL I/O Standards.
$V_{REF(AC)}$	AC input reference voltage for SSTL, HSTL, and HSUL I/O Standards. $V_{REF(AC)} = V_{REF(DC)}$ + noise. The peak-to-peak AC noise on V_{REF} should not exceed 2% of $V_{REF(DC)}$.
$V_{REF(DC)}$	DC input reference voltage for SSTL, HSTL, and HSUL I/O Standards.
$V_{SWING\ (AC)}$	AC differential input voltage: AC Input differential voltage required for switching.
$V_{SWING\ (DC)}$	DC differential input voltage: DC Input differential voltage required for switching.
V_{TT}	Termination voltage for SSTL, HSTL, and HSUL I/O Standards.
$V_{X\ (AC)}$	AC differential Input cross point voltage: The voltage at which the differential input signals must cross.

Document Revision History for the Intel MAX 10 FPGA Device Datasheet

Document Version	Changes
2018.06.29	• Removed links on instant-on feature. • Added JTAG timing specifications term in *Glossary*. • Renamed the following IP cores as per Intel rebranding: — Renamed Altera Modular ADC IP core to Modular ADC core Intel FPGA IP core. — Renamed Altera Modular Dual ADC IP core to Modular Dual ADC core Intel FPGA IP core.

Date	Version	Changes
		• Added –A6 speed grade in the following tables: — Intel MAX 10 Device Grades and Speed Grades Supported — Series OCT without Calibration Specifications for Intel MAX 10 Devices — Clock Tree Specifications for Intel MAX 10 Devices — Embedded Multiplier Specifications for Intel MAX 10 Devices — Memory Block Performance Specifications for Intel MAX 10 Devices — True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — Emulated RSDS_E_1R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices — IOE Programmable Delay on Row Pins for Intel MAX 10 Devices — IOE Programmable Delay on Column Pins for Intel MAX 10 Devices • Updated the maximum value for input clock cycle-to-cycle jitter ($t_{INJITTER\_CCJ}$) with F_{INPFD} < 100 MHz condition from 750 ps to ±750 ps in PLL Specifications for Intel MAX 10 Devices table. • Updated the dual supply mode performance in Embedded Multiplier Specifications for Intel MAX 10 Devices table. • Updated the dual supply mode performance in Memory Block Performance Specifications for Intel MAX 10 Devices table. • Added typical specifications in Internal Oscillator Frequencies for Intel MAX 10 Devices table. • Updated specifications in UFM Performance Specifications for Intel MAX 10 Devices table. • Updated sampling window specifications in LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices table. • Updated IOE programmable delay for row and column pins. • Changed instances of *Quartus II* to *Quartus Prime*.
June 2015	2015.06.12	• Updated the maximum values in Internal Weak Pull-Up Resistor for Intel MAX 10 Devices table. • Removed Internal Weak Pull-Up Resistor equation. • Updated the note for input resistance and input capacitance parameters in the ADC Performance Specifications table for both single supply and dual supply devices. Note: Download the SPICE models for simulation. • Added a note to AC Accuracy - THD, SNR, and SINAD parameters in the ADC Performance Specifications for Intel MAX 10 Dual Supply Devices table. Note: When using internal V_{REF}, THD = 66 dB, SNR = 58 dB and SINAD = 57.5 dB for dedicated ADC input channels. • Updated clock period jitter and cycle-to-cycle period jitter parameters in the Memory Output Clock Jitter Specifications for Intel MAX 10 Devices table.

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Date	Version	Changes
May 2015	2015.05.04	• Updated a note to V_{CCIO} for both single supply and dual supply power supplies recommended operating conditions tables. Note updated: V_{CCIO} for all I/O banks must be powered up during user mode because V_{CCIO} I/O banks are used for the ADC and I/O functionalities. • Updated Example for OCT Resistance Calculation after Calibration at Device Power-Up. • Removed a note to BLVDS in Differential I/O Standards Specifications for Intel MAX 10 Devices table. BLVDS is now supported in Intel MAX 10 single supply devices. Note removed: BLVDS TX is not supported in single supply devices. • Updated ADC Performance Specifications for both single supply and dual supply devices. — Changed the symbol for Operating junction temperature range parameter from T_A to T_J. — Edited sampling rate maximum value from 1000 kSPS to 1 MSPS. — Added a note to analog input voltage parameter. — Removed input frequency, f_{IN} specification. — Updated the condition for DNL specification: External V_{REF}, no missing code. Added DNL specification for condition: Internal V_{REF}, no missing code. — Added notes to AC accuracy specifications that the value with prescalar enabled is 6dB less than the specification. — Added a note to On-Chip Temperature Sensor (absolute accuracy) parameter about the averaging calculation. • Updated ADC Performance Specifications for Intel MAX 10 Single Supply Devices table. — Added condition for On-Chip Temperature Sensor (absolute accuracy) parameter: with 64 samples averaging. • Updated ADC Performance Specifications for Intel MAX 10 Dual Supply Devices table. — Updated Digital Supply Voltage minimum value from 1.14 V to 1.15 V and maximum value from 1.26 V to 1.25 V. • Updated f_{HSCLK} and HSIODR specifications for –A7 speed grade in the following tables: — True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True LVDS Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices — True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — Emulated LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices — Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — LVDS Receiver Timing Specifications for Intel MAX 10 Single Supply Devices — LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices

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Date	Version	Changes
		• Updated TCCS specifications in the following tables: — True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — Emulated RSDS_E_1R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True LVDS Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices — True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — Emulated LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices — Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices • Updated $t_{x\ Jitter}$ specifications in the following tables: — True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — Emulated RSDS_E_1R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices • Updated SW specifications in LVDS Receiver Timing Specifications for Intel MAX 10 Single Supply Devices table. • Added a note to $t_{x\ Jitter}$ for all LVDS tables. Note: TX jitter is the jitter induced from core noise and I/O switching noise. • Updated the description for t_{LOCK} for all LVDS tables: Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration. • Updated Memory Output Clock Jitter Specifications section. — Updated maximum external memory interfaces frequency from 300 MHz to 303 MHz. — Updated PLL output routing from global clock network to PHY clock network. • Added I/O Timing for Intel MAX 10 Devices table. • Added V_{HYS} in the Glossary table.
January 2015	2015.01.23	• Removed a note to V_{CCA} in Power Supplies Recommended Operating Conditions for Intel MAX 10 Dual Supply Devices table. This note is not valid: All V_{CCA} pins must be connected together for EQFP package. • Corrected the maximum value for $t_{OUTJITTER\_CCJ\_IO}$ ($F_{OUT} \geq 100$ MHz) from 60 ps to 650 ps in PLL Specifications for Intel MAX 10 Devices table.
December 2014	2014.12.15	• Restructured Programming/Erasure Specifications for Intel MAX 10 Devices table to add temperature specifications that affect the data retention duration. • Added statements in the I/O Pin Leakage Current section: Input channel leakage of ADC I/O pins due to hot socket is up to maximum of 1.8 mA. The input channel leakage occurs when the ADC IP core is enabled or disabled. This is applicable to all Intel MAX 10 devices with ADC IP core, which are 10M04, 10M08, 10M16, 10M25, 10M40, and 10M50 devices. The ADC I/O pins are in Bank 1A. • Added a statement in the I/O Standards Specifications section: You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.

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