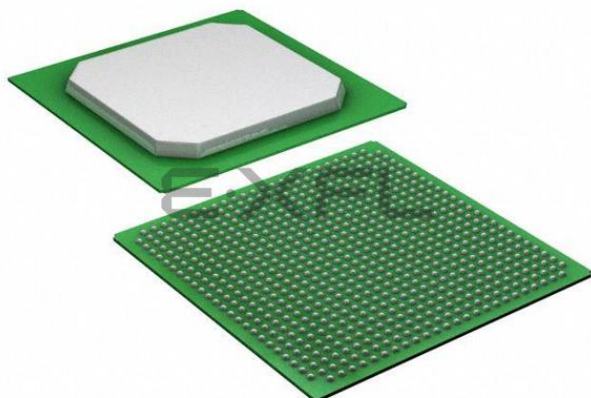




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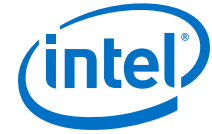
Details

Product Status	Active
Number of LABs/CLBs	2500
Number of Logic Elements/Cells	40000
Total RAM Bits	1290240
Number of I/O	500
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10m40dcf672c7g



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Symbol	Parameter	Min	Max	Unit
V _{CCD_PLL}	Supply voltage for PLL regulator (digital)	-0.5	1.63	V
V _{CCA_ADC}	Supply voltage for ADC analog block	-0.5	3.41	V
V _{CCINT}	Supply voltage for ADC digital block	-0.5	1.63	V

Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings for Intel MAX 10 Devices

Symbol	Parameter	Min	Max	Unit
V _I	DC input voltage	-0.5	4.12	V
I _{OUT}	DC output current per pin	-25	25	mA
T _{STG}	Storage temperature	-65	150	°C
T _J	Operating junction temperature	-40	125	°C

Maximum Allowed Overshoot During Transitions over a 11.4-Year Time Frame

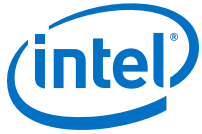
During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 4.17 V can only be at 4.17 V for ~11.7% over the lifetime of the device; for a device lifetime of 11.4 years, this amounts to 1.33 years.

Table 5. Maximum Allowed Overshoot During Transitions over a 11.4-Year Time Frame for Intel MAX 10 Devices

Condition (V)	Overshoot Duration as % of High Time	Unit
4.12	100.0	%
4.17	11.7	%
4.22	7.1	%
4.27	4.3	%
<i>continued...</i>		



Recommended Operating Conditions

Table 8. Recommended Operating Conditions for Intel MAX 10 Devices

Symbol	Parameter	Condition	Min	Max	Unit
V _I	DC input voltage	—	−0.5	3.6	V
V _O	Output voltage for I/O pins	—	0	V _{CCIO}	V
T _J	Operating junction temperature	Commercial	0	85	°C
		Industrial	−40 ⁽⁶⁾	100	°C
		Automotive	−40 ⁽⁶⁾	125	°C
t _{RAMP}	Power supply ramp time	—	(7)	10	ms
I _{Diode}	Magnitude of DC current across PCI* clamp diode when enabled	—	—	10	mA

Programming/Erasure Specifications

Table 9. Programming/Erasure Specifications for Intel MAX 10 Devices

This table shows the programming cycles and data retention duration of the user flash memory (UFM) and configuration flash memory (CFM) blocks.

For more information about data retention duration with 10,000 programming cycles for automotive temperature devices, contact your Intel quality representative.

Erase and reprogram cycles (E/P) ⁽⁸⁾ (Cycles/page)	Temperature (°C)	Data retention duration (Years)
10,000	85	20
10,000	100	10

(6) −40°C is only applicable to Start of Test, when the device is powered-on. The device does not stay at the minimum junction temperature for a long time.

(7) There is no absolute minimum value for the ramp time requirement. Intel characterized the minimum ramp time at 200 µs.

(8) The number of E/P cycles applies to the smallest possible flash block that can be erased or programmed in each Intel MAX 10 device. Each Intel MAX 10 device has multiple flash pages per device.

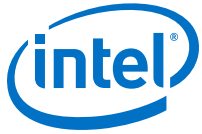


Table 11. ADC_VREF Pin Leakage Current for Intel MAX 10 Devices

Symbol	Parameter	Condition	Min	Max	Unit
I _{adc_vref}	ADC_VREF pin leakage current	Single supply mode	—	10	μA
		Dual supply mode	—	20	μA

Bus Hold Parameters

Bus hold retains the last valid logic state after the source driving it either enters the high impedance state or is removed. Each I/O pin has an option to enable bus hold in user mode. Bus hold is always disabled in configuration mode.

Table 12. Bus Hold Parameters for Intel MAX 10 Devices

Parameter	Condition	V _{CCIO} (V)												Unit
		1.2		1.5		1.8		2.5		3.0		3.3		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold low, sustaining current	V _{IN} > V _{IL} (maximum)	8	—	12	—	30	—	50	—	70	—	70	—	μA
Bus-hold high, sustaining current	V _{IN} < V _{IH} (minimum)	–8	—	–12	—	–30	—	–50	—	–70	—	–70	—	μA
Bus-hold low, overdrive current	0 V < V _{IN} < V _{CCIO}	—	125	—	175	—	200	—	300	—	500	—	500	μA
Bus-hold high, overdrive current	0 V < V _{IN} < V _{CCIO}	—	–125	—	–175	—	–200	—	–300	—	–500	—	–500	μA
Bus-hold trip point	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V



Table 15. OCT Variation after Calibration at Device Power-Up for Intel MAX 10 Devices

This table lists the change percentage of the OCT resistance with voltage and temperature.

Description	Nominal Voltage	dR/dT (%/°C)	dR/dV (%/mV)
OCT variation after calibration at device power-up	3.00	0.25	-0.027
	2.50	0.245	-0.04
	1.80	0.242	-0.079
	1.50	0.235	-0.125
	1.35	0.229	-0.16
	1.20	0.197	-0.208

Figure 1. Equation for OCT Resistance after Calibration at Device Power-Up

$$\Delta R_V = (V_2 - V_1) \times 1000 \times dR/dV$$

$$\Delta R_T = (T_2 - T_1) \times dR/dT$$

$$\text{For } \Delta R_X < 0; MF_X = 1/(|\Delta R_X|/100 + 1)$$

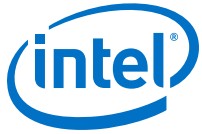
$$\text{For } \Delta R_X > 0; MF_X = \Delta R_X/100 + 1$$

$$MF = MF_V \times MF_T$$

$$R_{final} = R_{initial} \times MF$$

The definitions for equation are as follows:

- T_1 is the initial temperature.
- T_2 is the final temperature.
- MF is multiplication factor.
- $R_{initial}$ is initial resistance.
- R_{final} is final resistance.



Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

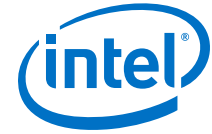
Table 21. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Intel MAX 10 Devices

I/O Standard	V _{CCIO} (V)			V _{REF} (V)			V _{TT} (V) ⁽¹⁴⁾		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	1.19	1.25	1.31	V _{REF} - 0.04	V _{REF}	V _{REF} + 0.04
SSTL-18 Class I, II	1.7	1.8	1.9	0.833	0.9	0.969	V _{REF} - 0.04	V _{REF}	V _{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 × V _{CCIO}	0.5 × V _{CCIO}	0.51 × V _{CCIO}	0.49 × V _{CCIO}	0.5 × V _{CCIO}	0.51 × V _{CCIO}
SSTL-135 Class I, II	1.283	1.35	1.45	0.49 × V _{CCIO}	0.5 × V _{CCIO}	0.51 × V _{CCIO}	0.49 × V _{CCIO}	0.5 × V _{CCIO}	0.51 × V _{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	0.85	0.9	0.95
HSTL-15 Class I, II	1.425	1.5	1.575	0.71	0.75	0.79	0.71	0.75	0.79
HSTL-12 Class I, II	1.14	1.2	1.26	0.48 × V _{CCIO} ⁽¹⁵⁾	0.5 × V _{CCIO} ⁽¹⁵⁾	0.52 × V _{CCIO} ⁽¹⁵⁾	—	0.5 × V _{CCIO}	—
				0.47 × V _{CCIO} ⁽¹⁶⁾	0.5 × V _{CCIO} ⁽¹⁶⁾	0.53 × V _{CCIO} ⁽¹⁶⁾			
HSUL-12	1.14	1.2	1.3	0.49 × V _{CCIO}	0.5 × V _{CCIO}	0.51 × V _{CCIO}	—	—	—

⁽¹⁴⁾ V_{TT} of transmitting device must track V_{REF} of the receiving device.

⁽¹⁵⁾ Value shown refers to DC input reference voltage, V_{REF(DC)}.

⁽¹⁶⁾ Value shown refers to AC input reference voltage, V_{REF(AC)}.



Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications

Table 22. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Intel MAX 10 Devices

To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL-15 Class I specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	$V_{IL(DC)} (V)$		$V_{IH(DC)} (V)$		$V_{IL(AC)} (V)$		$V_{IH(AC)} (V)$		$V_{OL} (V)$	$V_{OH} (V)$	$I_{OL} (mA)$	$I_{OH} (mA)$
	Min	Max	Min	Max	Min	Max	Min	Max	Max	Min		
SSTL-2 Class I	—	$V_{REF} - 0.18$	$V_{REF} + 0.18$	—	—	$V_{REF} - 0.31$	$V_{REF} + 0.31$	—	$V_{TT} - 0.57$	$V_{TT} + 0.57$	8.1	-8.1
SSTL-2 Class II	—	$V_{REF} - 0.18$	$V_{REF} + 0.18$	—	—	$V_{REF} - 0.31$	$V_{REF} + 0.31$	—	$V_{TT} - 0.76$	$V_{TT} + 0.76$	16.4	-16.4
SSTL-18 Class I	—	$V_{REF} - 0.125$	$V_{REF} + 0.125$	—	—	$V_{REF} - 0.25$	$V_{REF} + 0.25$	—	$V_{TT} - 0.475$	$V_{TT} + 0.475$	6.7	-6.7
SSTL-18 Class II	—	$V_{REF} - 0.125$	$V_{REF} + 0.125$	—	—	$V_{REF} - 0.25$	$V_{REF} + 0.25$	—	0.28	$V_{CCIO} - 0.28$	13.4	-13.4
SSTL-15 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	—	$V_{REF} - 0.175$	$V_{REF} + 0.175$	—	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	8	-8
SSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	—	$V_{REF} - 0.175$	$V_{REF} + 0.175$	—	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	16	-16
SSTL-135	—	$V_{REF} - 0.09$	$V_{REF} + 0.09$	—	—	$V_{REF} - 0.16$	$V_{REF} + 0.16$	—	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	—	—
HSTL-18 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	—	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-18 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	—	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-15 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	—	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	—	0.4	$V_{CCIO} - 0.4$	16	-16

continued...



Table 24. Differential HSTL and HSUL I/O Standards Specifications for Intel MAX 10 Devices

I/O Standard	V _{CCIO} (V)			V _{DIF(DC)} (V)		V _{X(AC)} (V)			V _{CM(DC)} (V)			V _{DIF(AC)} (V)
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.85	—	0.95	0.85	—	0.95	0.4
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.71	—	0.79	0.71	—	0.79	0.4
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V _{CCIO}	0.48 × V _{CCIO}	0.5 × V _{CCIO}	0.52 × V _{CCIO}	0.48 × V _{CCIO}	0.5 × V _{CCIO}	0.52 × V _{CCIO}	0.3
HSUL-12	1.14	1.2	1.3	0.26	—	0.5 × V _{CCIO} – 0.12	0.5 × V _{CCIO}	0.5 × V _{CCIO} + 0.12	0.4 × V _{CCIO}	0.5 × V _{CCIO}	0.6 × V _{CCIO}	0.44

Differential I/O Standards Specifications

Table 25. Differential I/O Standards Specifications for Intel MAX 10 Devices

I/O Standard	V _{CCIO} (V)			V _{ID} (mV)		V _{ICM} (V) ⁽¹⁸⁾			V _{OD} (mV) ⁽¹⁹⁾⁽²⁰⁾			V _{OS} (V) ⁽¹⁹⁾		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVPECL ⁽²¹⁾	2.375	2.5	2.625	100	—	0.05	D _{MAX} ≤ 500 Mbps	1.8	—	—	—	—	—	—
						0.55	500 Mbps ≤ D _{MAX} ≤ 700 Mbps	1.8						
						1.05	D _{MAX} > 700 Mbps	1.55						
LVDS	2.375	2.5	2.625	100	—	0.05	D _{MAX} ≤ 500 Mbps	1.8	247	—	600	1.125	1.25	1.375
						0.55	500 Mbps ≤ D _{MAX} ≤ 700 Mbps	1.8						

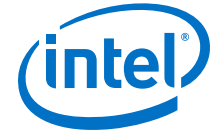
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⁽¹⁸⁾ V_{IN} range: 0 V ≤ V_{IN} ≤ 1.85 V.

⁽¹⁹⁾ R_L range: 90 ≤ R_L ≤ 110 Ω.

⁽²⁰⁾ Low V_{OD} setting is only supported for RSDS standard.

⁽²¹⁾ LVPECL input standard is only supported at clock input. Output standard is not supported.



Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{VCO} ⁽²⁹⁾	PLL internal voltage-controlled oscillator (VCO) operating range	—	600	—	1300	MHz
f_{INDUTY}	Input clock duty cycle	—	40	—	60	%
$t_{INJITTER_CCJ}$ ⁽³⁰⁾	Input clock cycle-to-cycle jitter	$F_{INPFD} \geq 100$ MHz	—	—	0.15	UI
		$F_{INPFD} < 100$ MHz	—	—	±750	ps
f_{OUT_EXT} ⁽²⁸⁾	PLL output frequency for external clock output	—	—	—	472.5	MHz
f_{OUT}	PLL output frequency to global clock	–6 speed grade	—	—	472.5	MHz
		–7 speed grade	—	—	450	MHz
		–8 speed grade	—	—	402.5	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output	Duty cycle set to 50%	45	50	55	%
t_{LOCK}	Time required to lock from end of device configuration	—	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically	After switchover, reconfiguring any non-post-scale counters or delays, or when areset is deasserted	—	—	1	ms
$t_{OUTJITTER_PERIOD_IO}$ ⁽³¹⁾	Regular I/O period jitter	$F_{OUT} \geq 100$ MHz	—	—	650	ps
		$F_{OUT} < 100$ MHz	—	—	75	mUI
$t_{OUTJITTER_CCJ_IO}$ ⁽³¹⁾	Regular I/O cycle-to-cycle jitter	$F_{OUT} \geq 100$ MHz	—	—	650	ps
		$F_{OUT} < 100$ MHz	—	—	75	mUI

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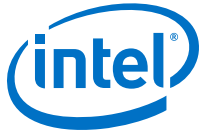
- ⁽²⁹⁾ The VCO frequency reported by the Intel Quartus Prime software in the PLL summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.
- ⁽³⁰⁾ A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source, which is less than 200 ps.
- ⁽³¹⁾ Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied.



Symbol	Parameter	Mode	-I6, -A6, -C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×8	80	—	100	80	—	100	80	—	100	Mbps
		×7	70	—	100	70	—	100	70	—	100	Mbps
		×4	40	—	100	40	—	100	40	—	100	Mbps
		×2	20	—	100	20	—	100	20	—	100	Mbps
		×1	10	—	100	10	—	100	10	—	100	Mbps
t _{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS ⁽⁵⁵⁾	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
t _x Jitter ⁽⁵⁶⁾	Output jitter (high-speed I/O performance pin)	—	—	—	425	—	—	425	—	—	425	ps
	Output jitter (low-speed I/O performance pin)	—	—	—	470	—	—	470	—	—	470	ps
t _{RISE}	Rise time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{FALL}	Fall time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

⁽⁵⁵⁾ TCCS specifications apply to I/O banks from the same side only.

⁽⁵⁶⁾ TX jitter is the jitter induced from core noise and I/O switching noise.



Emulated RSDS_E_1R Transmitter Timing Specifications

Table 39. Emulated RSDS_E_1R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

Emulated **RSDS_E_1R** transmitter is supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	-I6, -A6, -C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{HCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	—	85	5	—	85	5	—	85	MHz
		×8	5	—	85	5	—	85	5	—	85	MHz
		×7	5	—	85	5	—	85	5	—	85	MHz
		×4	5	—	85	5	—	85	5	—	85	MHz
		×2	5	—	85	5	—	85	5	—	85	MHz
		×1	5	—	170	5	—	170	5	—	170	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	—	170	100	—	170	100	—	170	Mbps
		×8	80	—	170	80	—	170	80	—	170	Mbps
		×7	70	—	170	70	—	170	70	—	170	Mbps
		×4	40	—	170	40	—	170	40	—	170	Mbps
		×2	20	—	170	20	—	170	20	—	170	Mbps
		×1	10	—	170	10	—	170	10	—	170	Mbps
f _{HCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	—	85	5	—	85	5	—	85	MHz
		×8	5	—	85	5	—	85	5	—	85	MHz
		×7	5	—	85	5	—	85	5	—	85	MHz
		×4	5	—	85	5	—	85	5	—	85	MHz
		×2	5	—	85	5	—	85	5	—	85	MHz
		×1	5	—	170	5	—	170	5	—	170	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	—	170	100	—	170	100	—	170	Mbps
		×8	80	—	170	80	—	170	80	—	170	Mbps
		×7	70	—	170	70	—	170	70	—	170	Mbps

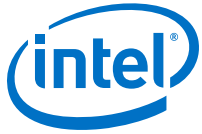
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Symbol	Parameter	Mode	-I6, -A6, -C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×7	70	—	300	70	—	300	70	—	300	Mbps
		×4	40	—	300	40	—	300	40	—	300	Mbps
		×2	20	—	300	20	—	300	20	—	300	Mbps
		×1	10	—	300	10	—	300	10	—	300	Mbps
t _{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS ⁽⁶¹⁾	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
t _{x Jitter} ⁽⁶²⁾	Output jitter (high-speed I/O performance pin)	—	—	—	425	—	—	425	—	—	425	ps
	Output jitter (low-speed I/O performance pin)	—	—	—	470	—	—	470	—	—	470	ps
t _{RISE}	Rise time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{FALL}	Fall time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

⁽⁶¹⁾ TCCS specifications apply to I/O banks from the same side only.

⁽⁶²⁾ TX jitter is the jitter induced from core noise and I/O switching noise.



True LVDS Transmitter Timing

Single Supply Devices True LVDS Transmitter Timing Specifications

Table 41. True LVDS Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices

True LVDS transmitter is only supported at the bottom I/O banks.

Symbol	Parameter	Mode	-C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{HCLK}	Input clock frequency	×10	5	—	145	5	—	100	5	—	100	MHz
		×8	5	—	145	5	—	100	5	—	100	MHz
		×7	5	—	145	5	—	100	5	—	100	MHz
		×4	5	—	145	5	—	100	5	—	100	MHz
		×2	5	—	145	5	—	100	5	—	100	MHz
		×1	5	—	290	5	—	200	5	—	200	MHz
HSIODR	Data rate	×10	100	—	290	100	—	200	100	—	200	Mbps
		×8	80	—	290	80	—	200	80	—	200	Mbps
		×7	70	—	290	70	—	200	70	—	200	Mbps
		×4	40	—	290	40	—	200	40	—	200	Mbps
		×2	20	—	290	20	—	200	20	—	200	Mbps
		×1	10	—	290	10	—	200	10	—	200	Mbps
t _{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS ⁽⁶³⁾	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
t _{x jitter} ⁽⁶⁴⁾	Output jitter	—	—	—	1,000	—	—	1,000	—	—	1,000	ps

continued...

⁽⁶³⁾ TCCS specifications apply to I/O banks from the same side only.

⁽⁶⁴⁾ TX jitter is the jitter induced from core noise and I/O switching noise.

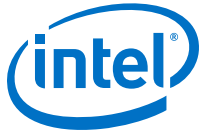


Table 56. I/O Timing for Intel MAX 10 Devices

These I/O timing parameters are for the 3.3-V LVTTTL I/O standard with the maximum drive strength and fast slew rate for 10M08DAF484 device.

Symbol	Parameter	-C7, -I7	-C8	Unit
T _{su}	Global clock setup time	-0.750	-0.808	ns
T _h	Global clock hold time	1.180	1.215	ns
T _{co}	Global clock to output delay	5.131	5.575	ns
T _{pd}	Best case pin-to-pin propagation delay through one LUT	4.907	5.467	ns

Programmable IOE Delay

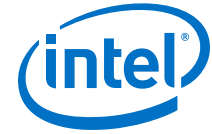
Programmable IOE Delay On Row Pins

Table 57. IOE Programmable Delay on Row Pins for Intel MAX 10 Devices

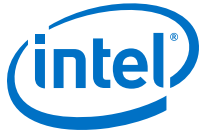
The incremental values for the settings are generally linear. For exact values of each setting, refer to the **Assignment Name** column in the latest version of the Intel Quartus Prime software.

The minimum and maximum offset timing numbers are in reference to setting '0' as available in the Intel Quartus Prime software.

Parameter	Paths Affected	Number of Settings	Minimum Offset	Maximum Offset							Unit
				Fast Corner		Slow Corner					
				−I7	−C8	−A6	−C7	−C8	−I7	−A7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	0.815	0.873	1.831	1.811	1.874	1.871	1.922	ns
Input delay from pin to input register	Pad to I/O input register	8	0	0.924	0.992	2.081	2.055	2.125	2.127	2.185	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.479	0.514	1.069	1.070	1.117	1.105	1.134	ns



Term	Definition
t _{DUTY}	HIGH-SPEED I/O Block: Duty cycle on high-speed transmitter output clock.
t _{FALL}	Signal high-to-low transition time (80–20%).
t _H	Input register hold time.
Timing Unit Interval (TUI)	HIGH-SPEED I/O block: The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t _C /w).
t _{INJITTER}	Period jitter on PLL clock input.
t _{OUTJITTER_DEDCCLK}	Period jitter on dedicated clock output driven by a PLL.
t _{OUTJITTER_IO}	Period jitter on general purpose I/O driven by a PLL.
t _{pllcin}	Delay from PLL inclk pad to I/O input register.
t _{pllcout}	Delay from PLL inclk pad to I/O output register.
t _{RISE}	Signal low-to-high transition time (20–80%).
t _{SU}	Input register setup time.
V _{CM(DC)}	DC common mode input voltage.
V _{DIF(AC)}	AC differential input voltage: The minimum AC input differential voltage required for switching.
V _{DIF(DC)}	DC differential input voltage: The minimum DC input differential voltage required for switching.
V _{HYS}	Hysteresis for Schmitt trigger input.
V _{ICM}	Input common mode voltage: The common mode of the differential signal at the receiver.
V _{ID}	Input differential Voltage Swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
V _{IH}	Voltage input high: The minimum positive voltage applied to the input which is accepted by the device as a logic high.
V _{IH(AC)}	High-level AC input voltage.
V _{IH(DC)}	High-level DC input voltage.
V _{IL}	Voltage input low: The maximum positive voltage applied to the input which is accepted by the device as a logic low.
V _{IL (AC)}	Low-level AC input voltage.
V _{IL (DC)}	Low-level DC input voltage.
V _{IN}	DC input voltage.
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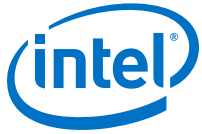


Date	Version	Changes
January 2016	2016.01.22	• Added description about automotive temperature devices in the Programming/Erasure Specifications table. • Changed the pin capacitance to maximum values. • Updated maximum TCCS specifications from 410 ps to 300 ps in the following tables: — True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — Emulated RSDS_E_1R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True LVDS Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices — True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — Emulated LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices — Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices • Added new table: True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices. • Updated maximum f_{HCLK} and HSIODR specifications for -A6, -C7, and -I7 speed grades in True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices table. • Updated SW specifications in the following tables: — LVDS Receiver Timing Specifications for Intel MAX 10 Single Supply Devices — LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices • Updated maximum f_{HCLK} and HSIODR (high-speed I/O performance pin) specifications for -I6, -A6, -C7, -I7 speed grades in LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices table. • Removed Internal Configuration Time information in the Uncompressed .rbf Sizes for Intel MAX 10 Devices table. • Added Internal Configuration Time tables for uncompressed .rbf files and compressed .rbf files. • Removed Preliminary tags for all tables.
November 2015	2015.11.02	• Added description to <i>Maximum Allowed Overshoot During Transitions over a 11.4-Year Time Frame</i> topic. • Added ADC_VREF Pin Leakage Current for Intel MAX 10 Devices table. • Updated the condition for "Bus-hold high, sustaining current" parameter from "$V_{IN} < V_{IL}$ (minimum)" to "$V_{IN} < V_{IH}$ (minimum)" in Bus Hold Parameters table.
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Date	Version	Changes
May 2015	2015.05.04	• Updated a note to V_{CCIO} for both single supply and dual supply power supplies recommended operating conditions tables. Note updated: V_{CCIO} for all I/O banks must be powered up during user mode because V_{CCIO} I/O banks are used for the ADC and I/O functionalities. • Updated Example for OCT Resistance Calculation after Calibration at Device Power-Up. • Removed a note to BLVDS in Differential I/O Standards Specifications for Intel MAX 10 Devices table. BLVDS is now supported in Intel MAX 10 single supply devices. Note removed: BLVDS TX is not supported in single supply devices. • Updated ADC Performance Specifications for both single supply and dual supply devices. — Changed the symbol for Operating junction temperature range parameter from T_A to T_J. — Edited sampling rate maximum value from 1000 kSPS to 1 MSPS. — Added a note to analog input voltage parameter. — Removed input frequency, f_{IN} specification. — Updated the condition for DNL specification: External V_{REF}, no missing code. Added DNL specification for condition: Internal V_{REF}, no missing code. — Added notes to AC accuracy specifications that the value with prescaler enabled is 6dB less than the specification. — Added a note to On-Chip Temperature Sensor (absolute accuracy) parameter about the averaging calculation. • Updated ADC Performance Specifications for Intel MAX 10 Single Supply Devices table. — Added condition for On-Chip Temperature Sensor (absolute accuracy) parameter: with 64 samples averaging. • Updated ADC Performance Specifications for Intel MAX 10 Dual Supply Devices table. — Updated Digital Supply Voltage minimum value from 1.14 V to 1.15 V and maximum value from 1.26 V to 1.25 V. • Updated f_{HCLK} and HSIODR specifications for –A7 speed grade in the following tables: — True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True LVDS Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices — True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — Emulated LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices — Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — LVDS Receiver Timing Specifications for Intel MAX 10 Single Supply Devices — LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices

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Date	Version	Changes
		- Updated SSTL-2 Class I and II I/O standard specifications for JEDEC compliance as follows: - VIL(AC) Max: Updated from $V_{REF} - 0.35$ to $V_{REF} - 0.31$ - VIH(AC) Min: Updated from $V_{REF} + 0.35$ to $V_{REF} + 0.31$ - Added a note to BLVDS in Differential I/O Standards Specifications for Intel MAX 10 Devices table: BLVDS TX is not supported in single supply devices. - Added a link to MAX 10 High-Speed LVDS I/O User Guide for the list of I/O standards supported in single supply and dual supply devices. - Added a statement in PLL Specifications for Intel MAX 10 Single Supply Device table: For V36 package, the PLL specification is based on single supply devices. - Added Internal Oscillator Specifications from Intel MAX 10 Clocking and PLL User Guide. - Added UFM specifications for serial interface. - Updated total harmonic distortion (THD) specifications as follows: - Single supply devices: Updated from 65 dB to -65 dB - Dual supply devices: Updated from 70 dB to -70 dB (updated from 65 dB to -65 dB for dual function pin) - Added condition for On-Chip Temperature Sensor—Absolute accuracy parameter in ADC Performance Specifications for Intel MAX 10 Dual Supply Devices table. The condition is: with 64 samples averaging. - Updated the description in Periphery Performance Specifications to mention that proper timing closure is required in design. - Updated HSIODR and f_{HCLK} specifications for x10 and x7 modes in True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices. - Added specifications for low-speed I/O performance pin sampling window in LVDS Receiver Timing Specifications for Intel MAX 10 Single Supply Devices table: Max = 900 ps for -C7, -I7, -A7, and -C8 speed grades. - Added $t_{RU_nCONFIG}$ and $t_{RU_nRSTIMER}$ specifications for different devices in Remote System Upgrade Circuitry Timing Specifications for Intel MAX 10 Devices table. - Removed the word "internal oscillator" in User Watchdog Timer Specifications for Intel MAX 10 Devices table to avoid confusion. - Added IOE programmable delay specifications.
September 2014	2014.09.22	Initial release.