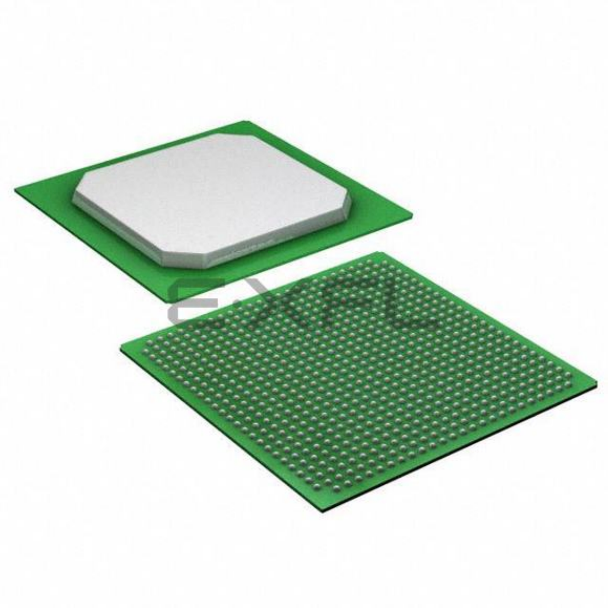
Intel - 10M40DCF672I7G Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	2500
Number of Logic Elements/Cells	40000
Total RAM Bits	1290240
Number of I/O	500
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10m40dcf672i7g

Contents

DC Characteristics

Supply Current and Power Consumption

Intel offers two ways to estimate power for your design—the Excel-based Early Power Estimator (EPE) and the Intel Quartus Prime Power Analyzer feature.

Use the Excel-based EPE before you start your design to estimate the supply current for your design. The EPE provides a magnitude estimate of the device power because these currents vary greatly with the usage of the resources.

The Intel Quartus Prime Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yield very accurate power estimates.

Related Information

- Early Power Estimator User Guide
  Provides more information about power estimation tools.
- Power Analysis chapter, Intel Quartus Prime Handbook
  Provides more information about power estimation tools.

I/O Pin Leakage Current

The values in the table are specified for normal device operation. The values vary during device power-up. This applies for all V_{CCIO} settings (3.3, 3.0, 2.5, 1.8, 1.5, 1.35, and 1.2 V).

10 µA I/O leakage current limit is applicable when the internal clamping diode is off. A higher current can be the observed when the diode is on.

Input channel leakage of ADC I/O pins due to hot socket is up to maximum of 1.8 mA. The input channel leakage occurs when the ADC IP core is enabled or disabled. This is applicable to all Intel MAX 10 devices with ADC IP core, which are 10M04, 10M08, 10M16, 10M25, 10M40, and 10M50 devices. The ADC I/O pins are in Bank 1A.

Table 10. I/O Pin Leakage Current for Intel MAX 10 Devices

Symbol	Parameter	Condition	Min	Max	Unit
I_I	Input pin leakage current	V_I = 0 V to $V_{CCIOMAX}$	−10	10	µA
I_{OZ}	Tristated I/O pin leakage current	V_O = 0 V to $V_{CCIOMAX}$	−10	10	µA

Table 11. ADC_VREF Pin Leakage Current for Intel MAX 10 Devices

Symbol	Parameter	Condition	Min	Max	Unit
I_{adc_vref}	ADC_VREF pin leakage current	Single supply mode	—	10	µA
		Dual supply mode	—	20	µA

Bus Hold Parameters

Bus hold retains the last valid logic state after the source driving it either enters the high impedance state or is removed. Each I/O pin has an option to enable bus hold in user mode. Bus hold is always disabled in configuration mode.

Table 12. Bus Hold Parameters for Intel MAX 10 Devices

Parameter	Condition	V_{CCIO} (V)												Unit
		1.2		1.5		1.8		2.5		3.0		3.3		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold low, sustaining current	$V_{IN} > V_{IL}$ (maximum)	8	—	12	—	30	—	50	—	70	—	70	—	µA
Bus-hold high, sustaining current	$V_{IN} < V_{IH}$ (minimum)	–8	—	–12	—	–30	—	–50	—	–70	—	–70	—	µA
Bus-hold low, overdrive current	$0 V < V_{IN} < V_{CCIO}$	—	125	—	175	—	200	—	300	—	500	—	500	µA
Bus-hold high, overdrive current	$0 V < V_{IN} < V_{CCIO}$	—	–125	—	–175	—	–200	—	–300	—	–500	—	–500	µA
Bus-hold trip point	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

Series OCT without Calibration Specifications

Table 13. Series OCT without Calibration Specifications for Intel MAX 10 Devices

This table shows the variation of on-chip termination (OCT) without calibration across process, voltage, and temperature (PVT).

Description	V_{CCIO} (V)	Resistance Tolerance		Unit
		–C7, –I6, –I7, –A6, –A7	–C8	
Series OCT without calibration	3.00	±35	±30	%
	2.50	±35	±30	%
	1.80	±40	±35	%
	1.50	±40	±40	%
	1.35	±40	±50	%
	1.20	±45	±60	%

Series OCT with Calibration at Device Power-Up Specifications

Table 14. Series OCT with Calibration at Device Power-Up Specifications for Intel MAX 10 Devices

OCT calibration is automatically performed at device power-up for OCT enabled I/Os.

Description	V_{CCIO} (V)	Calibration Accuracy	Unit
Series OCT with calibration at device power-up	3.00	±12	%
	2.50	±12	%
	1.80	±12	%
	1.50	±12	%
	1.35	±12	%
	1.20	±12	%

OCT Variation after Calibration at Device Power-Up

The OCT resistance may vary with the variation of temperature and voltage after calibration at device power-up.

Use the following table and equation to determine the final OCT resistance considering the variations after calibration at device power-up.

Table 15. OCT Variation after Calibration at Device Power-Up for Intel MAX 10 Devices

This table lists the change percentage of the OCT resistance with voltage and temperature.

Description	Nominal Voltage	dR/dT (%/°C)	dR/dV (%/mV)
OCT variation after calibration at device power-up	3.00	0.25	–0.027
	2.50	0.245	–0.04
	1.80	0.242	–0.079
	1.50	0.235	–0.125
	1.35	0.229	–0.16
	1.20	0.197	–0.208

Figure 1. Equation for OCT Resistance after Calibration at Device Power-Up

$$\Delta R_V = (V_2 - V_1) \times 1000 \times dR/dV$$

$$\Delta R_T = (T_2 - T_1) \times dR/dT$$

$$\text{For } \Delta R_X < 0; MF_X = 1/(|\Delta R_X|/100 + 1)$$

$$\text{For } \Delta R_X > 0; MF_X = \Delta R_X/100 + 1$$

$$MF = MF_V \times MF_T$$

$$R_{final} = R_{initial} \times MF$$

The definitions for equation are as follows:

- T_1 is the initial temperature.
- T_2 is the final temperature.
- MF is multiplication factor.
- $R_{initial}$ is initial resistance.
- R_{final} is final resistance.

- Subscript x refers to both V and T.
- ΔR_V is variation of resistance with voltage.
- ΔR_T is variation of resistance with temperature.
- dR/dT is the change percentage of resistance with temperature after calibration at device power-up.
- dR/dV is the change percentage of resistance with voltage after calibration at device power-up.
- V_1 is the initial voltage.
- V_2 is final voltage.

The following figure shows the example to calculate the change of 50 Ω I/O impedance from 25°C at 3.0 V to 85°C at 3.15 V.

Figure 2. Example for OCT Resistance Calculation after Calibration at Device Power-Up

$$\Delta R_V = (3.15 - 3) \times 1000 \ \times -0.027 = -4.05$$

$$\Delta R_T = (85 - 25) \times 0.25 = 15$$

Because ΔR_V is negative,

$$MF_V = 1/(4.05/100 + 1) = 0.961$$

Because ΔR_T is positive,

$$MF_T = 15/100 + 1 = 1.15$$

$$MF = 0.961 \times 1.15 = 1.105$$

$$R_{final} = 50 \times 1.105 = 55.25\Omega$$

Table 24. Differential HSTL and HSUL I/O Standards Specifications for Intel MAX 10 Devices

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.85	—	0.95	0.85	—	0.95	0.4
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.71	—	0.79	0.71	—	0.79	0.4
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO}	0.48 × V_{CCIO}	0.5 × V_{CCIO}	0.52 × V_{CCIO}	0.48 × V_{CCIO}	0.5 × V_{CCIO}	0.52 × V_{CCIO}	0.3
HSUL-12	1.14	1.2	1.3	0.26	—	0.5 × V_{CCIO} – 0.12	0.5 × V_{CCIO}	0.5 × V_{CCIO} + 0.12	0.4 × V_{CCIO}	0.5 × V_{CCIO}	0.6 × V_{CCIO}	0.44

Differential I/O Standards Specifications

Table 25. Differential I/O Standards Specifications for Intel MAX 10 Devices

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)		V_{ICM} (V) (18)			V_{OD} (mV) (19)(20)			V_{OS} (V) (19)		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVPECL (21)	2.375	2.5	2.625	100	—	0.05	D_{MAX} ≤ 500 Mbps	1.8	—	—	—	—	—	—
						0.55	500 Mbps ≤ D_{MAX} ≤ 700 Mbps	1.8						
						1.05	D_{MAX} > 700 Mbps	1.55						
LVDS	2.375	2.5	2.625	100	—	0.05	D_{MAX} ≤ 500 Mbps	1.8	247	—	600	1.125	1.25	1.375
						0.55	500 Mbps ≤ D_{MAX} ≤ 700 Mbps	1.8						

continued...

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(18) V_{IN} range: 0 V ≤ V_{IN} ≤ 1.85 V.

(19) R_L range: 90 ≤ R_L ≤ 110 Ω.

(20) Low V_{OD} setting is only supported for RSDS standard.

(21) LVPECL input standard is only supported at clock input. Output standard is not supported.

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)		V_{ICM} (V) [18]			V_{OD} (mV) [19][20]			V_{OS} (V) [19]		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
HiSpi	2.375	2.5	2.625	100	—	0.05	$D_{MAX} \leq$ 500 Mbps	1.8	—	—	—	—	—	—
						0.55	500 Mbps $\leq D_{MAX} \leq$ 700 Mbps	1.8						
						1.05	$D_{MAX} >$ 700 Mbps	1.55						

Related Information

Intel MAX 10 LVDS SERDES I/O Standards Support, Intel MAX 10 High-Speed LVDS I/O User Guide
Provides the list of I/O standards supported in single supply and dual supply devices.

Switching Characteristics

This section provides the performance characteristics of Intel MAX 10 core and periphery blocks.

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(18) V_{IN} range: 0 V ≤ V_{IN} ≤ 1.85 V.

(19) R_L range: 90 ≤ R_L ≤ 110 Ω.

(20) Low V_{OD} setting is only supported for RSDS standard.

(22) No fixed V_{IN} , V_{OD} , and V_{OS} specifications for Bus LVDS (BLVDS). They are dependent on the system topology.

(23) Mini-LVDS, RSDS, and Point-to-Point Differential Signaling (PPDS) standards are only supported at the output pins for Intel MAX 10 devices.

(24) Supported with requirement of an external level shift

(25) Sub-LVDS input buffer is using 2.5 V differential buffer.

(26) Differential output depends on the values of the external termination resistors.

(27) Differential output offset voltage depends on the values of the external termination resistors.

Embedded Multiplier Specifications

Table 30. Embedded Multiplier Specifications for Intel MAX 10 Devices

Mode	Number of Multipliers	Power Supply Mode	Performance			Unit
			–I6	–A6, –C7, –I7, –A7	–C8	
9 × 9-bit multiplier	1	Single supply mode	198	183	160	MHz
		Dual supply mode	310	260	210	MHz
18 × 18-bit multiplier	1	Single supply mode	198	183	160	MHz
		Dual supply mode	265	240	190	MHz

Memory Block Performance Specifications

Table 31. Memory Block Performance Specifications for Intel MAX 10 Devices

Memory	Mode	Resources Used		Power Supply Mode	Performance			Unit
		LEs	M9K Memory		–I6	–A6, –C7, –I7, –A7	–C8	
M9K Block	FIFO 256 × 36	47	1	Single supply mode	232	219	204	MHz
				Dual supply mode	330	300	250	MHz
	Single-port 256 × 36	0	1	Single supply mode	232	219	204	MHz
				Dual supply mode	330	300	250	MHz
	Simple dual-port 256 × 36 CLK	0	1	Single supply mode	232	219	204	MHz
				Dual supply mode	330	300	250	MHz
	True dual port 512 × 18 single CLK	0	1	Single supply mode	232	219	204	MHz
				Dual supply mode	330	300	250	MHz

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Conversion Rate (52)	Conversion time	—	Single measurement	—	—	1	Cycle
			Continuous measurement	—	—	1	Cycle
			Temperature measurement	—	—	1	Cycle

Related Information

SPICE Models for Intel FPGAs

Periphery Performance Specifications

This section describes the periphery performance, high-speed I/O, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specifications

For more information about the high-speed and low-speed I/O performance pins, refer to the respective device pin-out files.

Related Information

Documentation: Pin-Out Files for Intel FPGAs

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(52) For more detailed description, refer to the Timing section in the *Intel MAX 10 Analog-to-Digital Converter User Guide*.

Emulated RSDS_E_1R Transmitter Timing Specifications

Table 39. Emulated RSDS_E_1R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

Emulated **RSDS_E_1R** transmitter is supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	—	85	5	—	85	5	—	85	MHz
		×8	5	—	85	5	—	85	5	—	85	MHz
		×7	5	—	85	5	—	85	5	—	85	MHz
		×4	5	—	85	5	—	85	5	—	85	MHz
		×2	5	—	85	5	—	85	5	—	85	MHz
		×1	5	—	170	5	—	170	5	—	170	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	—	170	100	—	170	100	—	170	Mbps
		×8	80	—	170	80	—	170	80	—	170	Mbps
		×7	70	—	170	70	—	170	70	—	170	Mbps
		×4	40	—	170	40	—	170	40	—	170	Mbps
		×2	20	—	170	20	—	170	20	—	170	Mbps
		×1	10	—	170	10	—	170	10	—	170	Mbps
f_{HSCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	—	85	5	—	85	5	—	85	MHz
		×8	5	—	85	5	—	85	5	—	85	MHz
		×7	5	—	85	5	—	85	5	—	85	MHz
		×4	5	—	85	5	—	85	5	—	85	MHz
		×2	5	—	85	5	—	85	5	—	85	MHz
		×1	5	—	170	5	—	170	5	—	170	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	—	170	100	—	170	100	—	170	Mbps
		×8	80	—	170	80	—	170	80	—	170	Mbps
		×7	70	—	170	70	—	170	70	—	170	Mbps

continued...

True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications

Table 40. True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

True **mini-LVDS** transmitter is only supported at the bottom I/O banks. Emulated **mini-LVDS_E_3R** transmitter is supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	—	155	5	—	155	5	—	155	MHz
		×8	5	—	155	5	—	155	5	—	155	MHz
		×7	5	—	155	5	—	155	5	—	155	MHz
		×4	5	—	155	5	—	155	5	—	155	MHz
		×2	5	—	155	5	—	155	5	—	155	MHz
		×1	5	—	310	5	—	310	5	—	310	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	—	310	100	—	310	100	—	310	Mbps
		×8	80	—	310	80	—	310	80	—	310	Mbps
		×7	70	—	310	70	—	310	70	—	310	Mbps
		×4	40	—	310	40	—	310	40	—	310	Mbps
		×2	20	—	310	20	—	310	20	—	310	Mbps
		×1	10	—	310	10	—	310	10	—	310	Mbps
f_{HSCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	—	150	5	—	150	5	—	150	MHz
		×8	5	—	150	5	—	150	5	—	150	MHz
		×7	5	—	150	5	—	150	5	—	150	MHz
		×4	5	—	150	5	—	150	5	—	150	MHz
		×2	5	—	150	5	—	150	5	—	150	MHz
		×1	5	—	300	5	—	300	5	—	300	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	—	300	100	—	300	100	—	300	Mbps
		×8	80	—	300	80	—	300	80	—	300	Mbps

continued...

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×7	70	—	300	70	—	300	70	—	300	Mbps
		×4	40	—	300	40	—	300	40	—	300	Mbps
		×2	20	—	300	20	—	300	20	—	300	Mbps
		×1	10	—	300	10	—	300	10	—	300	Mbps
t_{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS(61)	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
$t_{x\ Jitter}$(62)	Output jitter (high-speed I/O performance pin)	—	—	—	425	—	—	425	—	—	425	ps
	Output jitter (low-speed I/O performance pin)	—	—	—	470	—	—	470	—	—	470	ps
t_{RISE}	Rise time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	Fall time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	Time required for the PLL to lock, after `CONF_DONE` signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

---

(61) TCCS specifications apply to I/O banks from the same side only.

(62) TX jitter is the jitter induced from core noise and I/O switching noise.

Symbol	Parameter	Mode	–I6			–A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×1	10	—	360	10	—	350	10	—	320	10	—	320	Mbps
t_{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	45	—	55	%
TCCS(65)	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	—	—	300	ps
$t_{x\ Jitter}$(66)	Output jitter	—	—	—	380	—	—	380	—	—	380	—	—	380	ps
t_{RISE}	Rise time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	Fall time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	Time required for the PLL to lock, after `CONF_DONE` signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	—	—	1	ms

---

(65) TCCS specifications apply to I/O banks from the same side only.

(66) TX jitter is the jitter induced from core noise and I/O switching noise.

LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications

Single Supply Devices LVDS Receiver Timing Specifications

Table 45. LVDS Receiver Timing Specifications for Intel MAX 10 Single Supply Devices

LVDS receivers are supported at all banks.

Symbol	Parameter	Mode	–C7, –I7		–A7		–C8		Unit
			Min	Max	Min	Max	Min	Max	
f_{HSCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	145	5	100	5	100	MHz
		×8	5	145	5	100	5	100	MHz
		×7	5	145	5	100	5	100	MHz
		×4	5	145	5	100	5	100	MHz
		×2	5	145	5	100	5	100	MHz
		×1	5	290	5	200	5	200	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	290	100	200	100	200	Mbps
		×8	80	290	80	200	80	200	Mbps
		×7	70	290	70	200	70	200	Mbps
		×4	40	290	40	200	40	200	Mbps
		×2	20	290	20	200	20	200	Mbps
		×1	10	290	10	200	10	200	Mbps
f_{HSCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	100	5	100	5	100	MHz
		×8	5	100	5	100	5	100	MHz
		×7	5	100	5	100	5	100	MHz
		×4	5	100	5	100	5	100	MHz
		×2	5	100	5	100	5	100	MHz
		×1	5	200	5	200	5	200	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	200	100	200	100	200	Mbps

continued...

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7		–A7		–C8		Unit
			Min	Max	Min	Max	Min	Max	
		×2	5	360	5	320	5	320	MHz
		×1	5	360	5	320	5	320	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	700	100	640	100	640	Mbps
		×8	80	720	80	640	80	640	Mbps
		×7	70	700	70	640	70	640	Mbps
		×4	40	720	40	640	40	640	Mbps
		×2	20	720	20	640	20	640	Mbps
		×1	10	360	10	320	10	320	Mbps
f_{HSCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	150	5	150	5	150	MHz
		×8	5	150	5	150	5	150	MHz
		×7	5	150	5	150	5	150	MHz
		×4	5	150	5	150	5	150	MHz
		×2	5	150	5	150	5	150	MHz
		×1	5	300	5	300	5	300	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	300	100	300	100	300	Mbps
		×8	80	300	80	300	80	300	Mbps
		×7	70	300	70	300	70	300	Mbps
		×4	40	300	40	300	40	300	Mbps
		×2	20	300	20	300	20	300	Mbps
		×1	10	300	10	300	10	300	Mbps
SW	Sampling window (high-speed I/O performance pin)	—	—	510	—	510	—	510	ps

continued...

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7		–A7		–C8		Unit
			Min	Max	Min	Max	Min	Max	
	Sampling window (low-speed I/O performance pin)	—	—	910	—	910	—	910	ps
$t_{x\ Jitter}$(72)	Input jitter	—	—	500	—	500	—	500	ps
t_{LOCK}	Time required for the PLL to lock, after `CONF_DONE` signal goes high, indicating the completion of device configuration	—	—	1	—	1	—	1	ms

Memory Standards Supported by the Soft Memory Controller

Table 47. Memory Standards Supported by the Soft Memory Controller for Intel MAX 10 Devices

Contact your local sales representatives for access to the -I6 or -A6 speed grade devices in the Intel Quartus Prime software.

External Memory Interface Standard	Rate Support	Speed Grade	Voltage (V)	Max Frequency (MHz)
DDR3 SDRAM	Half	–I6	1.5	303
DDR3L SDRAM	Half	–I6	1.35	303
DDR2 SDRAM	Half	–I6	1.8	200
		–I7 and –C7		167
LPDDR2(73)	Half	–I6	1.2	200(74)

Related Information

External Memory Interface Spec Estimator
Provides the specific details of the memory standards supported.

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(72) TX jitter is the jitter induced from core noise and I/O switching noise.

(73) Intel MAX 10 devices support only single-die LPDDR2.

(74) To achieve the specified performance, constrain the memory device I/O and core power supply variation to within ±3%. By default, the frequency is 167 MHz.

Device	CFM Data Size (bits)	
	Without Memory Initialization	With Memory Initialization
10M25	4,140,000	4,780,000
10M40	7,840,000	9,670,000
10M50	7,840,000	9,670,000

Internal Configuration Time

The internal configuration time measurement is from the rising edge of nSTATUS signal to the rising edge of `CONF_DONE` signal.

Table 53. Internal Configuration Time for Intel MAX 10 Devices (Uncompressed .rbf)

Device	Internal Configuration Time (ms)							
	Unencrypted				Encrypted			
	Without Memory Initialization		With Memory Initialization		Without Memory Initialization		With Memory Initialization	
	Min	Max	Min	Max	Min	Max	Min	Max
10M02	0.3	1.7	—	—	1.7	5.4	—	—
10M04	0.6	2.7	1.0	3.4	5.0	15.0	6.8	19.6
10M08	0.6	2.7	1.0	3.4	5.0	15.0	6.8	19.6
10M16	1.1	3.7	1.4	4.5	9.3	25.3	11.7	31.5
10M25	1.0	3.7	1.3	4.4	14.0	38.1	16.9	45.7
10M40	2.6	6.9	3.2	9.8	41.5	112.1	51.7	139.6
10M50	2.6	6.9	3.2	9.8	41.5	112.1	51.7	139.6

Term	Definition
t_{DUTY}	HIGH-SPEED I/O Block: Duty cycle on high-speed transmitter output clock.
t_{FALL}	Signal high-to-low transition time (80–20%).
t_H	Input register hold time.
Timing Unit Interval (TUI)	HIGH-SPEED I/O block: The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w).
$t_{INJITTER}$	Period jitter on PLL clock input.
$t_{OUTJITTER\_DEDCLK}$	Period jitter on dedicated clock output driven by a PLL.
$t_{OUTJITTER\_IO}$	Period jitter on general purpose I/O driven by a PLL.
t_{pllcin}	Delay from PLL inclk pad to I/O input register.
$t_{pllcout}$	Delay from PLL inclk pad to I/O output register.
t_{RISE}	Signal low-to-high transition time (20–80%).
t_{SU}	Input register setup time.
$V_{CM(DC)}$	DC common mode input voltage.
$V_{DIF(AC)}$	AC differential input voltage: The minimum AC input differential voltage required for switching.
$V_{DIF(DC)}$	DC differential input voltage: The minimum DC input differential voltage required for switching.
V_{HYS}	Hysteresis for Schmitt trigger input.
V_{ICM}	Input common mode voltage: The common mode of the differential signal at the receiver.
V_{ID}	Input differential Voltage Swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
V_{IH}	Voltage input high: The minimum positive voltage applied to the input which is accepted by the device as a logic high.
$V_{IH(AC)}$	High-level AC input voltage.
$V_{IH(DC)}$	High-level DC input voltage.
V_{IL}	Voltage input low: The maximum positive voltage applied to the input which is accepted by the device as a logic low.
$V_{IL\ (AC)}$	Low-level AC input voltage.
$V_{IL\ (DC)}$	Low-level DC input voltage.
V_{IN}	DC input voltage.

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Date	Version	Changes
		• Updated SSTL-2 Class I and II I/O standard specifications for JEDEC compliance as follows: — VIL(AC) Max: Updated from V_{REF} – 0.35 to V_{REF} – 0.31 — VIH(AC) Min: Updated from V_{REF} + 0.35 to V_{REF} + 0.31 • Added a note to BLVDS in Differential I/O Standards Specifications for Intel MAX 10 Devices table: BLVDS TX is not supported in single supply devices. • Added a link to MAX 10 High-Speed LVDS I/O User Guide for the list of I/O standards supported in single supply and dual supply devices. • Added a statement in PLL Specifications for Intel MAX 10 Single Supply Device table: For V36 package, the PLL specification is based on single supply devices. • Added Internal Oscillator Specifications from Intel MAX 10 Clocking and PLL User Guide. • Added UFM specifications for serial interface. • Updated total harmonic distortion (THD) specifications as follows: — Single supply devices: Updated from 65 dB to –65 dB — Dual supply devices: Updated from 70 dB to –70 dB (updated from 65 dB to –65 dB for dual function pin) • Added condition for On-Chip Temperature Sensor—Absolute accuracy parameter in ADC Performance Specifications for Intel MAX 10 Dual Supply Devices table. The condition is: with 64 samples averaging. • Updated the description in Periphery Performance Specifications to mention that proper timing closure is required in design. • Updated HSIODR and f_{HSCLK} specifications for x10 and x7 modes in True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices. • Added specifications for low-speed I/O performance pin sampling window in LVDS Receiver Timing Specifications for Intel MAX 10 Single Supply Devices table: Max = 900 ps for –C7, –I7, –A7, and –C8 speed grades. • Added $t_{RU\_nCONFIG}$ and $t_{RU\_nRSTIMER}$ specifications for different devices in Remote System Upgrade Circuitry Timing Specifications for Intel MAX 10 Devices table. • Removed the word "internal oscillator" in User Watchdog Timer Specifications for Intel MAX 10 Devices table to avoid confusion. • Added IOE programmable delay specifications.
September 2014	2014.09.22	Initial release.