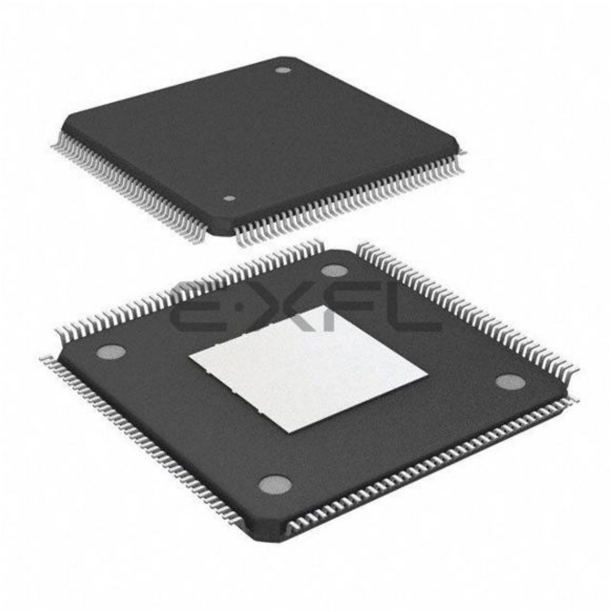
Intel - 10M40SAE144I7G Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	2500
Number of Logic Elements/Cells	40000
Total RAM Bits	1290240
Number of I/O	101
Number of Gates	-
Voltage - Supply	2.85V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	144-EQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10m40sae144i7g

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		1.35 V	1.2825	1.35	1.4175	V
		1.2 V	1.14	1.2	1.26	V
V_{CCA} (1)	Supply voltage for PLL regulator and ADC block (analog)	—	2.85/3.135	3.0/3.3	3.15/3.465	V

Dual Supply Devices Power Supplies Recommended Operating Conditions

Table 7. Power Supplies Recommended Operating Conditions for Intel MAX 10 Dual Supply Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CC}	Supply voltage for core and periphery	—	1.15	1.2	1.25	V
V_{CCIO} (3)	Supply voltage for input and output buffers	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.35 V	1.2825	1.35	1.4175	V
		1.2 V	1.14	1.2	1.26	V
V_{CCA}(4)	Supply voltage for PLL regulator (analog)	—	2.375	2.5	2.625	V
V_{CCD_PLL}(5)	Supply voltage for PLL regulator (digital)	—	1.15	1.2	1.25	V
V_{CCA_ADC}	Supply voltage for ADC analog block	—	2.375	2.5	2.625	V
V_{CCINT}	Supply voltage for ADC digital block	—	1.15	1.2	1.25	V

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(3) V_{CCIO} for all I/O banks must be powered up during user mode because V_{CCIO} I/O banks are used for the ADC and I/O functionalities.

(4) All V_{CCA} pins must be powered to 2.5 V (even when PLLs are not used), and must be powered up and powered down at the same time.

(5) V_{CCD_PLL} must always be connected to V_{CC} through a decoupling capacitor and ferrite bead.

Recommended Operating Conditions

Table 8. Recommended Operating Conditions for Intel MAX 10 Devices

Symbol	Parameter	Condition	Min	Max	Unit
V_I	DC input voltage	—	–0.5	3.6	V
V_O	Output voltage for I/O pins	—	0	V_{CCIO}	V
T_J	Operating junction temperature	Commercial	0	85	°C
		Industrial	–40(6)	100	°C
		Automotive	–40(6)	125	°C
t_{RAMP}	Power supply ramp time	—	(7)	10	ms
I_{Diode}	Magnitude of DC current across PCI* clamp diode when enabled	—	—	10	mA

Programming/Erasure Specifications

Table 9. Programming/Erasure Specifications for Intel MAX 10 Devices

This table shows the programming cycles and data retention duration of the user flash memory (UFM) and configuration flash memory (CFM) blocks.

For more information about data retention duration with 10,000 programming cycles for automotive temperature devices, contact your Intel quality representative.

Erase and reprogram cycles (E/P) (8) (Cycles/page)	Temperature (°C)	Data retention duration (Years)
10,000	85	20
10,000	100	10

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(6) –40°C is only applicable to Start of Test, when the device is powered-on. The device does not stay at the minimum junction temperature for a long time.

(7) There is no absolute minimum value for the ramp time requirement. Intel characterized the minimum ramp time at 200 µs.

(8) The number of E/P cycles applies to the smallest possible flash block that can be erased or programmed in each Intel MAX 10 device. Each Intel MAX 10 device has multiple flash pages per device.

Table 11. ADC_VREF Pin Leakage Current for Intel MAX 10 Devices

Symbol	Parameter	Condition	Min	Max	Unit
I_{adc_vref}	ADC_VREF pin leakage current	Single supply mode	—	10	µA
		Dual supply mode	—	20	µA

Bus Hold Parameters

Bus hold retains the last valid logic state after the source driving it either enters the high impedance state or is removed. Each I/O pin has an option to enable bus hold in user mode. Bus hold is always disabled in configuration mode.

Table 12. Bus Hold Parameters for Intel MAX 10 Devices

Parameter	Condition	V_{CCIO} (V)												Unit
		1.2		1.5		1.8		2.5		3.0		3.3		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold low, sustaining current	$V_{IN} > V_{IL}$ (maximum)	8	—	12	—	30	—	50	—	70	—	70	—	µA
Bus-hold high, sustaining current	$V_{IN} < V_{IH}$ (minimum)	–8	—	–12	—	–30	—	–50	—	–70	—	–70	—	µA
Bus-hold low, overdrive current	$0 V < V_{IN} < V_{CCIO}$	—	125	—	175	—	200	—	300	—	500	—	500	µA
Bus-hold high, overdrive current	$0 V < V_{IN} < V_{CCIO}$	—	–125	—	–175	—	–200	—	–300	—	–500	—	–500	µA
Bus-hold trip point	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

Series OCT without Calibration Specifications

Table 13. Series OCT without Calibration Specifications for Intel MAX 10 Devices

This table shows the variation of on-chip termination (OCT) without calibration across process, voltage, and temperature (PVT).

Description	V_{CCIO} (V)	Resistance Tolerance		Unit
		–C7, –I6, –I7, –A6, –A7	–C8	
Series OCT without calibration	3.00	±35	±30	%
	2.50	±35	±30	%
	1.80	±40	±35	%
	1.50	±40	±40	%
	1.35	±40	±50	%
	1.20	±45	±60	%

Series OCT with Calibration at Device Power-Up Specifications

Table 14. Series OCT with Calibration at Device Power-Up Specifications for Intel MAX 10 Devices

OCT calibration is automatically performed at device power-up for OCT enabled I/Os.

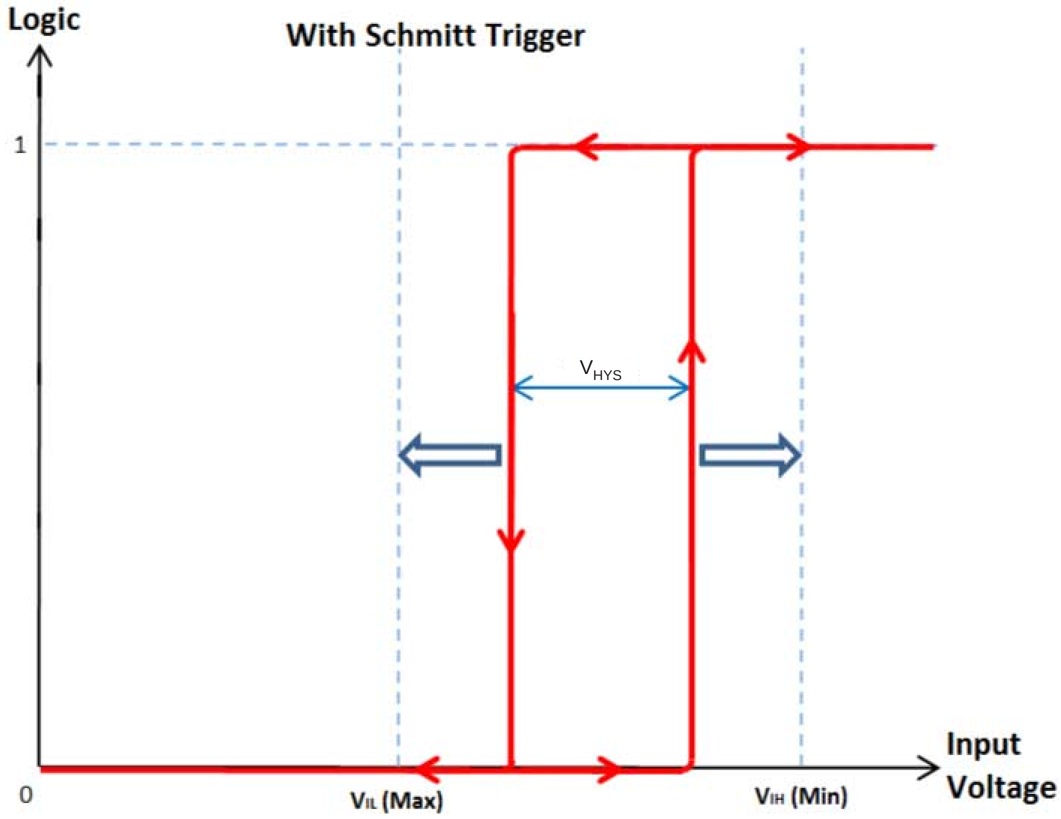
Description	V_{CCIO} (V)	Calibration Accuracy	Unit
Series OCT with calibration at device power-up	3.00	±12	%
	2.50	±12	%
	1.80	±12	%
	1.50	±12	%
	1.35	±12	%
	1.20	±12	%

OCT Variation after Calibration at Device Power-Up

The OCT resistance may vary with the variation of temperature and voltage after calibration at device power-up.

Use the following table and equation to determine the final OCT resistance considering the variations after calibration at device power-up.

Figure 4. Schmitt Trigger Input Standard Voltage Diagram



I/O Standards Specifications

Tables in this section list input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Intel MAX 10 devices.

For minimum voltage values, use the minimum V_{CCIO} values. For maximum voltage values, use the maximum V_{CCIO} values.

You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)		$V_{IH(AC)}$ (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Max	Min	Max	Min	Max	Min	Max	Max	Min		
HSTL-12 Class I	−0.15	V_{REF} − 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	−0.24	V_{REF} − 0.15	V_{REF} + 0.15	V_{CCIO} + 0.24	0.25 × V_{CCIO}	0.75 × V_{CCIO}	8	−8
HSTL-12 Class II	−0.15	V_{REF} − 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	−0.24	V_{REF} − 0.15	V_{REF} + 0.15	V_{CCIO} + 0.24	0.25 × V_{CCIO}	0.75 × V_{CCIO}	14	−14
HSUL-12	—	V_{REF} − 0.13	V_{REF} + 0.13	—	—	V_{REF} − 0.22	V_{REF} + 0.22	—	0.1 × V_{CCIO}	0.9 × V_{CCIO}	—	—

Differential SSTL I/O Standards Specifications

Differential SSTL requires a V_{REF} input.

Table 23. Differential SSTL I/O Standards Specifications for Intel MAX 10 Devices

I/O Standard	V_{CCIO} (V)			$V_{Swing(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{Swing(AC)}$ (V)	
	Min	Typ	Max	Min	Max[17]	Min	Typ	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.36	V_{CCIO}	V_{CCIO}/2 − 0.2	—	V_{CCIO}/2+ 0.2	0.7	V_{CCIO}
SSTL-18 Class I, II	1.7	1.8	1.9	0.25	V_{CCIO}	V_{CCIO}/2 − 0.175	—	V_{CCIO}/2+ 0.175	0.5	V_{CCIO}
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	V_{CCIO}/2 − 0.15	—	V_{CCIO}/2 + 0.15	2($V_{IH(AC)}$ − V_{REF})	2($V_{IL(AC)}$ − V_{REF})
SSTL-135	1.283	1.35	1.45	0.18	—	V_{REF} − 0.135	0.5 × V_{CCIO}	V_{REF} + 0.135	2($V_{IH(AC)}$ − V_{REF})	2($V_{IL(AC)}$ − V_{REF})

Differential HSTL and HSUL I/O Standards Specifications

Differential HSTL requires a V_{REF} input.

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[17] The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	—	±50	ps
t_{ARESET}	Minimum pulse width on areset signal.	—	10	—	—	ns
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for PLLs	—	—	3.5 (32)	—	SCANCLK cycles
$f_{SCANCLK}$	`scanclk` frequency	—	—	—	100	MHz

Table 28. PLL Specifications for Intel MAX 10 Single Supply Devices

For V36 package, the PLL specification is based on single supply devices.

Symbol	Parameter	Condition	Max	Unit
$t_{OUTJITTER\_PERIOD\_DEDCLK}$ (31)	Dedicated clock output period jitter	$F_{OUT} \geq 100$ MHz	660	ps
		$F_{OUT} < 100$ MHz	66	mUI
$t_{OUTJITTER\_CCJ\_DEDCLK}$ (31)	Dedicated clock output cycle-to-cycle jitter	$F_{OUT} \geq 100$ MHz	660	ps
		$F_{OUT} < 100$ MHz	66	mUI

Table 29. PLL Specifications for Intel MAX 10 Dual Supply Devices

Symbol	Parameter	Condition	Max	Unit
$t_{OUTJITTER\_PERIOD\_DEDCLK}$ (31)	Dedicated clock output period jitter	$F_{OUT} \geq 100$ MHz	300	ps
		$F_{OUT} < 100$ MHz	30	mUI
$t_{OUTJITTER\_CCJ\_DEDCLK}$ (31)	Dedicated clock output cycle-to-cycle jitter	$F_{OUT} \geq 100$ MHz	300	ps
		$F_{OUT} < 100$ MHz	30	mUI

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(32) With 100 MHz `scanclk` frequency.

Parameter		Symbol	Condition	Min	Typ	Max	Unit
	Integral non linearity	INL	—	–2	—	2	LSB
AC Accuracy	Total harmonic distortion	THD	F_{IN} = 50 kHz, F_S = 1 MHz, PLL	–65 (37)	—	—	dB
	Signal-to-noise ratio	SNR	F_{IN} = 50 kHz, F_S = 1 MHz, PLL	54 (38)	—	—	dB
	Signal-to-noise and distortion	SINAD	F_{IN} = 50 kHz, F_S = 1 MHz, PLL	53 (39)	—	—	dB
On-Chip Temperature Sensor	Temperature sampling rate	T_S	—	—	—	50	kSPS
	Absolute accuracy	—	–40 to 125°C, with 64 samples averaging (40)	—	—	±10	°C
Conversion Rate (41)	Conversion time	—	Single measurement	—	—	1	Cycle
			Continuous measurement	—	—	1	Cycle
			Temperature measurement	—	—	1	Cycle

Related Information

SPICE Models for Intel FPGAs

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(37) THD with prescalar enabled is 6dB less than the specification.

(38) SNR with prescalar enabled is 6dB less than the specification.

(39) SINAD with prescalar enabled is 6dB less than the specification.

(40) For the Intel Quartus Prime software version 15.0 and later, Modular ADC Core Intel FPGA IP and Modular Dual ADC Core Intel FPGA IP cores handle the 64 samples averaging. For the Intel Quartus Prime software versions prior to 14.1, you need to implement your own averaging calculation.

(41) For more detailed description, refer to the Timing section in the *Intel MAX 10 Analog-to-Digital Converter User Guide*.

Dual Supply Devices ADC Performance Specifications

Table 35. ADC Performance Specifications for Intel MAX 10 Dual Supply Devices

Parameter		Symbol	Condition	Min	Typ	Max	Unit
ADC resolution		—	—	—	—	12	bits
Analog supply voltage		V_{CCA_ADC}	—	2.375	2.5	2.625	V
Digital supply voltage		V_{CCINT}	—	1.15	1.2	1.25	V
External reference voltage		V_{REF}	—	V_{CCA_ADC} – 0.5	—	V_{CCA_ADC}	V
Sampling rate		F_S	Accumulative sampling rate	—	—	1	MSPS
Operating junction temperature range		T_J	—	–40	25	125	°C
Analog input voltage		V_{IN}	Prescalar disabled	0	—	V_{REF}	V
			Prescalar enabled (42)	0	—	3	V
Analog supply current (DC)		I_{ACC_ADC}	Average current	—	275	450	µA
Digital supply current (DC)		I_{CCINT}	Average current	—	65	150	µA
Input resistance		R_{IN}	—	—	(43)	—	—
Input capacitance		C_{IN}	—	—	(43)	—	—
DC Accuracy	Offset error and drift	E_{offset}	Prescalar disabled	–0.2	—	0.2	%FS
			Prescalar enabled	–0.5	—	0.5	%FS
	Gain error and drift	E_{gain}	Prescalar disabled	–0.5	—	0.5	%FS
			Prescalar enabled	–0.75	—	0.75	%FS
	Differential non linearity	DNL	External V_{REF}, no missing code	–0.9	—	0.9	LSB

continued...

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(42) Prescalar function divides the analog input voltage by half. The analog input handles up to 3 V input for the Intel MAX 10 dual supply devices.

(43) Download the SPICE models for simulation.

Parameter		Symbol	Condition	Min	Typ	Max	Unit
			Internal V_{REF}, no missing code	–1	—	1.7	LSB
	Integral non linearity	INL	—	–2	—	2	LSB
AC Accuracy	Total harmonic distortion	THD	F_{IN} = 50 kHz, F_S = 1 MHz, PLL	–70 (44)(45)(46)	—	—	dB
	Signal-to-noise ratio	SNR	F_{IN} = 50 kHz, F_S = 1 MHz, PLL	62 (47)(48)(46)	—	—	dB
	Signal-to-noise and distortion	SINAD	F_{IN} = 50 kHz, F_S = 1 MHz, PLL	61.5 (49)(50)(46)	—	—	dB
On-Chip Temperature Sensor	Temperature sampling rate	T_S	—	—	—	50	kSPS
	Absolute accuracy	—	–40 to 125°C, with 64 samples averaging (51)	—	—	±5	°C

continued...

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(44) Total harmonic distortion is –65 dB for dual function pin.

(45) THD with prescalar enabled is 6dB less than the specification.

(46) When using internal V_{REF}, THD = 66 dB, SNR = 58 dB and SINAD = 57.5 dB for dedicated ADC input channels.

(47) Signal-to-noise ratio is 54 dB for dual function pin.

(48) SNR with prescalar enabled is 6dB less than the specification.

(49) Signal-to-noise and distortion is 53 dB for dual function pin.

(50) SINAD with prescalar enabled is 6dB less than the specification.

(51) For the Intel Quartus Prime software version 15.0 and later, Modular ADC Core and Modular Dual ADC Core IP cores handle the 64 samples averaging. For the Intel Quartus Prime software versions prior to 14.1, you need to implement your own averaging calculation.

Dual Supply Devices True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications

Table 38. True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

True **RSDS** transmitter is only supported at bottom I/O banks. Emulated **RSDS** transmitter is supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	—	155	5	—	155	5	—	155	MHz
		×8	5	—	155	5	—	155	5	—	155	MHz
		×7	5	—	155	5	—	155	5	—	155	MHz
		×4	5	—	155	5	—	155	5	—	155	MHz
		×2	5	—	155	5	—	155	5	—	155	MHz
		×1	5	—	310	5	—	310	5	—	310	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	—	310	100	—	310	100	—	310	Mbps
		×8	80	—	310	80	—	310	80	—	310	Mbps
		×7	70	—	310	70	—	310	70	—	310	Mbps
		×4	40	—	310	40	—	310	40	—	310	Mbps
		×2	20	—	310	20	—	310	20	—	310	Mbps
		×1	10	—	310	10	—	310	10	—	310	Mbps
f_{HSCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	—	150	5	—	150	5	—	150	MHz
		×8	5	—	150	5	—	150	5	—	150	MHz
		×7	5	—	150	5	—	150	5	—	150	MHz
		×4	5	—	150	5	—	150	5	—	150	MHz
		×2	5	—	150	5	—	150	5	—	150	MHz
		×1	5	—	300	5	—	300	5	—	300	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	—	300	100	—	300	100	—	300	Mbps
		×8	80	—	300	80	—	300	80	—	300	Mbps
		×7	70	—	300	70	—	300	70	—	300	Mbps

continued...

Emulated RSDS_E_1R Transmitter Timing Specifications

Table 39. Emulated RSDS_E_1R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

Emulated **RSDS_E_1R** transmitter is supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	—	85	5	—	85	5	—	85	MHz
		×8	5	—	85	5	—	85	5	—	85	MHz
		×7	5	—	85	5	—	85	5	—	85	MHz
		×4	5	—	85	5	—	85	5	—	85	MHz
		×2	5	—	85	5	—	85	5	—	85	MHz
		×1	5	—	170	5	—	170	5	—	170	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	—	170	100	—	170	100	—	170	Mbps
		×8	80	—	170	80	—	170	80	—	170	Mbps
		×7	70	—	170	70	—	170	70	—	170	Mbps
		×4	40	—	170	40	—	170	40	—	170	Mbps
		×2	20	—	170	20	—	170	20	—	170	Mbps
		×1	10	—	170	10	—	170	10	—	170	Mbps
f_{HSCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	—	85	5	—	85	5	—	85	MHz
		×8	5	—	85	5	—	85	5	—	85	MHz
		×7	5	—	85	5	—	85	5	—	85	MHz
		×4	5	—	85	5	—	85	5	—	85	MHz
		×2	5	—	85	5	—	85	5	—	85	MHz
		×1	5	—	170	5	—	170	5	—	170	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	—	170	100	—	170	100	—	170	Mbps
		×8	80	—	170	80	—	170	80	—	170	Mbps
		×7	70	—	170	70	—	170	70	—	170	Mbps

continued...

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×4	40	—	170	40	—	170	40	—	170	Mbps
		×2	20	—	170	20	—	170	20	—	170	Mbps
		×1	10	—	170	10	—	170	10	—	170	Mbps
t_{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS(59)	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
$t_{x\ Jitter}$(60)	Output jitter (high-speed I/O performance pin)	—	—	—	425	—	—	425	—	—	425	ps
	Output jitter (low-speed I/O performance pin)	—	—	—	470	—	—	470	—	—	470	ps
t_{RISE}	Rise time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	Fall time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	Time required for the PLL to lock, after `CONF_DONE` signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

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(59) TCCS specifications apply to I/O banks from the same side only.

(60) TX jitter is the jitter induced from core noise and I/O switching noise.

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×7	70	—	300	70	—	300	70	—	300	Mbps
		×4	40	—	300	40	—	300	40	—	300	Mbps
		×2	20	—	300	20	—	300	20	—	300	Mbps
		×1	10	—	300	10	—	300	10	—	300	Mbps
t_{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS(69)	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
$t_{x\ Jitter}$(70)	Output jitter (high-speed I/O performance pin)	—	—	—	425	—	—	425	—	—	425	ps
	Output jitter (low-speed I/O performance pin)	—	—	—	470	—	—	470	—	—	470	ps
t_{RISE}	Rise time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	Fall time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	Time required for the PLL to lock, after `CONF_DONE` signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

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(69) TCCS specifications apply to I/O banks from the same side only.

(70) TX jitter is the jitter induced from core noise and I/O switching noise.

LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications

Single Supply Devices LVDS Receiver Timing Specifications

Table 45. LVDS Receiver Timing Specifications for Intel MAX 10 Single Supply Devices

LVDS receivers are supported at all banks.

Symbol	Parameter	Mode	–C7, –I7		–A7		–C8		Unit
			Min	Max	Min	Max	Min	Max	
f_{HSCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	145	5	100	5	100	MHz
		×8	5	145	5	100	5	100	MHz
		×7	5	145	5	100	5	100	MHz
		×4	5	145	5	100	5	100	MHz
		×2	5	145	5	100	5	100	MHz
		×1	5	290	5	200	5	200	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	290	100	200	100	200	Mbps
		×8	80	290	80	200	80	200	Mbps
		×7	70	290	70	200	70	200	Mbps
		×4	40	290	40	200	40	200	Mbps
		×2	20	290	20	200	20	200	Mbps
		×1	10	290	10	200	10	200	Mbps
f_{HSCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	100	5	100	5	100	MHz
		×8	5	100	5	100	5	100	MHz
		×7	5	100	5	100	5	100	MHz
		×4	5	100	5	100	5	100	MHz
		×2	5	100	5	100	5	100	MHz
		×1	5	200	5	200	5	200	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	200	100	200	100	200	Mbps

continued...

Symbol	Parameter	Mode	–C7, –I7		–A7		–C8		Unit
			Min	Max	Min	Max	Min	Max	
		×8	80	200	80	200	80	200	Mbps
		×7	70	200	70	200	70	200	Mbps
		×4	40	200	40	200	40	200	Mbps
		×2	20	200	20	200	20	200	Mbps
		×1	10	200	10	200	10	200	Mbps
SW	Sampling window (high-speed I/O performance pin)	—	—	910	—	910	—	910	ps
	Sampling window (low-speed I/O performance pin)	—	—	1,110	—	1,110	—	1,110	ps
$t_{x\ Jitter}$(71)	Input jitter	—	—	1,000	—	1,000	—	1,000	ps
t_{LOCK}	Time required for the PLL to lock, after `CONF_DONE` signal goes high, indicating the completion of device configuration	—	—	1	—	1	—	1	ms

Dual Supply Devices LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications

Table 46. LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices

LVDS, **TMDS**, **HiSpi**, **SLVS**, and **Sub-LVDS** receivers are supported at all banks.

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7		–A7		–C8		Unit
			Min	Max	Min	Max	Min	Max	
f_{HSCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	350	5	320	5	320	MHz
		×8	5	360	5	320	5	320	MHz
		×7	5	350	5	320	5	320	MHz
		×4	5	360	5	320	5	320	MHz

continued...

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(71) TX jitter is the jitter induced from core noise and I/O switching noise.

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7		–A7		–C8		Unit
			Min	Max	Min	Max	Min	Max	
	Sampling window (low-speed I/O performance pin)	—	—	910	—	910	—	910	ps
$t_{x\ Jitter}$(72)	Input jitter	—	—	500	—	500	—	500	ps
t_{LOCK}	Time required for the PLL to lock, after `CONF_DONE` signal goes high, indicating the completion of device configuration	—	—	1	—	1	—	1	ms

Memory Standards Supported by the Soft Memory Controller

Table 47. Memory Standards Supported by the Soft Memory Controller for Intel MAX 10 Devices

Contact your local sales representatives for access to the -I6 or -A6 speed grade devices in the Intel Quartus Prime software.

External Memory Interface Standard	Rate Support	Speed Grade	Voltage (V)	Max Frequency (MHz)
DDR3 SDRAM	Half	–I6	1.5	303
DDR3L SDRAM	Half	–I6	1.35	303
DDR2 SDRAM	Half	–I6	1.8	200
		–I7 and –C7		167
LPDDR2(73)	Half	–I6	1.2	200(74)

Related Information

External Memory Interface Spec Estimator
Provides the specific details of the memory standards supported.

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(72) TX jitter is the jitter induced from core noise and I/O switching noise.

(73) Intel MAX 10 devices support only single-die LPDDR2.

(74) To achieve the specified performance, constrain the memory device I/O and core power supply variation to within ±3%. By default, the frequency is 167 MHz.

Remote System Upgrade Circuitry Timing Specifications

Table 50. Remote System Upgrade Circuitry Timing Specifications for Intel MAX 10 Devices

Parameter	Device	Minimum	Maximum	Unit
$t_{MAX\_RU\_CLK}$	All	—	40	MHz
$t_{RU\_nCONFIG}$	10M02, 10M04, 10M08, 10M16, 10M25	250	—	ns
	10M40, 10M50	350	—	ns
$t_{RU\_nRSTIMER}$	10M02, 10M04, 10M08, 10M16, 10M25	300	—	ns
	10M40, 10M50	500	—	ns

User Watchdog Internal Circuitry Timing Specifications

Table 51. User Watchdog Timer Specifications for Intel MAX 10 Devices

The specifications are subject to PVT changes.

Parameter	Device	Minimum	Typical	Maximum	Unit
User watchdog frequency	10M02, 10M04, 10M08, 10M16, 10M25	3.4	5.1	7.3	MHz
	10M40, 10M50	2.2	3.3	4.8	MHz

Uncompressed Raw Binary File (.rbf) Sizes

Table 52. Uncompressed .rbf Sizes for Intel MAX 10 Devices

Device	CFM Data Size (bits)	
	Without Memory Initialization	With Memory Initialization
10M02	554,000	—
10M04	1,540,000	1,880,000
10M08	1,540,000	1,880,000
10M16	2,800,000	3,430,000

continued...

Device	CFM Data Size (bits)	
	Without Memory Initialization	With Memory Initialization
10M25	4,140,000	4,780,000
10M40	7,840,000	9,670,000
10M50	7,840,000	9,670,000

Internal Configuration Time

The internal configuration time measurement is from the rising edge of nSTATUS signal to the rising edge of CONF_DONE signal.

Table 53. Internal Configuration Time for Intel MAX 10 Devices (Uncompressed .rbf)

Device	Internal Configuration Time (ms)							
	Unencrypted				Encrypted			
	Without Memory Initialization		With Memory Initialization		Without Memory Initialization		With Memory Initialization	
	Min	Max	Min	Max	Min	Max	Min	Max
10M02	0.3	1.7	—	—	1.7	5.4	—	—
10M04	0.6	2.7	1.0	3.4	5.0	15.0	6.8	19.6
10M08	0.6	2.7	1.0	3.4	5.0	15.0	6.8	19.6
10M16	1.1	3.7	1.4	4.5	9.3	25.3	11.7	31.5
10M25	1.0	3.7	1.3	4.4	14.0	38.1	16.9	45.7
10M40	2.6	6.9	3.2	9.8	41.5	112.1	51.7	139.6
10M50	2.6	6.9	3.2	9.8	41.5	112.1	51.7	139.6

Term	Definition
t_{DUTY}	HIGH-SPEED I/O Block: Duty cycle on high-speed transmitter output clock.
t_{FALL}	Signal high-to-low transition time (80–20%).
t_H	Input register hold time.
Timing Unit Interval (TUI)	HIGH-SPEED I/O block: The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w).
$t_{INJITTER}$	Period jitter on PLL clock input.
$t_{OUTJITTER\_DEDCLK}$	Period jitter on dedicated clock output driven by a PLL.
$t_{OUTJITTER\_IO}$	Period jitter on general purpose I/O driven by a PLL.
t_{pllcin}	Delay from PLL inclk pad to I/O input register.
$t_{pllcout}$	Delay from PLL inclk pad to I/O output register.
t_{RISE}	Signal low-to-high transition time (20–80%).
t_{SU}	Input register setup time.
$V_{CM(DC)}$	DC common mode input voltage.
$V_{DIF(AC)}$	AC differential input voltage: The minimum AC input differential voltage required for switching.
$V_{DIF(DC)}$	DC differential input voltage: The minimum DC input differential voltage required for switching.
V_{HYS}	Hysteresis for Schmitt trigger input.
V_{ICM}	Input common mode voltage: The common mode of the differential signal at the receiver.
V_{ID}	Input differential Voltage Swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
V_{IH}	Voltage input high: The minimum positive voltage applied to the input which is accepted by the device as a logic high.
$V_{IH(AC)}$	High-level AC input voltage.
$V_{IH(DC)}$	High-level DC input voltage.
V_{IL}	Voltage input low: The maximum positive voltage applied to the input which is accepted by the device as a logic low.
$V_{IL\ (AC)}$	Low-level AC input voltage.
$V_{IL\ (DC)}$	Low-level DC input voltage.
V_{IN}	DC input voltage.

continued...