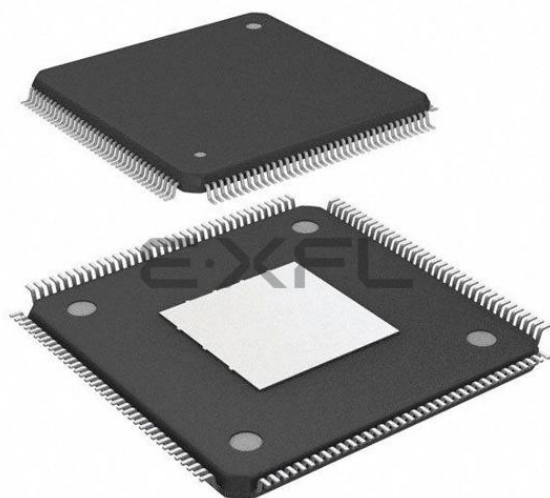




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

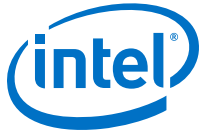
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	2500
Number of Logic Elements/Cells	40000
Total RAM Bits	1290240
Number of I/O	101
Number of Gates	-
Voltage - Supply	2.85V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	144-EQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10m40sce144i7g



Operating Conditions

Intel MAX 10 devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Intel MAX 10 devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions for Intel MAX 10 devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Caution: Conditions outside the range listed in the absolute maximum ratings tables may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Single Supply Devices Absolute Maximum Ratings

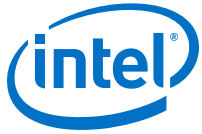
Table 2. Absolute Maximum Ratings for Intel MAX 10 Single Supply Devices

Symbol	Parameter	Min	Max	Unit
V _{CC_ONE}	Supply voltage for core and periphery through on-die voltage regulator	-0.5	3.9	V
V _{CCIO}	Supply voltage for input and output buffers	-0.5	3.9	V
V _{CCA}	Supply voltage for phase-locked loop (PLL) regulator and analog-to-digital converter (ADC) block (analog)	-0.5	3.9	V

Dual Supply Devices Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings for Intel MAX 10 Dual Supply Devices

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply voltage for core and periphery	-0.5	1.63	V
V _{CCIO}	Supply voltage for input and output buffers	-0.5	3.9	V
V _{CCA}	Supply voltage for PLL regulator (analog)	-0.5	3.41	V
continued...				



Condition (V)	Overshoot Duration as % of High Time	Unit
4.32	2.6	%
4.37	1.6	%
4.42	1.0	%
4.47	0.6	%
4.52	0.3	%
4.57	0.2	%

Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Intel MAX 10 devices. The tables list the steady-state voltage values expected from Intel MAX 10 devices. Power supply ramps must all be strictly monotonic, without plateaus.

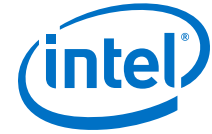
Single Supply Devices Power Supplies Recommended Operating Conditions

Table 6. Power Supplies Recommended Operating Conditions for Intel MAX 10 Single Supply Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{CC_ONE} ⁽¹⁾	Supply voltage for core and periphery through on-die voltage regulator	—	2.85/3.135	3.0/3.3	3.15/3.465	V
V _{CCIO} ⁽²⁾	Supply voltage for input and output buffers	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
continued...						

(1) V_{CCA} must be connected to V_{CC_ONE} through a filter.

(2) V_{CCIO} for all I/O banks must be powered up during user mode because V_{CCIO} I/O banks are used for the ADC and I/O functionalities.



Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{CCA}^{(1)}$	Supply voltage for PLL regulator and ADC block (analog)	1.35 V	1.2825	1.35	1.4175	V
		1.2 V	1.14	1.2	1.26	V
		—	2.85/3.135	3.0/3.3	3.15/3.465	V

Dual Supply Devices Power Supplies Recommended Operating Conditions

Table 7. Power Supplies Recommended Operating Conditions for Intel MAX 10 Dual Supply Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CC}	Supply voltage for core and periphery	—	1.15	1.2	1.25	V
$V_{CCIO}^{(3)}$	Supply voltage for input and output buffers	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.35 V	1.2825	1.35	1.4175	V
		1.2 V	1.14	1.2	1.26	V
$V_{CCA}^{(4)}$	Supply voltage for PLL regulator (analog)	—	2.375	2.5	2.625	V
$V_{CCD_PLL}^{(5)}$	Supply voltage for PLL regulator (digital)	—	1.15	1.2	1.25	V
V_{CCA_ADC}	Supply voltage for ADC analog block	—	2.375	2.5	2.625	V
V_{CCINT}	Supply voltage for ADC digital block	—	1.15	1.2	1.25	V

⁽³⁾ V_{CCIO} for all I/O banks must be powered up during user mode because V_{CCIO} I/O banks are used for the ADC and I/O functionalities.

⁽⁴⁾ All V_{CCA} pins must be powered to 2.5 V (even when PLLs are not used), and must be powered up and powered down at the same time.

⁽⁵⁾ V_{CCD_PLL} must always be connected to V_{CC} through a decoupling capacitor and ferrite bead.



Series OCT without Calibration Specifications

Table 13. Series OCT without Calibration Specifications for Intel MAX 10 Devices

This table shows the variation of on-chip termination (OCT) without calibration across process, voltage, and temperature (PVT).

Description	V _{CCIO} (V)	Resistance Tolerance		Unit
		-C7, -I6, -I7, -A6, -A7	-C8	
Series OCT without calibration	3.00	±35	±30	%
	2.50	±35	±30	%
	1.80	±40	±35	%
	1.50	±40	±40	%
	1.35	±40	±50	%
	1.20	±45	±60	%

Series OCT with Calibration at Device Power-Up Specifications

Table 14. Series OCT with Calibration at Device Power-Up Specifications for Intel MAX 10 Devices

OCT calibration is automatically performed at device power-up for OCT enabled I/Os.

Description	V _{CCIO} (V)	Calibration Accuracy	Unit
Series OCT with calibration at device power-up	3.00	±12	%
	2.50	±12	%
	1.80	±12	%
	1.50	±12	%
	1.35	±12	%
	1.20	±12	%

OCT Variation after Calibration at Device Power-Up

The OCT resistance may vary with the variation of temperature and voltage after calibration at device power-up.

Use the following table and equation to determine the final OCT resistance considering the variations after calibration at device power-up.



Table 15. OCT Variation after Calibration at Device Power-Up for Intel MAX 10 Devices

This table lists the change percentage of the OCT resistance with voltage and temperature.

Description	Nominal Voltage	dR/dT (%/°C)	dR/dV (%/mV)
OCT variation after calibration at device power-up	3.00	0.25	-0.027
	2.50	0.245	-0.04
	1.80	0.242	-0.079
	1.50	0.235	-0.125
	1.35	0.229	-0.16
	1.20	0.197	-0.208

Figure 1. Equation for OCT Resistance after Calibration at Device Power-Up

$$\Delta R_V = (V_2 - V_1) \times 1000 \times dR/dV$$

$$\Delta R_T = (T_2 - T_1) \times dR/dT$$

$$\text{For } \Delta R_X < 0; MF_X = 1/(|\Delta R_X|/100 + 1)$$

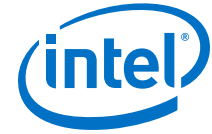
$$\text{For } \Delta R_X > 0; MF_X = \Delta R_X/100 + 1$$

$$MF = MF_V \times MF_T$$

$$R_{final} = R_{initial} \times MF$$

The definitions for equation are as follows:

- T_1 is the initial temperature.
- T_2 is the final temperature.
- MF is multiplication factor.
- $R_{initial}$ is initial resistance.
- R_{final} is final resistance.



- Subscript x refers to both V and T.
- ΔR_V is variation of resistance with voltage.
- ΔR_T is variation of resistance with temperature.
- dR/dT is the change percentage of resistance with temperature after calibration at device power-up.
- dR/dV is the change percentage of resistance with voltage after calibration at device power-up.
- V_1 is the initial voltage.
- V_2 is final voltage.

The following figure shows the example to calculate the change of 50 Ω I/O impedance from 25°C at 3.0 V to 85°C at 3.15 V.

Figure 2. Example for OCT Resistance Calculation after Calibration at Device Power-Up

$$\Delta R_V = (3.15 - 3) \times 1000 \times -0.027 = -4.05$$

$$\Delta R_T = (85 - 25) \times 0.25 = 15$$

Because ΔR_V is negative,

$$MF_V = 1/(4.05/100 + 1) = 0.961$$

Because ΔR_T is positive,

$$MF_T = 15/100 + 1 = 1.15$$

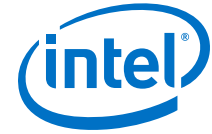
$$MF = 0.961 \times 1.15 = 1.105$$

$$R_{final} = 50 \times 1.105 = 55.25\Omega$$



Table 19. Hysteresis Specifications for Schmitt Trigger Input for Intel MAX 10 Devices

Symbol	Parameter	Condition	Minimum	Unit
V _{HYS}	Hysteresis for Schmitt trigger input	V _{CCIO} = 3.3 V	180	mV
		V _{CCIO} = 2.5 V	150	mV
		V _{CCIO} = 1.8 V	120	mV
		V _{CCIO} = 1.5 V	110	mV



Single-Ended I/O Standards Specifications

Table 20. Single-Ended I/O Standards Specifications for Intel MAX 10 Devices

To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the 3.3-V LVTTTL specification (4 mA), you should set the current strength settings to 4 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3 V LVTTTL	3.135	3.3	3.465	-0.3	0.8	1.7	3.6	0.45	2.4	4	-4
3.3 V LVCMOS	3.135	3.3	3.465	-0.3	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	2	-2
3.0 V LVTTTL	2.85	3	3.15	-0.3	0.8	1.7	$V_{CCIO} + 0.3$	0.45	2.4	4	-4
3.0 V LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	$V_{CCIO} + 0.3$	0.2	$V_{CCIO} - 0.2$	0.1	-0.1
2.5 V LVTTTL and LVCMOS	2.375	2.5	2.625	-0.3	0.7	1.7	$V_{CCIO} + 0.3$	0.4	2	1	-1
1.8 V LVTTTL and LVCMOS	1.71	1.8	1.89	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	2.25	0.45	$V_{CCIO} - 0.45$	2	-2
1.5 V LVCMOS	1.425	1.5	1.575	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2
1.2 V LVCMOS	1.14	1.2	1.26	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2
3.3 V Schmitt Trigger	3.135	3.3	3.465	-0.3	0.8	1.7	$V_{CCIO} + 0.3$	—	—	—	—
2.5 V Schmitt Trigger	2.375	2.5	2.625	-0.3	0.7	1.7	$V_{CCIO} + 0.3$	—	—	—	—
1.8 V Schmitt Trigger	1.71	1.8	1.89	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	—	—	—	—
1.5 V Schmitt Trigger	1.425	1.5	1.575	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	—	—	—	—
3.0 V PCI	2.85	3	3.15	—	$0.3 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	1.5	-0.5



Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

Table 21. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Intel MAX 10 Devices

I/O Standard	V _{CCIO} (V)			V _{REF} (V)			V _{TT} (V) ⁽¹⁴⁾		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	1.19	1.25	1.31	V _{REF} - 0.04	V _{REF}	V _{REF} + 0.04
SSTL-18 Class I, II	1.7	1.8	1.9	0.833	0.9	0.969	V _{REF} - 0.04	V _{REF}	V _{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 × V _{CCIO}	0.5 × V _{CCIO}	0.51 × V _{CCIO}	0.49 × V _{CCIO}	0.5 × V _{CCIO}	0.51 × V _{CCIO}
SSTL-135 Class I, II	1.283	1.35	1.45	0.49 × V _{CCIO}	0.5 × V _{CCIO}	0.51 × V _{CCIO}	0.49 × V _{CCIO}	0.5 × V _{CCIO}	0.51 × V _{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	0.85	0.9	0.95
HSTL-15 Class I, II	1.425	1.5	1.575	0.71	0.75	0.79	0.71	0.75	0.79
HSTL-12 Class I, II	1.14	1.2	1.26	0.48 × V _{CCIO} ⁽¹⁵⁾	0.5 × V _{CCIO} ⁽¹⁵⁾	0.52 × V _{CCIO} ⁽¹⁵⁾	—	0.5 × V _{CCIO}	—
				0.47 × V _{CCIO} ⁽¹⁶⁾	0.5 × V _{CCIO} ⁽¹⁶⁾	0.53 × V _{CCIO} ⁽¹⁶⁾			
HSUL-12	1.14	1.2	1.3	0.49 × V _{CCIO}	0.5 × V _{CCIO}	0.51 × V _{CCIO}	—	—	—

⁽¹⁴⁾ V_{TT} of transmitting device must track V_{REF} of the receiving device.

⁽¹⁵⁾ Value shown refers to DC input reference voltage, V_{REF(DC)}.

⁽¹⁶⁾ Value shown refers to AC input reference voltage, V_{REF(AC)}.



Table 24. Differential HSTL and HSUL I/O Standards Specifications for Intel MAX 10 Devices

I/O Standard	V _{CCIO} (V)			V _{DIF(DC)} (V)		V _{X(AC)} (V)			V _{CM(DC)} (V)			V _{DIF(AC)} (V)
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.85	—	0.95	0.85	—	0.95	0.4
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.71	—	0.79	0.71	—	0.79	0.4
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V _{CCIO}	0.48 × V _{CCIO}	0.5 × V _{CCIO}	0.52 × V _{CCIO}	0.48 × V _{CCIO}	0.5 × V _{CCIO}	0.52 × V _{CCIO}	0.3
HSUL-12	1.14	1.2	1.3	0.26	—	0.5 × V _{CCIO} – 0.12	0.5 × V _{CCIO}	0.5 × V _{CCIO} + 0.12	0.4 × V _{CCIO}	0.5 × V _{CCIO}	0.6 × V _{CCIO}	0.44

Differential I/O Standards Specifications

Table 25. Differential I/O Standards Specifications for Intel MAX 10 Devices

I/O Standard	V _{CCIO} (V)			V _{ID} (mV)		V _{ICM} (V) ⁽¹⁸⁾			V _{OD} (mV) ⁽¹⁹⁾⁽²⁰⁾			V _{OS} (V) ⁽¹⁹⁾		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVPECL ⁽²¹⁾	2.375	2.5	2.625	100	—	0.05	D _{MAX} ≤ 500 Mbps	1.8	—	—	—	—	—	—
						0.55	500 Mbps ≤ D _{MAX} ≤ 700 Mbps	1.8						
						1.05	D _{MAX} > 700 Mbps	1.55						
LVDS	2.375	2.5	2.625	100	—	0.05	D _{MAX} ≤ 500 Mbps	1.8	247	—	600	1.125	1.25	1.375
						0.55	500 Mbps ≤ D _{MAX} ≤ 700 Mbps	1.8						

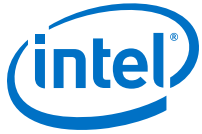
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⁽¹⁸⁾ V_{IN} range: 0 V ≤ V_{IN} ≤ 1.85 V.

⁽¹⁹⁾ R_L range: 90 ≤ R_L ≤ 110 Ω.

⁽²⁰⁾ Low V_{OD} setting is only supported for RSDS standard.

⁽²¹⁾ LVPECL input standard is only supported at clock input. Output standard is not supported.



Core Performance Specifications

Clock Tree Specifications

Table 26. Clock Tree Specifications for Intel MAX 10 Devices

Device	Performance					Unit
	-I6	-A6, -C7	-I7	-A7	-C8	
10M02	450	416	416	382	402	MHz
10M04	450	416	416	382	402	MHz
10M08	450	416	416	382	402	MHz
10M16	450	416	416	382	402	MHz
10M25	450	416	416	382	402	MHz
10M40	450	416	416	382	402	MHz
10M50	450	416	416	382	402	MHz

PLL Specifications

Table 27. PLL Specifications for Intel MAX 10 Devices

V_{CCD_PLL} should always be connected to V_{CCINT} through decoupling capacitor and ferrite bead.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{IN}^{(28)}$	Input clock frequency	—	5	—	472.5	MHz
f_{INPFD}	Phase frequency detector (PFD) input frequency	—	5	—	325	MHz
continued...						

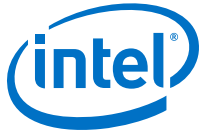
(28) This parameter is limited in the Intel Quartus Prime software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.



Symbol	Parameter	Mode	-I6, -A6, -C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×4	40	—	300	40	—	300	40	—	300	Mbps
		×2	20	—	300	20	—	300	20	—	300	Mbps
		×1	10	—	300	10	—	300	10	—	300	Mbps
t _{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS ⁽⁵⁷⁾	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
t _{x Jitter} ⁽⁵⁸⁾	Output jitter (high-speed I/O performance pin)	—	—	—	425	—	—	425	—	—	425	ps
	Output jitter (low-speed I/O performance pin)	—	—	—	470	—	—	470	—	—	470	ps
t _{RISE}	Rise time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{FALL}	Fall time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

⁽⁵⁷⁾ TCCS specifications apply to I/O banks from the same side only.

⁽⁵⁸⁾ TX jitter is the jitter induced from core noise and I/O switching noise.



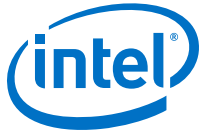
True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications

Table 40. True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

True **mini-LVDS** transmitter is only supported at the bottom I/O banks. Emulated **mini-LVDS_E_3R** transmitter is supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	-I6, -A6, -C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{HSCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	—	155	5	—	155	5	—	155	MHz
		×8	5	—	155	5	—	155	5	—	155	MHz
		×7	5	—	155	5	—	155	5	—	155	MHz
		×4	5	—	155	5	—	155	5	—	155	MHz
		×2	5	—	155	5	—	155	5	—	155	MHz
		×1	5	—	310	5	—	310	5	—	310	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	—	310	100	—	310	100	—	310	Mbps
		×8	80	—	310	80	—	310	80	—	310	Mbps
		×7	70	—	310	70	—	310	70	—	310	Mbps
		×4	40	—	310	40	—	310	40	—	310	Mbps
		×2	20	—	310	20	—	310	20	—	310	Mbps
		×1	10	—	310	10	—	310	10	—	310	Mbps
f _{HSCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	—	150	5	—	150	5	—	150	MHz
		×8	5	—	150	5	—	150	5	—	150	MHz
		×7	5	—	150	5	—	150	5	—	150	MHz
		×4	5	—	150	5	—	150	5	—	150	MHz
		×2	5	—	150	5	—	150	5	—	150	MHz
		×1	5	—	300	5	—	300	5	—	300	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	—	300	100	—	300	100	—	300	Mbps
		×8	80	—	300	80	—	300	80	—	300	Mbps

continued...



True LVDS Transmitter Timing

Single Supply Devices True LVDS Transmitter Timing Specifications

Table 41. True LVDS Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices

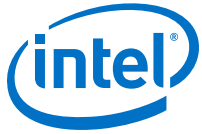
True LVDS transmitter is only supported at the bottom I/O banks.

Symbol	Parameter	Mode	-C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{HCLK}	Input clock frequency	×10	5	—	145	5	—	100	5	—	100	MHz
		×8	5	—	145	5	—	100	5	—	100	MHz
		×7	5	—	145	5	—	100	5	—	100	MHz
		×4	5	—	145	5	—	100	5	—	100	MHz
		×2	5	—	145	5	—	100	5	—	100	MHz
		×1	5	—	290	5	—	200	5	—	200	MHz
HSIODR	Data rate	×10	100	—	290	100	—	200	100	—	200	Mbps
		×8	80	—	290	80	—	200	80	—	200	Mbps
		×7	70	—	290	70	—	200	70	—	200	Mbps
		×4	40	—	290	40	—	200	40	—	200	Mbps
		×2	20	—	290	20	—	200	20	—	200	Mbps
		×1	10	—	290	10	—	200	10	—	200	Mbps
t _{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS ⁽⁶³⁾	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
t _{x jitter} ⁽⁶⁴⁾	Output jitter	—	—	—	1,000	—	—	1,000	—	—	1,000	ps

continued...

⁽⁶³⁾ TCCS specifications apply to I/O banks from the same side only.

⁽⁶⁴⁾ TX jitter is the jitter induced from core noise and I/O switching noise.



Symbol	Parameter	Mode	-I6, -A6, -C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×7	70	—	300	70	—	300	70	—	300	Mbps
		×4	40	—	300	40	—	300	40	—	300	Mbps
		×2	20	—	300	20	—	300	20	—	300	Mbps
		×1	10	—	300	10	—	300	10	—	300	Mbps
t _{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS ⁽⁶⁹⁾	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
t _{x jitter} ⁽⁷⁰⁾	Output jitter (high-speed I/O performance pin)	—	—	—	425	—	—	425	—	—	425	ps
	Output jitter (low-speed I/O performance pin)	—	—	—	470	—	—	470	—	—	470	ps
t _{RISE}	Rise time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{FALL}	Fall time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

⁽⁶⁹⁾ TCCS specifications apply to I/O banks from the same side only.

⁽⁷⁰⁾ TX jitter is the jitter induced from core noise and I/O switching noise.



LVDS, TMDs, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications

Single Supply Devices LVDS Receiver Timing Specifications

Table 45. LVDS Receiver Timing Specifications for Intel MAX 10 Single Supply Devices

LVDS receivers are supported at all banks.

Symbol	Parameter	Mode	-C7, -I7		-A7		-C8		Unit
			Min	Max	Min	Max	Min	Max	
f _{HCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	145	5	100	5	100	MHz
		×8	5	145	5	100	5	100	MHz
		×7	5	145	5	100	5	100	MHz
		×4	5	145	5	100	5	100	MHz
		×2	5	145	5	100	5	100	MHz
		×1	5	290	5	200	5	200	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	290	100	200	100	200	Mbps
		×8	80	290	80	200	80	200	Mbps
		×7	70	290	70	200	70	200	Mbps
		×4	40	290	40	200	40	200	Mbps
		×2	20	290	20	200	20	200	Mbps
		×1	10	290	10	200	10	200	Mbps
f _{HCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	100	5	100	5	100	MHz
		×8	5	100	5	100	5	100	MHz
		×7	5	100	5	100	5	100	MHz
		×4	5	100	5	100	5	100	MHz
		×2	5	100	5	100	5	100	MHz
		×1	5	200	5	200	5	200	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	200	100	200	100	200	Mbps

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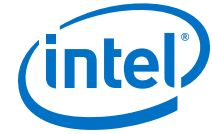


Table 54. Internal Configuration Time for Intel MAX 10 Devices (Compressed .rbf)

Compression ratio depends on design complexity. The minimum value is based on the best case (25% of original .rbf sizes) and the maximum value is based on the typical case (70% of original .rbf sizes).

Device	Internal Configuration Time (ms)			
	Unencrypted/Encrypted			
	Without Memory Initialization		With Memory Initialization	
	Min	Max	Min	Max
10M02	0.3	5.2	—	—
10M04	0.6	10.7	1.0	13.9
10M08	0.6	10.7	1.0	13.9
10M16	1.1	17.9	1.4	22.3
10M25	1.1	26.9	1.4	32.2
10M40	2.6	66.1	3.2	82.2
10M50	2.6	66.1	3.2	82.2

Internal Configuration Timing Parameter

Table 55. Internal Configuration Timing Parameter for Intel MAX 10 Devices

Symbol	Parameter	Device	Minimum	Maximum	Unit
t_{CD2UM}	CONF_DONE high to user mode	10M02, 10M04, 10M08, 10M16, 10M25	182.8	385.5	μs
		10M40, 10M50	275.3	605.7	μs

I/O Timing

The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

The Intel Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specific device and design after you complete place-and-route.

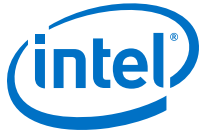


Table 56. I/O Timing for Intel MAX 10 Devices

These I/O timing parameters are for the 3.3-V LVTTTL I/O standard with the maximum drive strength and fast slew rate for 10M08DAF484 device.

Symbol	Parameter	-C7, -I7	-C8	Unit
T _{su}	Global clock setup time	-0.750	-0.808	ns
T _h	Global clock hold time	1.180	1.215	ns
T _{co}	Global clock to output delay	5.131	5.575	ns
T _{pd}	Best case pin-to-pin propagation delay through one LUT	4.907	5.467	ns

Programmable IOE Delay

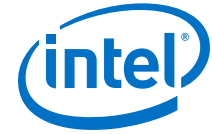
Programmable IOE Delay On Row Pins

Table 57. IOE Programmable Delay on Row Pins for Intel MAX 10 Devices

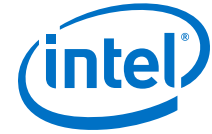
The incremental values for the settings are generally linear. For exact values of each setting, refer to the **Assignment Name** column in the latest version of the Intel Quartus Prime software.

The minimum and maximum offset timing numbers are in reference to setting '0' as available in the Intel Quartus Prime software.

Parameter	Paths Affected	Number of Settings	Minimum Offset	Maximum Offset							Unit
				Fast Corner		Slow Corner					
				−I7	−C8	−A6	−C7	−C8	−I7	−A7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	0.815	0.873	1.831	1.811	1.874	1.871	1.922	ns
Input delay from pin to input register	Pad to I/O input register	8	0	0.924	0.992	2.081	2.055	2.125	2.127	2.185	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.479	0.514	1.069	1.070	1.117	1.105	1.134	ns



Term	Definition
t _{DUTY}	HIGH-SPEED I/O Block: Duty cycle on high-speed transmitter output clock.
t _{FALL}	Signal high-to-low transition time (80–20%).
t _H	Input register hold time.
Timing Unit Interval (TUI)	HIGH-SPEED I/O block: The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t _C /w).
t _{INJITTER}	Period jitter on PLL clock input.
t _{OUTJITTER_DEDCLK}	Period jitter on dedicated clock output driven by a PLL.
t _{OUTJITTER_IO}	Period jitter on general purpose I/O driven by a PLL.
t _{pllcin}	Delay from PLL inclk pad to I/O input register.
t _{pllcout}	Delay from PLL inclk pad to I/O output register.
t _{RISE}	Signal low-to-high transition time (20–80%).
t _{SU}	Input register setup time.
V _{CM(DC)}	DC common mode input voltage.
V _{DIF(AC)}	AC differential input voltage: The minimum AC input differential voltage required for switching.
V _{DIF(DC)}	DC differential input voltage: The minimum DC input differential voltage required for switching.
V _{HYS}	Hysteresis for Schmitt trigger input.
V _{ICM}	Input common mode voltage: The common mode of the differential signal at the receiver.
V _{ID}	Input differential Voltage Swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
V _{IH}	Voltage input high: The minimum positive voltage applied to the input which is accepted by the device as a logic high.
V _{IH(AC)}	High-level AC input voltage.
V _{IH(DC)}	High-level DC input voltage.
V _{IL}	Voltage input low: The maximum positive voltage applied to the input which is accepted by the device as a logic low.
V _{IL (AC)}	Low-level AC input voltage.
V _{IL (DC)}	Low-level DC input voltage.
V _{IN}	DC input voltage.
continued...	



Date	Version	Changes
		- Added –A6 speed grade in the following tables: - Intel MAX 10 Device Grades and Speed Grades Supported - Series OCT without Calibration Specifications for Intel MAX 10 Devices - Clock Tree Specifications for Intel MAX 10 Devices - Embedded Multiplier Specifications for Intel MAX 10 Devices - Memory Block Performance Specifications for Intel MAX 10 Devices - True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices - True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices - Emulated RSDS_E_1R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices - True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices - True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices - Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices - LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices - IOE Programmable Delay on Row Pins for Intel MAX 10 Devices - IOE Programmable Delay on Column Pins for Intel MAX 10 Devices - Updated the maximum value for input clock cycle-to-cycle jitter ($t_{INJITTER_CCJ}$) with $F_{INPFD} < 100$ MHz condition from 750 ps to ± 750 ps in PLL Specifications for Intel MAX 10 Devices table. - Updated the dual supply mode performance in Embedded Multiplier Specifications for Intel MAX 10 Devices table. - Updated the dual supply mode performance in Memory Block Performance Specifications for Intel MAX 10 Devices table. - Added typical specifications in Internal Oscillator Frequencies for Intel MAX 10 Devices table. - Updated specifications in UFM Performance Specifications for Intel MAX 10 Devices table. - Updated sampling window specifications in LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices table. - Updated IOE programmable delay for row and column pins. - Changed instances of <i>Quartus II</i> to <i>Quartus Prime</i>.
June 2015	2015.06.12	- Updated the maximum values in Internal Weak Pull-Up Resistor for Intel MAX 10 Devices table. - Removed Internal Weak Pull-Up Resistor equation. - Updated the note for input resistance and input capacitance parameters in the ADC Performance Specifications table for both single supply and dual supply devices. Note: Download the SPICE models for simulation. - Added a note to AC Accuracy - THD, SNR, and SINAD parameters in the ADC Performance Specifications for Intel MAX 10 Dual Supply Devices table. Note: When using internal V_{REF}, THD = 66 dB, SNR = 58 dB and SINAD = 57.5 dB for dedicated ADC input channels. - Updated clock period jitter and cycle-to-cycle period jitter parameters in the Memory Output Clock Jitter Specifications for Intel MAX 10 Devices table.
continued...		