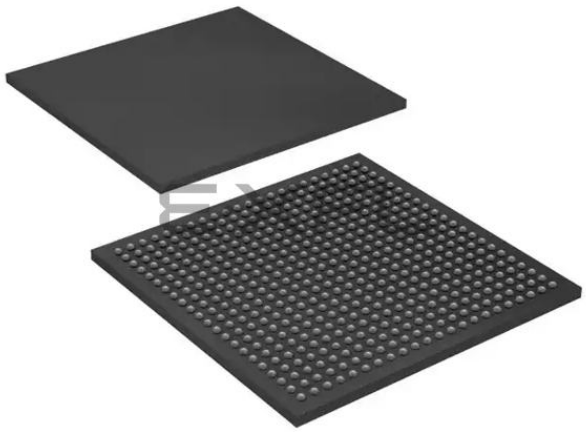

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

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Details	
Product Status	Active
Number of LABs/CLBs	3125
Number of Logic Elements/Cells	50000
Total RAM Bits	1677312
Number of I/O	360
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10m50daf484c7g

Contents

Operating Conditions

Intel MAX 10 devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Intel MAX 10 devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions for Intel MAX 10 devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Caution: Conditions outside the range listed in the absolute maximum ratings tables may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Single Supply Devices Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings for Intel MAX 10 Single Supply Devices

Symbol	Parameter	Min	Max	Unit
V_{CC_ONE}	Supply voltage for core and periphery through on-die voltage regulator	–0.5	3.9	V
V_{CCIO}	Supply voltage for input and output buffers	–0.5	3.9	V
V_{CCA}	Supply voltage for phase-locked loop (PLL) regulator and analog-to-digital converter (ADC) block (analog)	–0.5	3.9	V

Dual Supply Devices Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings for Intel MAX 10 Dual Supply Devices

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply voltage for core and periphery	–0.5	1.63	V
V_{CCIO}	Supply voltage for input and output buffers	–0.5	3.9	V
V_{CCA}	Supply voltage for PLL regulator (analog)	–0.5	3.41	V

continued...

Table 11. ADC_VREF Pin Leakage Current for Intel MAX 10 Devices

Symbol	Parameter	Condition	Min	Max	Unit
I_{adc_vref}	ADC_VREF pin leakage current	Single supply mode	—	10	µA
		Dual supply mode	—	20	µA

Bus Hold Parameters

Bus hold retains the last valid logic state after the source driving it either enters the high impedance state or is removed. Each I/O pin has an option to enable bus hold in user mode. Bus hold is always disabled in configuration mode.

Table 12. Bus Hold Parameters for Intel MAX 10 Devices

Parameter	Condition	V_{CCIO} (V)												Unit
		1.2		1.5		1.8		2.5		3.0		3.3		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold low, sustaining current	$V_{IN} > V_{IL}$ (maximum)	8	—	12	—	30	—	50	—	70	—	70	—	µA
Bus-hold high, sustaining current	$V_{IN} < V_{IH}$ (minimum)	–8	—	–12	—	–30	—	–50	—	–70	—	–70	—	µA
Bus-hold low, overdrive current	$0 V < V_{IN} < V_{CCIO}$	—	125	—	175	—	200	—	300	—	500	—	500	µA
Bus-hold high, overdrive current	$0 V < V_{IN} < V_{CCIO}$	—	–125	—	–175	—	–200	—	–300	—	–500	—	–500	µA
Bus-hold trip point	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

Table 15. OCT Variation after Calibration at Device Power-Up for Intel MAX 10 Devices

This table lists the change percentage of the OCT resistance with voltage and temperature.

Description	Nominal Voltage	dR/dT (%/°C)	dR/dV (%/mV)
OCT variation after calibration at device power-up	3.00	0.25	–0.027
	2.50	0.245	–0.04
	1.80	0.242	–0.079
	1.50	0.235	–0.125
	1.35	0.229	–0.16
	1.20	0.197	–0.208

Figure 1. Equation for OCT Resistance after Calibration at Device Power-Up

$$\Delta R_V = (V_2 - V_1) \times 1000 \times dR/dV$$

$$\Delta R_T = (T_2 - T_1) \times dR/dT$$

$$\text{For } \Delta R_X < 0; MF_X = 1/(|\Delta R_X|/100 + 1)$$

$$\text{For } \Delta R_X > 0; MF_X = \Delta R_X/100 + 1$$

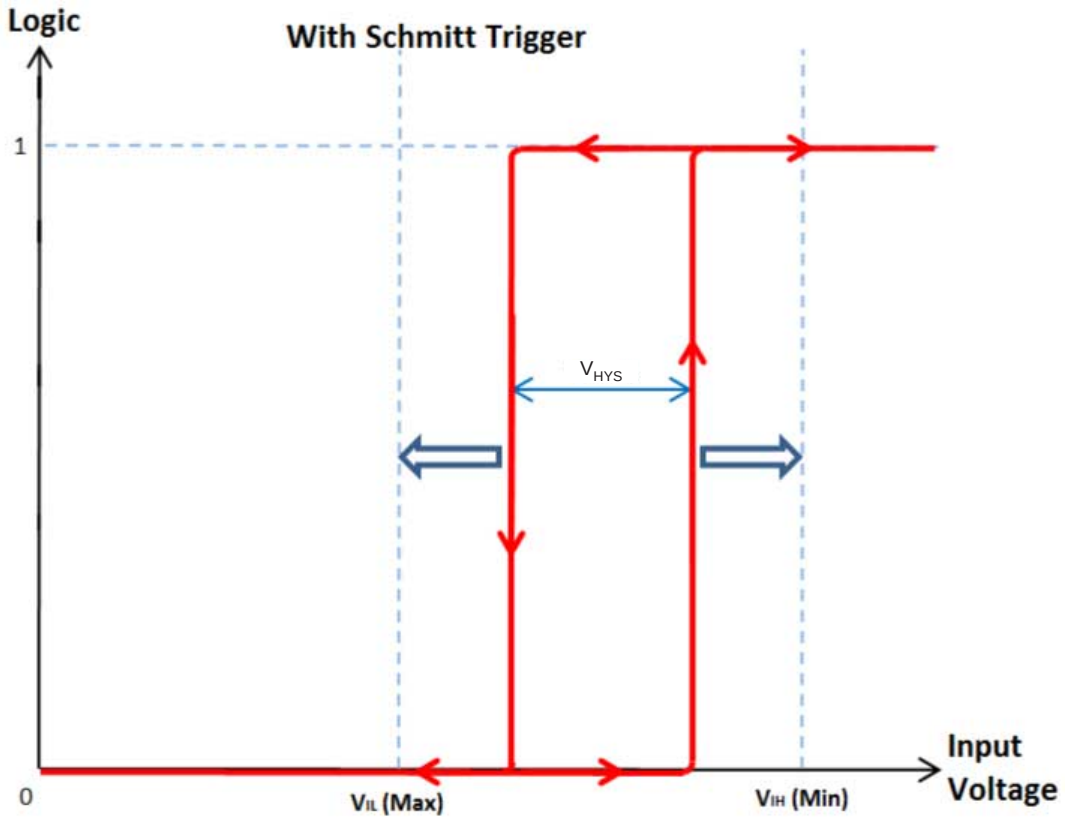
$$MF = MF_V \times MF_T$$

$$R_{final} = R_{initial} \times MF$$

The definitions for equation are as follows:

- T_1 is the initial temperature.
- T_2 is the final temperature.
- MF is multiplication factor.
- $R_{initial}$ is initial resistance.
- R_{final} is final resistance.

Figure 4. Schmitt Trigger Input Standard Voltage Diagram



I/O Standards Specifications

Tables in this section list input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Intel MAX 10 devices.

For minimum voltage values, use the minimum V_{CCIO} values. For maximum voltage values, use the maximum V_{CCIO} values.

You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{VCO} (29)	PLL internal voltage-controlled oscillator (VCO) operating range	—	600	—	1300	MHz
f_{INDUTY}	Input clock duty cycle	—	40	—	60	%
$t_{INJITTER\_CCJ}$ (30)	Input clock cycle-to-cycle jitter	F_{INPFD} ≥ 100 MHz	—	—	0.15	UI
		F_{INPFD} < 100 MHz	—	—	±750	ps
f_{OUT_EXT} (28)	PLL output frequency for external clock output	—	—	—	472.5	MHz
f_{OUT}	PLL output frequency to global clock	–6 speed grade	—	—	472.5	MHz
		–7 speed grade	—	—	450	MHz
		–8 speed grade	—	—	402.5	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output	Duty cycle set to 50%	45	50	55	%
t_{LOCK}	Time required to lock from end of device configuration	—	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically	After switchover, reconfiguring any non-post-scale counters or delays, or when `areset` is deasserted	—	—	1	ms
$t_{OUTJITTER\_PERIOD\_IO}$ (31)	Regular I/O period jitter	F_{OUT} ≥ 100 MHz	—	—	650	ps
		F_{OUT} < 100 MHz	—	—	75	mUI
$t_{OUTJITTER\_CCJ\_IO}$ (31)	Regular I/O cycle-to-cycle jitter	F_{OUT} ≥ 100 MHz	—	—	650	ps
		F_{OUT} < 100 MHz	—	—	75	mUI

continued...

(29) The VCO frequency reported by the Intel Quartus Prime software in the PLL summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

(30) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source, which is less than 200 ps.

(31) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	—	±50	ps
t_{ARESET}	Minimum pulse width on areset signal.	—	10	—	—	ns
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for PLLs	—	—	3.5 (32)	—	SCANCLK cycles
$f_{SCANCLK}$	scanclk frequency	—	—	—	100	MHz

Table 28. PLL Specifications for Intel MAX 10 Single Supply Devices

For V36 package, the PLL specification is based on single supply devices.

Symbol	Parameter	Condition	Max	Unit
$t_{OUTJITTER\_PERIOD\_DEDCLK}$ (31)	Dedicated clock output period jitter	$F_{OUT} \geq 100$ MHz	660	ps
		$F_{OUT} < 100$ MHz	66	mUI
$t_{OUTJITTER\_CCJ\_DEDCLK}$ (31)	Dedicated clock output cycle-to-cycle jitter	$F_{OUT} \geq 100$ MHz	660	ps
		$F_{OUT} < 100$ MHz	66	mUI

Table 29. PLL Specifications for Intel MAX 10 Dual Supply Devices

Symbol	Parameter	Condition	Max	Unit
$t_{OUTJITTER\_PERIOD\_DEDCLK}$ (31)	Dedicated clock output period jitter	$F_{OUT} \geq 100$ MHz	300	ps
		$F_{OUT} < 100$ MHz	30	mUI
$t_{OUTJITTER\_CCJ\_DEDCLK}$ (31)	Dedicated clock output cycle-to-cycle jitter	$F_{OUT} \geq 100$ MHz	300	ps
		$F_{OUT} < 100$ MHz	30	mUI

(32) With 100 MHz scanclk frequency.

ADC Performance Specifications

Single Supply Devices ADC Performance Specifications

Table 34. ADC Performance Specifications for Intel MAX 10 Single Supply Devices

Parameter		Symbol	Condition	Min	Typ	Max	Unit
ADC resolution		—	—	—	—	12	bits
ADC supply voltage		V_{CC_ONE}	—	2.85	3.0/3.3	3.465	V
External reference voltage		V_{REF}	—	V_{CC_ONE} – 0.5	—	V_{CC_ONE}	V
Sampling rate		F_S	Accumulative sampling rate	—	—	1	MSPS
Operating junction temperature range		T_J	—	–40	25	125	°C
Analog input voltage		V_{IN}	Prescalar disabled	0	—	V_{REF}	V
			Prescalar enabled (35)	0	—	3.6	V
Input resistance		R_{IN}	—	—	(36)	—	—
Input capacitance		C_{IN}	—	—	(36)	—	—
DC Accuracy	Offset error and drift	E_{offset}	Prescalar disabled	–0.2	—	0.2	%FS
			Prescalar enabled	–0.5	—	0.5	%FS
	Gain error and drift	E_{gain}	Prescalar disabled	–0.5	—	0.5	%FS
			Prescalar enabled	–0.75	—	0.75	%FS
	Differential non linearity	DNL	External V_{REF}, no missing code	–0.9	—	0.9	LSB
			Internal V_{REF}, no missing code	–1	—	1.7	LSB

continued...

(35) Prescalar function divides the analog input voltage by half. The analog input handles up to 3.6 V for the Intel MAX 10 single supply devices.

(36) Download the SPICE models for simulation.

Parameter		Symbol	Condition	Min	Typ	Max	Unit
	Integral non linearity	INL	—	–2	—	2	LSB
AC Accuracy	Total harmonic distortion	THD	F_{IN} = 50 kHz, F_S = 1 MHz, PLL	–65 (37)	—	—	dB
	Signal-to-noise ratio	SNR	F_{IN} = 50 kHz, F_S = 1 MHz, PLL	54 (38)	—	—	dB
	Signal-to-noise and distortion	SINAD	F_{IN} = 50 kHz, F_S = 1 MHz, PLL	53 (39)	—	—	dB
On-Chip Temperature Sensor	Temperature sampling rate	T_S	—	—	—	50	kSPS
	Absolute accuracy	—	–40 to 125°C, with 64 samples averaging (40)	—	—	±10	°C
Conversion Rate (41)	Conversion time	—	Single measurement	—	—	1	Cycle
			Continuous measurement	—	—	1	Cycle
			Temperature measurement	—	—	1	Cycle

Related Information

SPICE Models for Intel FPGAs

(37) THD with prescalar enabled is 6dB less than the specification.

(38) SNR with prescalar enabled is 6dB less than the specification.

(39) SINAD with prescalar enabled is 6dB less than the specification.

(40) For the Intel Quartus Prime software version 15.0 and later, Modular ADC Core Intel FPGA IP and Modular Dual ADC Core Intel FPGA IP cores handle the 64 samples averaging. For the Intel Quartus Prime software versions prior to 14.1, you need to implement your own averaging calculation.

(41) For more detailed description, refer to the Timing section in the *Intel MAX 10 Analog-to-Digital Converter User Guide*.

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×4	40	—	300	40	—	300	40	—	300	Mbps
		×2	20	—	300	20	—	300	20	—	300	Mbps
		×1	10	—	300	10	—	300	10	—	300	Mbps
t_{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS[53]	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
$t_{x\ Jitter}$[54]	Output jitter (high-speed I/O performance pin)	—	—	—	425	—	—	425	—	—	425	ps
	Output jitter (low-speed I/O performance pin)	—	—	—	470	—	—	470	—	—	470	ps
t_{RISE}	Rise time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	Fall time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

(53) TCCS specifications apply to I/O banks from the same side only.

(54) TX jitter is the jitter induced from core noise and I/O switching noise.

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×8	80	—	100	80	—	100	80	—	100	Mbps
		×7	70	—	100	70	—	100	70	—	100	Mbps
		×4	40	—	100	40	—	100	40	—	100	Mbps
		×2	20	—	100	20	—	100	20	—	100	Mbps
		×1	10	—	100	10	—	100	10	—	100	Mbps
t_{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS(55)	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
$t_{x\ Jitter}$(56)	Output jitter (high-speed I/O performance pin)	—	—	—	425	—	—	425	—	—	425	ps
	Output jitter (low-speed I/O performance pin)	—	—	—	470	—	—	470	—	—	470	ps
t_{RISE}	Rise time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	Fall time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

(55) TCCS specifications apply to I/O banks from the same side only.

(56) TX jitter is the jitter induced from core noise and I/O switching noise.

Symbol	Parameter	Mode	–C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{RISE}	Rise time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	Fall time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

Dual Supply Devices True LVDS Transmitter Timing Specifications

Table 42. True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

True **LVDS** transmitter is only supported at the bottom I/O banks.

Symbol	Parameter	Mode	–I6			–A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	Input clock frequency	×10	5	—	360	5	—	340	5	—	310	5	—	300	MHz
		×8	5	—	360	5	—	360	5	—	320	5	—	320	MHz
		×7	5	—	360	5	—	340	5	—	310	5	—	300	MHz
		×4	5	—	360	5	—	350	5	—	320	5	—	320	MHz
		×2	5	—	360	5	—	350	5	—	320	5	—	320	MHz
		×1	5	—	360	5	—	350	5	—	320	5	—	320	MHz
HSIODR	Data rate	×10	100	—	720	100	—	680	100	—	620	100	—	600	Mbps
		×8	80	—	720	80	—	720	80	—	640	80	—	640	Mbps
		×7	70	—	720	70	—	680	70	—	620	70	—	600	Mbps
		×4	40	—	720	40	—	700	40	—	640	40	—	640	Mbps
		×2	20	—	720	20	—	700	20	—	640	20	—	640	Mbps

continued...

Symbol	Parameter	Mode	–I6			–A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×1	10	—	360	10	—	350	10	—	320	10	—	320	Mbps
t_{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	45	—	55	%
TCCS(65)	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	—	—	300	ps
$t_{x\ Jitter}$(66)	Output jitter	—	—	—	380	—	—	380	—	—	380	—	—	380	ps
t_{RISE}	Rise time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	Fall time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	—	—	1	ms

(65) TCCS specifications apply to I/O banks from the same side only.

(66) TX jitter is the jitter induced from core noise and I/O switching noise.

Symbol	Parameter	Mode	–C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×8	80	—	200	80	—	200	80	—	200	Mbps
		×7	70	—	200	70	—	200	70	—	200	Mbps
		×4	40	—	200	40	—	200	40	—	200	Mbps
		×2	20	—	200	20	—	200	20	—	200	Mbps
		×1	10	—	200	10	—	200	10	—	200	Mbps
t_{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS[67]	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
$t_{x\ Jitter}$[68]	Output jitter	—	—	—	1,000	—	—	1,000	—	—	1,000	ps
t_{RISE}	Rise time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	Fall time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

(67) TCCS specifications apply to I/O banks from the same side only.

(68) TX jitter is the jitter induced from core noise and I/O switching noise.

Dual Supply Devices Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications

Table 44. Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

Emulated **LVDS_E_3R**, **SLVS**, and **Sub-LVDS** transmitters are supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	—	300	5	—	275	5	—	275	MHz
		×8	5	—	300	5	—	275	5	—	275	MHz
		×7	5	—	300	5	—	275	5	—	275	MHz
		×4	5	—	300	5	—	275	5	—	275	MHz
		×2	5	—	300	5	—	275	5	—	275	MHz
		×1	5	—	300	5	—	275	5	—	275	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	—	600	100	—	550	100	—	550	Mbps
		×8	80	—	600	80	—	550	80	—	550	Mbps
		×7	70	—	600	70	—	550	70	—	550	Mbps
		×4	40	—	600	40	—	550	40	—	550	Mbps
		×2	20	—	600	20	—	550	20	—	550	Mbps
		×1	10	—	300	10	—	275	10	—	275	Mbps
f_{HSCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	—	150	5	—	150	5	—	150	MHz
		×8	5	—	150	5	—	150	5	—	150	MHz
		×7	5	—	150	5	—	150	5	—	150	MHz
		×4	5	—	150	5	—	150	5	—	150	MHz
		×2	5	—	150	5	—	150	5	—	150	MHz
		×1	5	—	300	5	—	300	5	—	300	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	—	300	100	—	300	100	—	300	Mbps
		×8	80	—	300	80	—	300	80	—	300	Mbps

continued...

Device	CFM Data Size (bits)	
	Without Memory Initialization	With Memory Initialization
10M25	4,140,000	4,780,000
10M40	7,840,000	9,670,000
10M50	7,840,000	9,670,000

Internal Configuration Time

The internal configuration time measurement is from the rising edge of nSTATUS signal to the rising edge of CONF_DONE signal.

Table 53. Internal Configuration Time for Intel MAX 10 Devices (Uncompressed .rbf)

Device	Internal Configuration Time (ms)							
	Unencrypted				Encrypted			
	Without Memory Initialization		With Memory Initialization		Without Memory Initialization		With Memory Initialization	
	Min	Max	Min	Max	Min	Max	Min	Max
10M02	0.3	1.7	—	—	1.7	5.4	—	—
10M04	0.6	2.7	1.0	3.4	5.0	15.0	6.8	19.6
10M08	0.6	2.7	1.0	3.4	5.0	15.0	6.8	19.6
10M16	1.1	3.7	1.4	4.5	9.3	25.3	11.7	31.5
10M25	1.0	3.7	1.3	4.4	14.0	38.1	16.9	45.7
10M40	2.6	6.9	3.2	9.8	41.5	112.1	51.7	139.6
10M50	2.6	6.9	3.2	9.8	41.5	112.1	51.7	139.6

Table 54. Internal Configuration Time for Intel MAX 10 Devices (Compressed .rbf)

Compression ratio depends on design complexity. The minimum value is based on the best case (25% of original `.rbf` sizes) and the maximum value is based on the typical case (70% of original `.rbf` sizes).

Device	Internal Configuration Time (ms)			
	Unencrypted/Encrypted			
	Without Memory Initialization		With Memory Initialization	
	Min	Max	Min	Max
10M02	0.3	5.2	—	—
10M04	0.6	10.7	1.0	13.9
10M08	0.6	10.7	1.0	13.9
10M16	1.1	17.9	1.4	22.3
10M25	1.1	26.9	1.4	32.2
10M40	2.6	66.1	3.2	82.2
10M50	2.6	66.1	3.2	82.2

Internal Configuration Timing Parameter

Table 55. Internal Configuration Timing Parameter for Intel MAX 10 Devices

Symbol	Parameter	Device	Minimum	Maximum	Unit
t_{CD2UM}	`CONF_DONE` high to user mode	10M02, 10M04, 10M08, 10M16, 10M25	182.8	385.5	µs
		10M40, 10M50	275.3	605.7	µs

I/O Timing

The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

The Intel Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specific device and design after you complete place-and-route.

Table 56. I/O Timing for Intel MAX 10 Devices

These I/O timing parameters are for the 3.3-V LVTTL I/O standard with the maximum drive strength and fast slew rate for 10M08DAF484 device.

Symbol	Parameter	–C7, –I7	–C8	Unit
T_{su}	Global clock setup time	–0.750	–0.808	ns
T_h	Global clock hold time	1.180	1.215	ns
T_{co}	Global clock to output delay	5.131	5.575	ns
T_{pd}	Best case pin-to-pin propagation delay through one LUT	4.907	5.467	ns

Programmable IOE Delay

Programmable IOE Delay On Row Pins

Table 57. IOE Programmable Delay on Row Pins for Intel MAX 10 Devices

The incremental values for the settings are generally linear. For exact values of each setting, refer to the **Assignment Name** column in the latest version of the Intel Quartus Prime software.

The minimum and maximum offset timing numbers are in reference to setting '0' as available in the Intel Quartus Prime software.

Parameter	Paths Affected	Number of Settings	Minimum Offset	Maximum Offset							Unit
				Fast Corner		Slow Corner					
				–I7	–C8	–A6	–C7	–C8	–I7	–A7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	0.815	0.873	1.831	1.811	1.874	1.871	1.922	ns
Input delay from pin to input register	Pad to I/O input register	8	0	0.924	0.992	2.081	2.055	2.125	2.127	2.185	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.479	0.514	1.069	1.070	1.117	1.105	1.134	ns

Term	Definition
t_{DUTY}	HIGH-SPEED I/O Block: Duty cycle on high-speed transmitter output clock.
t_{FALL}	Signal high-to-low transition time (80–20%).
t_H	Input register hold time.
Timing Unit Interval (TUI)	HIGH-SPEED I/O block: The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w).
$t_{INJITTER}$	Period jitter on PLL clock input.
$t_{OUTJITTER\_DEDCLK}$	Period jitter on dedicated clock output driven by a PLL.
$t_{OUTJITTER\_IO}$	Period jitter on general purpose I/O driven by a PLL.
t_{plicin}	Delay from PLL inclk pad to I/O input register.
$t_{plicout}$	Delay from PLL inclk pad to I/O output register.
t_{RISE}	Signal low-to-high transition time (20–80%).
t_{SU}	Input register setup time.
$V_{CM(DC)}$	DC common mode input voltage.
$V_{DIF(AC)}$	AC differential input voltage: The minimum AC input differential voltage required for switching.
$V_{DIF(DC)}$	DC differential input voltage: The minimum DC input differential voltage required for switching.
V_{HYS}	Hysteresis for Schmitt trigger input.
V_{ICM}	Input common mode voltage: The common mode of the differential signal at the receiver.
V_{ID}	Input differential Voltage Swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
V_{IH}	Voltage input high: The minimum positive voltage applied to the input which is accepted by the device as a logic high.
$V_{IH(AC)}$	High-level AC input voltage.
$V_{IH(DC)}$	High-level DC input voltage.
V_{IL}	Voltage input low: The maximum positive voltage applied to the input which is accepted by the device as a logic low.
$V_{IL\ (AC)}$	Low-level AC input voltage.
$V_{IL\ (DC)}$	Low-level DC input voltage.
V_{IN}	DC input voltage.

continued...

Term	Definition
V_{OCM}	Output common mode voltage: The common mode of the differential signal at the transmitter.
V_{OD}	Output differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission line at the transmitter. $V_{OD} = V_{OH} – V_{OL}$.
V_{OH}	Voltage output high: The maximum positive voltage from an output which the device considers is accepted as the minimum positive high level.
V_{OL}	Voltage output low: The maximum positive voltage from an output which the device considers is accepted as the maximum positive low level.
V_{OS}	Output offset voltage: $V_{OS} = (V_{OH} + V_{OL}) / 2$.
$V_{OX\ (AC)}$	AC differential Output cross point voltage: The voltage at which the differential output signals must cross.
V_{REF}	Reference voltage for SSTL, HSTL, and HSUL I/O Standards.
$V_{REF(AC)}$	AC input reference voltage for SSTL, HSTL, and HSUL I/O Standards. $V_{REF(AC)} = V_{REF(DC)}$ + noise. The peak-to-peak AC noise on V_{REF} should not exceed 2% of $V_{REF(DC)}$.
$V_{REF(DC)}$	DC input reference voltage for SSTL, HSTL, and HSUL I/O Standards.
$V_{SWING\ (AC)}$	AC differential input voltage: AC Input differential voltage required for switching.
$V_{SWING\ (DC)}$	DC differential input voltage: DC Input differential voltage required for switching.
V_{TT}	Termination voltage for SSTL, HSTL, and HSUL I/O Standards.
$V_{X\ (AC)}$	AC differential Input cross point voltage: The voltage at which the differential input signals must cross.

Document Revision History for the Intel MAX 10 FPGA Device Datasheet

Document Version	Changes
2018.06.29	• Removed links on instant-on feature. • Added JTAG timing specifications term in *Glossary*. • Renamed the following IP cores as per Intel rebranding: — Renamed Altera Modular ADC IP core to Modular ADC core Intel FPGA IP core. — Renamed Altera Modular Dual ADC IP core to Modular Dual ADC core Intel FPGA IP core.