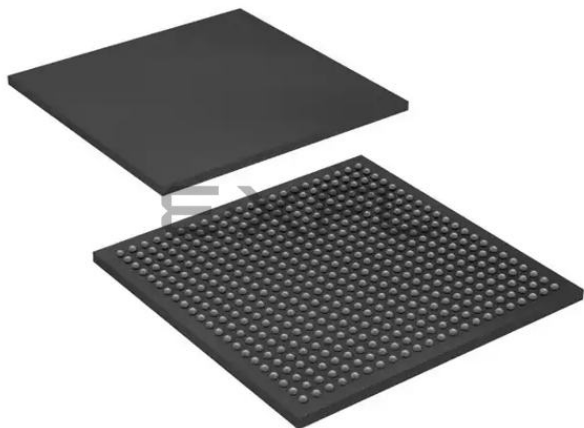




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

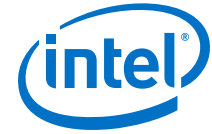
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	3125
Number of Logic Elements/Cells	50000
Total RAM Bits	1677312
Number of I/O	360
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10m50daf484i7g

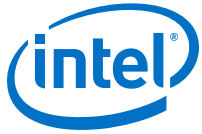


Single-Ended I/O Standards Specifications

Table 20. Single-Ended I/O Standards Specifications for Intel MAX 10 Devices

To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the 3.3-V LVTTTL specification (4 mA), you should set the current strength settings to 4 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3 V LVTTTL	3.135	3.3	3.465	-0.3	0.8	1.7	3.6	0.45	2.4	4	-4
3.3 V LVCMOS	3.135	3.3	3.465	-0.3	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	2	-2
3.0 V LVTTTL	2.85	3	3.15	-0.3	0.8	1.7	$V_{CCIO} + 0.3$	0.45	2.4	4	-4
3.0 V LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	$V_{CCIO} + 0.3$	0.2	$V_{CCIO} - 0.2$	0.1	-0.1
2.5 V LVTTTL and LVCMOS	2.375	2.5	2.625	-0.3	0.7	1.7	$V_{CCIO} + 0.3$	0.4	2	1	-1
1.8 V LVTTTL and LVCMOS	1.71	1.8	1.89	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	2.25	0.45	$V_{CCIO} - 0.45$	2	-2
1.5 V LVCMOS	1.425	1.5	1.575	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2
1.2 V LVCMOS	1.14	1.2	1.26	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2
3.3 V Schmitt Trigger	3.135	3.3	3.465	-0.3	0.8	1.7	$V_{CCIO} + 0.3$	—	—	—	—
2.5 V Schmitt Trigger	2.375	2.5	2.625	-0.3	0.7	1.7	$V_{CCIO} + 0.3$	—	—	—	—
1.8 V Schmitt Trigger	1.71	1.8	1.89	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	—	—	—	—
1.5 V Schmitt Trigger	1.425	1.5	1.575	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	—	—	—	—
3.0 V PCI	2.85	3	3.15	—	$0.3 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	1.5	-0.5



Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

Table 21. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Intel MAX 10 Devices

I/O Standard	V _{CCIO} (V)			V _{REF} (V)			V _{TT} (V) ⁽¹⁴⁾		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	1.19	1.25	1.31	V _{REF} - 0.04	V _{REF}	V _{REF} + 0.04
SSTL-18 Class I, II	1.7	1.8	1.9	0.833	0.9	0.969	V _{REF} - 0.04	V _{REF}	V _{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 × V _{CCIO}	0.5 × V _{CCIO}	0.51 × V _{CCIO}	0.49 × V _{CCIO}	0.5 × V _{CCIO}	0.51 × V _{CCIO}
SSTL-135 Class I, II	1.283	1.35	1.45	0.49 × V _{CCIO}	0.5 × V _{CCIO}	0.51 × V _{CCIO}	0.49 × V _{CCIO}	0.5 × V _{CCIO}	0.51 × V _{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	0.85	0.9	0.95
HSTL-15 Class I, II	1.425	1.5	1.575	0.71	0.75	0.79	0.71	0.75	0.79
HSTL-12 Class I, II	1.14	1.2	1.26	0.48 × V _{CCIO} ⁽¹⁵⁾	0.5 × V _{CCIO} ⁽¹⁵⁾	0.52 × V _{CCIO} ⁽¹⁵⁾	—	0.5 × V _{CCIO}	—
				0.47 × V _{CCIO} ⁽¹⁶⁾	0.5 × V _{CCIO} ⁽¹⁶⁾	0.53 × V _{CCIO} ⁽¹⁶⁾			
HSUL-12	1.14	1.2	1.3	0.49 × V _{CCIO}	0.5 × V _{CCIO}	0.51 × V _{CCIO}	—	—	—

⁽¹⁴⁾ V_{TT} of transmitting device must track V_{REF} of the receiving device.

⁽¹⁵⁾ Value shown refers to DC input reference voltage, V_{REF(DC)}.

⁽¹⁶⁾ Value shown refers to AC input reference voltage, V_{REF(AC)}.



I/O Standard	V _{IL(DC)} (V)		V _{IH(DC)} (V)		V _{IL(AC)} (V)		V _{IH(AC)} (V)		V _{OL} (V)	V _{OH} (V)	I _{OL} (mA)	I _{OH} (mA)
	Min	Max	Min	Max	Min	Max	Min	Max	Max	Min		
HSTL-12 Class I	-0.15	V _{REF} - 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	-0.24	V _{REF} - 0.15	V _{REF} + 0.15	V _{CCIO} + 0.24	0.25 × V _{CCIO}	0.75 × V _{CCIO}	8	-8
HSTL-12 Class II	-0.15	V _{REF} - 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	-0.24	V _{REF} - 0.15	V _{REF} + 0.15	V _{CCIO} + 0.24	0.25 × V _{CCIO}	0.75 × V _{CCIO}	14	-14
HSUL-12	—	V _{REF} - 0.13	V _{REF} + 0.13	—	—	V _{REF} - 0.22	V _{REF} + 0.22	—	0.1 × V _{CCIO}	0.9 × V _{CCIO}	—	—

Differential SSTL I/O Standards Specifications

Differential SSTL requires a V_{REF} input.

Table 23. Differential SSTL I/O Standards Specifications for Intel MAX 10 Devices

I/O Standard	V _{CCIO} (V)			V _{Swing(DC)} (V)		V _{X(AC)} (V)			V _{Swing(AC)} (V)	
	Min	Typ	Max	Min	Max ⁽¹⁷⁾	Min	Typ	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.36	V _{CCIO}	V _{CCIO} /2 - 0.2	—	V _{CCIO} /2 + 0.2	0.7	V _{CCIO}
SSTL-18 Class I, II	1.7	1.8	1.9	0.25	V _{CCIO}	V _{CCIO} /2 - 0.175	—	V _{CCIO} /2 + 0.175	0.5	V _{CCIO}
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	V _{CCIO} /2 - 0.15	—	V _{CCIO} /2 + 0.15	2(V _{IH(AC)} - V _{REF})	2(V _{IL(AC)} - V _{REF})
SSTL-135	1.283	1.35	1.45	0.18	—	V _{REF} - 0.135	0.5 × V _{CCIO}	V _{REF} + 0.135	2(V _{IH(AC)} - V _{REF})	2(V _{IL(AC)} - V _{REF})

Differential HSTL and HSUL I/O Standards Specifications

Differential HSTL requires a V_{REF} input.

⁽¹⁷⁾ The maximum value for V_{SWING(DC)} is not defined. However, each single-ended signal needs to be within the respective single-ended limits (V_{IH(DC)} and V_{IL(DC)}).

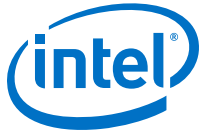


I/O Standard	V _{CCIO} (V)			V _{ID} (mV)		V _{ICM} (V) ⁽¹⁸⁾			V _{OD} (mV) ⁽¹⁹⁾⁽²⁰⁾			V _{OS} (V) ⁽¹⁹⁾		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
						1.05	D _{MAX} > 700 Mbps	1.55						
BLVDS ⁽²²⁾	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—
mini-LVDS ⁽²³⁾	2.375	2.5	2.625	—	—	—	—	—	300	—	600	1	1.2	1.4
RSDS ⁽²³⁾	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.5
PPDS (Row I/Os) ⁽²³⁾	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.4
TMDS ⁽²⁴⁾	2.375	2.5	2.625	100	—	0.05	D _{MAX} ≤ 500 Mbps	1.8	—	—	—	—	—	—
						0.55	500 Mbps ≤ D _{MAX} ≤ 700 Mbps	1.8						
						1.05	D _{MAX} > 700 Mbps	1.55						
Sub-LVDS ⁽²⁵⁾	1.71	1.8	1.89	100	—	0.55	—	1.25	⁽²⁶⁾			0.8	0.9	1
SLVS	2.375	2.5	2.625	100	—	0.05	—	1.1	⁽²⁶⁾			⁽²⁷⁾		
continued..														

⁽¹⁸⁾ V_{IN} range: 0 V ≤ V_{IN} ≤ 1.85 V.

⁽¹⁹⁾ R_L range: 90 ≤ R_L ≤ 110 Ω.

⁽²⁰⁾ Low V_{OD} setting is only supported for RSBS standard.



Internal Oscillator Specifications

Table 32. Internal Oscillator Frequencies for Intel MAX 10 Devices

You can access to the internal oscillator frequencies in this table. The duty cycle of internal oscillator is approximately 45%–55%.

Device	Frequency			Unit
	Minimum	Typical	Maximum	
10M02	55	82	116	MHz
10M04				
10M08				
10M16				
10M25				
10M40	35	52	77	MHz
10M50				

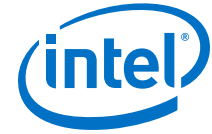
UFM Performance Specifications

Table 33. UFM Performance Specifications for Intel MAX 10 Devices

Block	Mode	Interface	Device	Frequency		Unit
				Minimum	Maximum	
UFM	Avalon®-MM slave	Parallel ⁽³³⁾	10M02 ⁽³⁴⁾	3.43	7.25	MHz
			10M04, 10M08, 10M16, 10M25, 10M40, 10M50	5	116	MHz
		Serial ⁽³⁴⁾	10M02, 10M04, 10M08, 10M16, 10M25	3.43	7.25	MHz
			10M40, 10M50	2.18	4.81	MHz

⁽³³⁾ Clock source is derived from user, except for 10M02 device.

⁽³⁴⁾ Clock source is derived from 1/16 of the frequency of the internal oscillator.



ADC Performance Specifications

Single Supply Devices ADC Performance Specifications

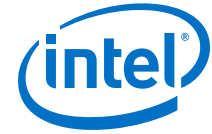
Table 34. ADC Performance Specifications for Intel MAX 10 Single Supply Devices

Parameter		Symbol	Condition	Min	Typ	Max	Unit
ADC resolution		—	—	—	—	12	bits
ADC supply voltage		V_{CC_ONE}	—	2.85	3.0/3.3	3.465	V
External reference voltage		V_{REF}	—	$V_{CC_ONE} - 0.5$	—	V_{CC_ONE}	V
Sampling rate		F_S	Accumulative sampling rate	—	—	1	MSPS
Operating junction temperature range		T_J	—	−40	25	125	°C
Analog input voltage		V_{IN}	Prescaler disabled	0	—	V_{REF}	V
			Prescaler enabled ⁽³⁵⁾	0	—	3.6	V
Input resistance		R_{IN}	—	—	⁽³⁶⁾	—	—
Input capacitance		C_{IN}	—	—	⁽³⁶⁾	—	—
DC Accuracy	Offset error and drift	E_{offset}	Prescaler disabled	−0.2	—	0.2	%FS
			Prescaler enabled	−0.5	—	0.5	%FS
	Gain error and drift	E_{gain}	Prescaler disabled	−0.5	—	0.5	%FS
			Prescaler enabled	−0.75	—	0.75	%FS
	Differential non linearity	DNL	External V_{REF} , no missing code	−0.9	—	0.9	LSB
			Internal V_{REF} , no missing code	−1	—	1.7	LSB

continued...

⁽³⁵⁾ Prescaler function divides the analog input voltage by half. The analog input handles up to 3.6 V for the Intel MAX 10 single supply devices.

⁽³⁶⁾ Download the SPICE models for simulation.



Parameter		Symbol	Condition	Min	Typ	Max	Unit
Conversion Rate ⁽⁵²⁾	Conversion time	—	Single measurement	—	—	1	Cycle
			Continuous measurement	—	—	1	Cycle
			Temperature measurement	—	—	1	Cycle

Related Information

[SPICE Models for Intel FPGAs](#)

Periphery Performance Specifications

This section describes the periphery performance, high-speed I/O, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

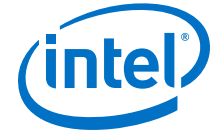
High-Speed I/O Specifications

For more information about the high-speed and low-speed I/O performance pins, refer to the respective device pin-out files.

Related Information

[Documentation: Pin-Out Files for Intel FPGAs](#)

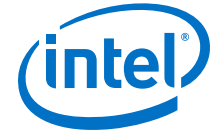
⁽⁵²⁾ For more detailed description, refer to the Timing section in the *Intel MAX 10 Analog-to-Digital Converter User Guide*.



Symbol	Parameter	Mode	-I6, -A6, -C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×4	40	—	300	40	—	300	40	—	300	Mbps
		×2	20	—	300	20	—	300	20	—	300	Mbps
		×1	10	—	300	10	—	300	10	—	300	Mbps
t _{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS ⁽⁵³⁾	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
t _{x jitter} ⁽⁵⁴⁾	Output jitter (high-speed I/O performance pin)	—	—	—	425	—	—	425	—	—	425	ps
	Output jitter (low-speed I/O performance pin)	—	—	—	470	—	—	470	—	—	470	ps
t _{RISE}	Rise time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{FALL}	Fall time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

⁽⁵³⁾ TCCS specifications apply to I/O banks from the same side only.

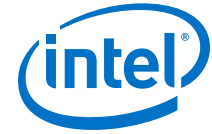
⁽⁵⁴⁾ TX jitter is the jitter induced from core noise and I/O switching noise.



Symbol	Parameter	Mode	-I6, -A6, -C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×8	80	—	100	80	—	100	80	—	100	Mbps
		×7	70	—	100	70	—	100	70	—	100	Mbps
		×4	40	—	100	40	—	100	40	—	100	Mbps
		×2	20	—	100	20	—	100	20	—	100	Mbps
		×1	10	—	100	10	—	100	10	—	100	Mbps
t _{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS ⁽⁵⁵⁾	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
t _x Jitter ⁽⁵⁶⁾	Output jitter (high-speed I/O performance pin)	—	—	—	425	—	—	425	—	—	425	ps
	Output jitter (low-speed I/O performance pin)	—	—	—	470	—	—	470	—	—	470	ps
t _{RISE}	Rise time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{FALL}	Fall time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

⁽⁵⁵⁾ TCCS specifications apply to I/O banks from the same side only.

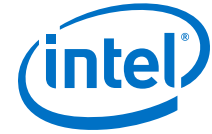
⁽⁵⁶⁾ TX jitter is the jitter induced from core noise and I/O switching noise.



Symbol	Parameter	Mode	-I6, -A6, -C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×4	40	—	300	40	—	300	40	—	300	Mbps
		×2	20	—	300	20	—	300	20	—	300	Mbps
		×1	10	—	300	10	—	300	10	—	300	Mbps
t _{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS ⁽⁵⁷⁾	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
t _{x jitter} ⁽⁵⁸⁾	Output jitter (high-speed I/O performance pin)	—	—	—	425	—	—	425	—	—	425	ps
	Output jitter (low-speed I/O performance pin)	—	—	—	470	—	—	470	—	—	470	ps
t _{RISE}	Rise time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{FALL}	Fall time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

⁽⁵⁷⁾ TCCS specifications apply to I/O banks from the same side only.

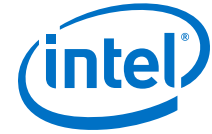
⁽⁵⁸⁾ TX jitter is the jitter induced from core noise and I/O switching noise.



Symbol	Parameter	Mode	-I6, -A6, -C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×4	40	—	170	40	—	170	40	—	170	Mbps
		×2	20	—	170	20	—	170	20	—	170	Mbps
		×1	10	—	170	10	—	170	10	—	170	Mbps
t _{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS ⁽⁵⁹⁾	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
t _{x jitter} ⁽⁶⁰⁾	Output jitter (high-speed I/O performance pin)	—	—	—	425	—	—	425	—	—	425	ps
	Output jitter (low-speed I/O performance pin)	—	—	—	470	—	—	470	—	—	470	ps
t _{RISE}	Rise time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{FALL}	Fall time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

⁽⁵⁹⁾ TCCS specifications apply to I/O banks from the same side only.

⁽⁶⁰⁾ TX jitter is the jitter induced from core noise and I/O switching noise.



Symbol	Parameter	Mode	-C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t _{RISE}	Rise time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{FALL}	Fall time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

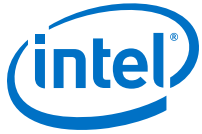
Dual Supply Devices True LVDS Transmitter Timing Specifications

Table 42. True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

True LVDS transmitter is only supported at the bottom I/O banks.

Symbol	Parameter	Mode	-I6			-A6, -C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{HSCLK}	Input clock frequency	×10	5	—	360	5	—	340	5	—	310	5	—	300	MHz
		×8	5	—	360	5	—	360	5	—	320	5	—	320	MHz
		×7	5	—	360	5	—	340	5	—	310	5	—	300	MHz
		×4	5	—	360	5	—	350	5	—	320	5	—	320	MHz
		×2	5	—	360	5	—	350	5	—	320	5	—	320	MHz
		×1	5	—	360	5	—	350	5	—	320	5	—	320	MHz
HSIODR	Data rate	×10	100	—	720	100	—	680	100	—	620	100	—	600	Mbps
		×8	80	—	720	80	—	720	80	—	640	80	—	640	Mbps
		×7	70	—	720	70	—	680	70	—	620	70	—	600	Mbps
		×4	40	—	720	40	—	700	40	—	640	40	—	640	Mbps
		×2	20	—	720	20	—	700	20	—	640	20	—	640	Mbps

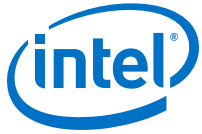
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Symbol	Parameter	Mode	-I6			-A6, -C7, -I7			-A7			-C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×1	10	—	360	10	—	350	10	—	320	10	—	320	Mbps
t _{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	45	—	55	%
TCCS ⁽⁶⁵⁾	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	—	—	300	ps
t _x Jitter ⁽⁶⁶⁾	Output jitter	—	—	—	380	—	—	380	—	—	380	—	—	380	ps
t _{RISE}	Rise time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	ps
t _{FALL}	Fall time	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	ps
t _{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	—	—	1	ms

⁽⁶⁵⁾ TCCS specifications apply to I/O banks from the same side only.

⁽⁶⁶⁾ TX jitter is the jitter induced from core noise and I/O switching noise.



Symbol	Parameter	Mode	-I6, -A6, -C7, -I7		-A7		-C8		Unit
			Min	Max	Min	Max	Min	Max	
	Sampling window (low-speed I/O performance pin)	—	—	910	—	910	—	910	ps
$t_{x \text{ Jitter}}^{(72)}$	Input jitter	—	—	500	—	500	—	500	ps
t_{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	1	—	1	—	1	ms

Memory Standards Supported by the Soft Memory Controller

Table 47. Memory Standards Supported by the Soft Memory Controller for Intel MAX 10 Devices

Contact your local sales representatives for access to the -I6 or -A6 speed grade devices in the Intel Quartus Prime software.

External Memory Interface Standard	Rate Support	Speed Grade	Voltage (V)	Max Frequency (MHz)
DDR3 SDRAM	Half	-I6	1.5	303
DDR3L SDRAM	Half	-I6	1.35	303
DDR2 SDRAM	Half	-I6	1.8	200
		-I7 and -C7		167
LPDDR2 ⁽⁷³⁾	Half	-I6	1.2	200 ⁽⁷⁴⁾

Related Information

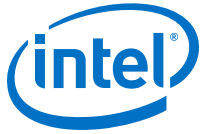
[External Memory Interface Spec Estimator](#)

Provides the specific details of the memory standards supported.

⁽⁷²⁾ TX jitter is the jitter induced from core noise and I/O switching noise.

⁽⁷³⁾ Intel MAX 10 devices support only single-die LPDDR2.

⁽⁷⁴⁾ To achieve the specified performance, constrain the memory device I/O and core power supply variation to within $\pm 3\%$. By default, the frequency is 167 MHz.



Device	CFM Data Size (bits)	
	Without Memory Initialization	With Memory Initialization
10M25	4,140,000	4,780,000
10M40	7,840,000	9,670,000
10M50	7,840,000	9,670,000

Internal Configuration Time

The internal configuration time measurement is from the rising edge of nSTATUS signal to the rising edge of CONF_DONE signal.

Table 53. Internal Configuration Time for Intel MAX 10 Devices (Uncompressed .rbf)

Device	Internal Configuration Time (ms)							
	Unencrypted				Encrypted			
	Without Memory Initialization		With Memory Initialization		Without Memory Initialization		With Memory Initialization	
	Min	Max	Min	Max	Min	Max	Min	Max
10M02	0.3	1.7	—	—	1.7	5.4	—	—
10M04	0.6	2.7	1.0	3.4	5.0	15.0	6.8	19.6
10M08	0.6	2.7	1.0	3.4	5.0	15.0	6.8	19.6
10M16	1.1	3.7	1.4	4.5	9.3	25.3	11.7	31.5
10M25	1.0	3.7	1.3	4.4	14.0	38.1	16.9	45.7
10M40	2.6	6.9	3.2	9.8	41.5	112.1	51.7	139.6
10M50	2.6	6.9	3.2	9.8	41.5	112.1	51.7	139.6

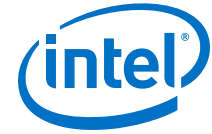


Table 54. Internal Configuration Time for Intel MAX 10 Devices (Compressed .rbf)

Compression ratio depends on design complexity. The minimum value is based on the best case (25% of original .rbf sizes) and the maximum value is based on the typical case (70% of original .rbf sizes).

Device	Internal Configuration Time (ms)			
	Unencrypted/Encrypted			
	Without Memory Initialization		With Memory Initialization	
	Min	Max	Min	Max
10M02	0.3	5.2	—	—
10M04	0.6	10.7	1.0	13.9
10M08	0.6	10.7	1.0	13.9
10M16	1.1	17.9	1.4	22.3
10M25	1.1	26.9	1.4	32.2
10M40	2.6	66.1	3.2	82.2
10M50	2.6	66.1	3.2	82.2

Internal Configuration Timing Parameter

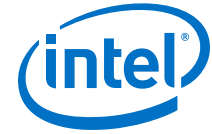
Table 55. Internal Configuration Timing Parameter for Intel MAX 10 Devices

Symbol	Parameter	Device	Minimum	Maximum	Unit
t _{CD2UM}	CONF_DONE high to user mode	10M02, 10M04, 10M08, 10M16, 10M25	182.8	385.5	μs
		10M40, 10M50	275.3	605.7	μs

I/O Timing

The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

The Intel Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specific device and design after you complete place-and-route.



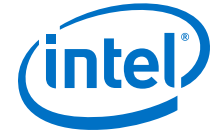
Programmable IOE Delay for Column Pins

Table 58. IOE Programmable Delay on Column Pins for Intel MAX 10 Devices

The incremental values for the settings are generally linear. For exact values of each setting, refer to the **Assignment Name** column in the latest version of the Intel Quartus Prime software.

The minimum and maximum offset timing numbers are in reference to setting '0' as available in the Intel Quartus Prime software.

Parameter	Paths Affected	Number of Settings	Minimum Offset	Maximum Offset							Unit
				Fast Corner		Slow Corner					
				−I7	−C8	−A6	−C7	−C8	−I7	−A7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	0.81	0.868	1.823	1.802	1.864	1.862	1.912	ns
Input delay from pin to input register	Pad to I/O input register	8	0	0.914	0.981	2.06	2.032	2.101	2.102	2.161	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.435	0.466	0.971	0.97	1.013	1.001	1.028	ns



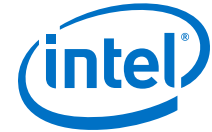
Term	Definition
t _{DUTY}	HIGH-SPEED I/O Block: Duty cycle on high-speed transmitter output clock.
t _{FALL}	Signal high-to-low transition time (80–20%).
t _H	Input register hold time.
Timing Unit Interval (TUI)	HIGH-SPEED I/O block: The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t _C /w).
t _{INJITTER}	Period jitter on PLL clock input.
t _{OUTJITTER_DEDCLK}	Period jitter on dedicated clock output driven by a PLL.
t _{OUTJITTER_IO}	Period jitter on general purpose I/O driven by a PLL.
t _{pllcin}	Delay from PLL inclk pad to I/O input register.
t _{pllcout}	Delay from PLL inclk pad to I/O output register.
t _{RISE}	Signal low-to-high transition time (20–80%).
t _{SU}	Input register setup time.
V _{CM(DC)}	DC common mode input voltage.
V _{DIF(AC)}	AC differential input voltage: The minimum AC input differential voltage required for switching.
V _{DIF(DC)}	DC differential input voltage: The minimum DC input differential voltage required for switching.
V _{HYS}	Hysteresis for Schmitt trigger input.
V _{ICM}	Input common mode voltage: The common mode of the differential signal at the receiver.
V _{ID}	Input differential Voltage Swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
V _{IH}	Voltage input high: The minimum positive voltage applied to the input which is accepted by the device as a logic high.
V _{IH(AC)}	High-level AC input voltage.
V _{IH(DC)}	High-level DC input voltage.
V _{IL}	Voltage input low: The maximum positive voltage applied to the input which is accepted by the device as a logic low.
V _{IL (AC)}	Low-level AC input voltage.
V _{IL (DC)}	Low-level DC input voltage.
V _{IN}	DC input voltage.
continued...	



Term	Definition
V _{OCM}	Output common mode voltage: The common mode of the differential signal at the transmitter.
V _{OD}	Output differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission line at the transmitter. $V_{OD} = V_{OH} - V_{OL}$.
V _{OH}	Voltage output high: The maximum positive voltage from an output which the device considers is accepted as the minimum positive high level.
V _{OL}	Voltage output low: The maximum positive voltage from an output which the device considers is accepted as the maximum positive low level.
V _{OS}	Output offset voltage: $V_{OS} = (V_{OH} + V_{OL}) / 2$.
V _{OX (AC)}	AC differential Output cross point voltage: The voltage at which the differential output signals must cross.
V _{REF}	Reference voltage for SSTL, HSTL, and HSUL I/O Standards.
V _{REF(AC)}	AC input reference voltage for SSTL, HSTL, and HSUL I/O Standards. $V_{REF(AC)} = V_{REF(DC)} + \text{noise}$. The peak-to-peak AC noise on V _{REF} should not exceed 2% of V _{REF(DC)} .
V _{REF(DC)}	DC input reference voltage for SSTL, HSTL, and HSUL I/O Standards.
V _{SWING (AC)}	AC differential input voltage: AC Input differential voltage required for switching.
V _{SWING (DC)}	DC differential input voltage: DC Input differential voltage required for switching.
V _{TT}	Termination voltage for SSTL, HSTL, and HSUL I/O Standards.
V _{X (AC)}	AC differential Input cross point voltage: The voltage at which the differential input signals must cross.

Document Revision History for the Intel MAX 10 FPGA Device Datasheet

Document Version	Changes
2018.06.29	- Removed links on instant-on feature. - Added JTAG timing specifications term in <i>Glossary</i>. - Renamed the following IP cores as per Intel rebranding: - Renamed Altera Modular ADC IP core to Modular ADC core Intel FPGA IP core. - Renamed Altera Modular Dual ADC IP core to Modular Dual ADC core Intel FPGA IP core.



Date	Version	Changes
		- Added –A6 speed grade in the following tables: - Intel MAX 10 Device Grades and Speed Grades Supported - Series OCT without Calibration Specifications for Intel MAX 10 Devices - Clock Tree Specifications for Intel MAX 10 Devices - Embedded Multiplier Specifications for Intel MAX 10 Devices - Memory Block Performance Specifications for Intel MAX 10 Devices - True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices - True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices - Emulated RSDS_E_1R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices - True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices - True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices - Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices - LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices - IOE Programmable Delay on Row Pins for Intel MAX 10 Devices - IOE Programmable Delay on Column Pins for Intel MAX 10 Devices - Updated the maximum value for input clock cycle-to-cycle jitter ($t_{INJITTER_CCJ}$) with $F_{INPFD} < 100$ MHz condition from 750 ps to ± 750 ps in PLL Specifications for Intel MAX 10 Devices table. - Updated the dual supply mode performance in Embedded Multiplier Specifications for Intel MAX 10 Devices table. - Updated the dual supply mode performance in Memory Block Performance Specifications for Intel MAX 10 Devices table. - Added typical specifications in Internal Oscillator Frequencies for Intel MAX 10 Devices table. - Updated specifications in UFM Performance Specifications for Intel MAX 10 Devices table. - Updated sampling window specifications in LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices table. - Updated IOE programmable delay for row and column pins. - Changed instances of <i>Quartus II</i> to <i>Quartus Prime</i>.
June 2015	2015.06.12	- Updated the maximum values in Internal Weak Pull-Up Resistor for Intel MAX 10 Devices table. - Removed Internal Weak Pull-Up Resistor equation. - Updated the note for input resistance and input capacitance parameters in the ADC Performance Specifications table for both single supply and dual supply devices. Note: Download the SPICE models for simulation. - Added a note to AC Accuracy - THD, SNR, and SINAD parameters in the ADC Performance Specifications for Intel MAX 10 Dual Supply Devices table. Note: When using internal V_{REF}, THD = 66 dB, SNR = 58 dB and SINAD = 57.5 dB for dedicated ADC input channels. - Updated clock period jitter and cycle-to-cycle period jitter parameters in the Memory Output Clock Jitter Specifications for Intel MAX 10 Devices table.
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