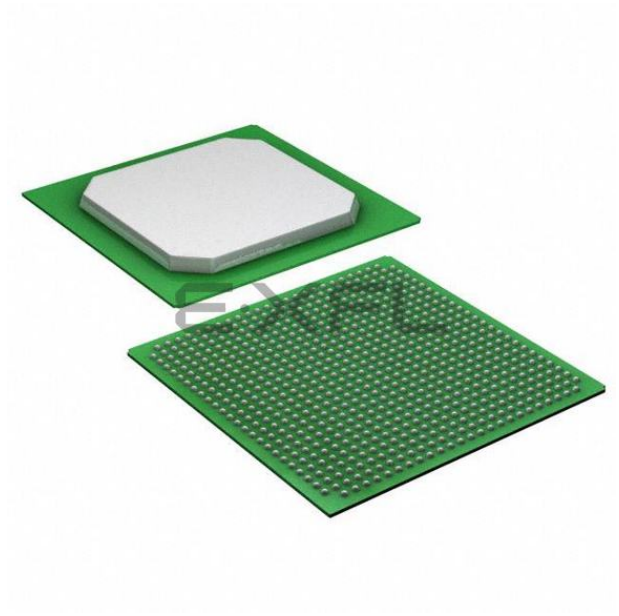

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	3125
Number of Logic Elements/Cells	50000
Total RAM Bits	1677312
Number of I/O	500
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10m50dcf672c7g

Operating Conditions

Intel MAX 10 devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Intel MAX 10 devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions for Intel MAX 10 devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Caution: Conditions outside the range listed in the absolute maximum ratings tables may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Single Supply Devices Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings for Intel MAX 10 Single Supply Devices

Symbol	Parameter	Min	Max	Unit
V_{CC_ONE}	Supply voltage for core and periphery through on-die voltage regulator	–0.5	3.9	V
V_{CCIO}	Supply voltage for input and output buffers	–0.5	3.9	V
V_{CCA}	Supply voltage for phase-locked loop (PLL) regulator and analog-to-digital converter (ADC) block (analog)	–0.5	3.9	V

Dual Supply Devices Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings for Intel MAX 10 Dual Supply Devices

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply voltage for core and periphery	–0.5	1.63	V
V_{CCIO}	Supply voltage for input and output buffers	–0.5	3.9	V
V_{CCA}	Supply voltage for PLL regulator (analog)	–0.5	3.41	V

continued...

Symbol	Parameter	Min	Max	Unit
V_{CCD_PLL}	Supply voltage for PLL regulator (digital)	–0.5	1.63	V
V_{CCA_ADC}	Supply voltage for ADC analog block	–0.5	3.41	V
V_{CCINT}	Supply voltage for ADC digital block	–0.5	1.63	V

Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings for Intel MAX 10 Devices

Symbol	Parameter	Min	Max	Unit
V_I	DC input voltage	–0.5	4.12	V
I_{OUT}	DC output current per pin	–25	25	mA
T_{STG}	Storage temperature	–65	150	°C
T_J	Operating junction temperature	–40	125	°C

Maximum Allowed Overshoot During Transitions over a 11.4-Year Time Frame

During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 4.17 V can only be at 4.17 V for ~11.7% over the lifetime of the device; for a device lifetime of 11.4 years, this amounts to 1.33 years.

Table 5. Maximum Allowed Overshoot During Transitions over a 11.4-Year Time Frame for Intel MAX 10 Devices

Condition (V)	Overshoot Duration as % of High Time	Unit
4.12	100.0	%
4.17	11.7	%
4.22	7.1	%
4.27	4.3	%

continued...

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		1.35 V	1.2825	1.35	1.4175	V
		1.2 V	1.14	1.2	1.26	V
V_{CCA} (1)	Supply voltage for PLL regulator and ADC block (analog)	—	2.85/3.135	3.0/3.3	3.15/3.465	V

Dual Supply Devices Power Supplies Recommended Operating Conditions

Table 7. Power Supplies Recommended Operating Conditions for Intel MAX 10 Dual Supply Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CC}	Supply voltage for core and periphery	—	1.15	1.2	1.25	V
V_{CCIO} (3)	Supply voltage for input and output buffers	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.35 V	1.2825	1.35	1.4175	V
		1.2 V	1.14	1.2	1.26	V
V_{CCA}(4)	Supply voltage for PLL regulator (analog)	—	2.375	2.5	2.625	V
V_{CCD_PLL}(5)	Supply voltage for PLL regulator (digital)	—	1.15	1.2	1.25	V
V_{CCA_ADC}	Supply voltage for ADC analog block	—	2.375	2.5	2.625	V
V_{CCINT}	Supply voltage for ADC digital block	—	1.15	1.2	1.25	V

(3) V_{CCIO} for all I/O banks must be powered up during user mode because V_{CCIO} I/O banks are used for the ADC and I/O functionalities.

(4) All V_{CCA} pins must be powered to 2.5 V (even when PLLs are not used), and must be powered up and powered down at the same time.

(5) V_{CCD_PLL} must always be connected to V_{CC} through a decoupling capacitor and ferrite bead.

Series OCT without Calibration Specifications

Table 13. Series OCT without Calibration Specifications for Intel MAX 10 Devices

This table shows the variation of on-chip termination (OCT) without calibration across process, voltage, and temperature (PVT).

Description	V_{CCIO} (V)	Resistance Tolerance		Unit
		–C7, –I6, –I7, –A6, –A7	–C8	
Series OCT without calibration	3.00	±35	±30	%
	2.50	±35	±30	%
	1.80	±40	±35	%
	1.50	±40	±40	%
	1.35	±40	±50	%
	1.20	±45	±60	%

Series OCT with Calibration at Device Power-Up Specifications

Table 14. Series OCT with Calibration at Device Power-Up Specifications for Intel MAX 10 Devices

OCT calibration is automatically performed at device power-up for OCT enabled I/Os.

Description	V_{CCIO} (V)	Calibration Accuracy	Unit
Series OCT with calibration at device power-up	3.00	±12	%
	2.50	±12	%
	1.80	±12	%
	1.50	±12	%
	1.35	±12	%
	1.20	±12	%

OCT Variation after Calibration at Device Power-Up

The OCT resistance may vary with the variation of temperature and voltage after calibration at device power-up.

Use the following table and equation to determine the final OCT resistance considering the variations after calibration at device power-up.

Pin Capacitance

Table 16. Pin Capacitance for Intel MAX 10 Devices

Symbol	Parameter	Maximum	Unit
C_{IOB}	Input capacitance on bottom I/O pins	8	pF
C_{IOLRT}	Input capacitance on left/right/top I/O pins	7	pF
C_{LVDSB}	Input capacitance on bottom I/O pins with dedicated LVDS output (9)	8	pF
C_{ADCL}	Input capacitance on left I/O pins with ADC input (10)	9	pF
$C_{VREFLRT}$	Input capacitance on left/right/top dual purpose V_{REF} pin when used as V_{REF} or user I/O pin (11)	48	pF
C_{VREFB}	Input capacitance on bottom dual purpose V_{REF} pin when used as V_{REF} or user I/O pin	50	pF
C_{CLKB}	Input capacitance on bottom dual purpose clock input pins (12)	7	pF
C_{CLKLRT}	Input capacitance on left/right/top dual purpose clock input pins (12)	6	pF

Internal Weak Pull-Up Resistor

All I/O pins, except configuration, test, and JTAG pins, have an option to enable weak pull-up.

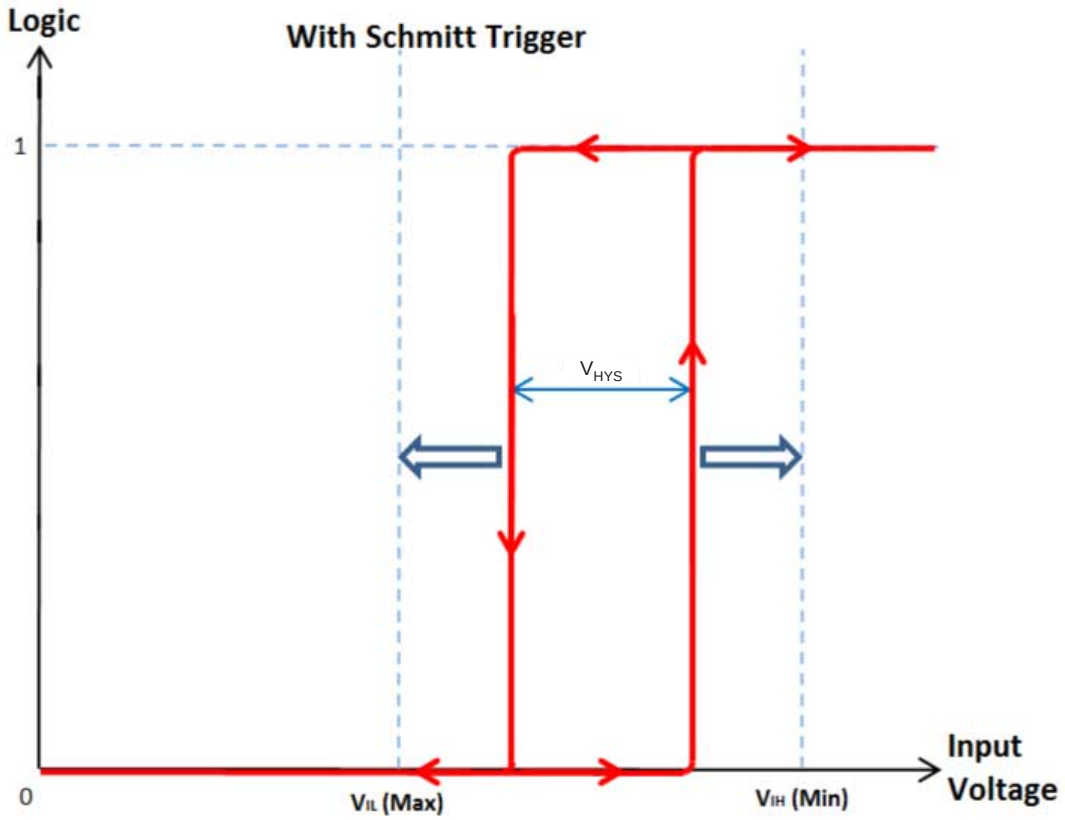
(9) Dedicated LVDS output buffer is only available at bottom I/O banks.

(10) ADC pins are only available at left I/O banks.

(11) When V_{REF} pin is used as regular input or output, F_{max} performance is reduced due to higher pin capacitance. Using the V_{REF} pin capacitance specification from device datasheet, perform SI analysis on your board setup to determine the F_{max} of your system.

(12) 10M40 and 10M50 devices have dual purpose clock input pins at top/bottom I/O banks.

Figure 4. Schmitt Trigger Input Standard Voltage Diagram



I/O Standards Specifications

Tables in this section list input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Intel MAX 10 devices.

For minimum voltage values, use the minimum V_{CCIO} values. For maximum voltage values, use the maximum V_{CCIO} values.

You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.

Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

Table 21. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Intel MAX 10 Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V) (14)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	1.19	1.25	1.31	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.7	1.8	1.9	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-135 Class I, II	1.283	1.35	1.45	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	0.85	0.9	0.95
HSTL-15 Class I, II	1.425	1.5	1.575	0.71	0.75	0.79	0.71	0.75	0.79
HSTL-12 Class I, II	1.14	1.2	1.26	0.48 × V_{CCIO} (15)	0.5 × V_{CCIO} (15)	0.52 × V_{CCIO} (15)	—	0.5 × V_{CCIO}	—
				0.47 × V_{CCIO} (16)	0.5 × V_{CCIO} (16)	0.53 × V_{CCIO} (16)			
HSUL-12	1.14	1.2	1.3	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	—	—	—

(14) V_{TT} of transmitting device must track V_{REF} of the receiving device.

(15) Value shown refers to DC input reference voltage, $V_{REF(DC)}$.

(16) Value shown refers to AC input reference voltage, $V_{REF(AC)}$.

Table 24. Differential HSTL and HSUL I/O Standards Specifications for Intel MAX 10 Devices

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.85	—	0.95	0.85	—	0.95	0.4
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.71	—	0.79	0.71	—	0.79	0.4
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO}	0.48 × V_{CCIO}	0.5 × V_{CCIO}	0.52 × V_{CCIO}	0.48 × V_{CCIO}	0.5 × V_{CCIO}	0.52 × V_{CCIO}	0.3
HSUL-12	1.14	1.2	1.3	0.26	—	0.5 × V_{CCIO} – 0.12	0.5 × V_{CCIO}	0.5 × V_{CCIO} + 0.12	0.4 × V_{CCIO}	0.5 × V_{CCIO}	0.6 × V_{CCIO}	0.44

Differential I/O Standards Specifications

Table 25. Differential I/O Standards Specifications for Intel MAX 10 Devices

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)		V_{ICM} (V) (18)			V_{OD} (mV) (19)(20)			V_{OS} (V) (19)		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVPECL (21)	2.375	2.5	2.625	100	—	0.05	D_{MAX} ≤ 500 Mbps	1.8	—	—	—	—	—	—
						0.55	500 Mbps ≤ D_{MAX} ≤ 700 Mbps	1.8						
						1.05	D_{MAX} > 700 Mbps	1.55						
LVDS	2.375	2.5	2.625	100	—	0.05	D_{MAX} ≤ 500 Mbps	1.8	247	—	600	1.125	1.25	1.375
						0.55	500 Mbps ≤ D_{MAX} ≤ 700 Mbps	1.8						

continued...

(18) V_{IN} range: 0 V ≤ V_{IN} ≤ 1.85 V.

(19) R_L range: 90 ≤ R_L ≤ 110 Ω.

(20) Low V_{OD} setting is only supported for RSDS standard.

(21) LVPECL input standard is only supported at clock input. Output standard is not supported.

Core Performance Specifications

Clock Tree Specifications

Table 26. Clock Tree Specifications for Intel MAX 10 Devices

Device	Performance					Unit
	–I6	–A6, –C7	–I7	–A7	–C8	
10M02	450	416	416	382	402	MHz
10M04	450	416	416	382	402	MHz
10M08	450	416	416	382	402	MHz
10M16	450	416	416	382	402	MHz
10M25	450	416	416	382	402	MHz
10M40	450	416	416	382	402	MHz
10M50	450	416	416	382	402	MHz

PLL Specifications

Table 27. PLL Specifications for Intel MAX 10 Devices

V_{CCD_PLL} should always be connected to V_{CCINT} through decoupling capacitor and ferrite bead.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{IN} (28)	Input clock frequency	—	5	—	472.5	MHz
f_{INPFD}	Phase frequency detector (PFD) input frequency	—	5	—	325	MHz

continued...

(28) This parameter is limited in the Intel Quartus Prime software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

Embedded Multiplier Specifications

Table 30. Embedded Multiplier Specifications for Intel MAX 10 Devices

Mode	Number of Multipliers	Power Supply Mode	Performance			Unit
			–I6	–A6, –C7, –I7, –A7	–C8	
9 × 9-bit multiplier	1	Single supply mode	198	183	160	MHz
		Dual supply mode	310	260	210	MHz
18 × 18-bit multiplier	1	Single supply mode	198	183	160	MHz
		Dual supply mode	265	240	190	MHz

Memory Block Performance Specifications

Table 31. Memory Block Performance Specifications for Intel MAX 10 Devices

Memory	Mode	Resources Used		Power Supply Mode	Performance			Unit
		LEs	M9K Memory		–I6	–A6, –C7, –I7, –A7	–C8	
M9K Block	FIFO 256 × 36	47	1	Single supply mode	232	219	204	MHz
				Dual supply mode	330	300	250	MHz
	Single-port 256 × 36	0	1	Single supply mode	232	219	204	MHz
				Dual supply mode	330	300	250	MHz
	Simple dual-port 256 × 36 CLK	0	1	Single supply mode	232	219	204	MHz
				Dual supply mode	330	300	250	MHz
	True dual port 512 × 18 single CLK	0	1	Single supply mode	232	219	204	MHz
				Dual supply mode	330	300	250	MHz

Parameter		Symbol	Condition	Min	Typ	Max	Unit
	Integral non linearity	INL	—	–2	—	2	LSB
AC Accuracy	Total harmonic distortion	THD	F_{IN} = 50 kHz, F_S = 1 MHz, PLL	–65 (37)	—	—	dB
	Signal-to-noise ratio	SNR	F_{IN} = 50 kHz, F_S = 1 MHz, PLL	54 (38)	—	—	dB
	Signal-to-noise and distortion	SINAD	F_{IN} = 50 kHz, F_S = 1 MHz, PLL	53 (39)	—	—	dB
On-Chip Temperature Sensor	Temperature sampling rate	T_S	—	—	—	50	kSPS
	Absolute accuracy	—	–40 to 125°C, with 64 samples averaging (40)	—	—	±10	°C
Conversion Rate (41)	Conversion time	—	Single measurement	—	—	1	Cycle
			Continuous measurement	—	—	1	Cycle
			Temperature measurement	—	—	1	Cycle

Related Information

SPICE Models for Intel FPGAs

(37) THD with prescalar enabled is 6dB less than the specification.

(38) SNR with prescalar enabled is 6dB less than the specification.

(39) SINAD with prescalar enabled is 6dB less than the specification.

(40) For the Intel Quartus Prime software version 15.0 and later, Modular ADC Core Intel FPGA IP and Modular Dual ADC Core Intel FPGA IP cores handle the 64 samples averaging. For the Intel Quartus Prime software versions prior to 14.1, you need to implement your own averaging calculation.

(41) For more detailed description, refer to the Timing section in the *Intel MAX 10 Analog-to-Digital Converter User Guide*.

True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications

Table 36. True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

True **PPDS** transmitter is only supported at bottom I/O banks. Emulated **PPDS** transmitter is supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	—	155	5	—	155	5	—	155	MHz
		×8	5	—	155	5	—	155	5	—	155	MHz
		×7	5	—	155	5	—	155	5	—	155	MHz
		×4	5	—	155	5	—	155	5	—	155	MHz
		×2	5	—	155	5	—	155	5	—	155	MHz
		×1	5	—	310	5	—	310	5	—	310	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	—	310	100	—	310	100	—	310	Mbps
		×8	80	—	310	80	—	310	80	—	310	Mbps
		×7	70	—	310	70	—	310	70	—	310	Mbps
		×4	40	—	310	40	—	310	40	—	310	Mbps
		×2	20	—	310	20	—	310	20	—	310	Mbps
		×1	10	—	310	10	—	310	10	—	310	Mbps
f_{HSCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	—	150	5	—	150	5	—	150	MHz
		×8	5	—	150	5	—	150	5	—	150	MHz
		×7	5	—	150	5	—	150	5	—	150	MHz
		×4	5	—	150	5	—	150	5	—	150	MHz
		×2	5	—	150	5	—	150	5	—	150	MHz
		×1	5	—	300	5	—	300	5	—	300	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	—	300	100	—	300	100	—	300	Mbps
		×8	80	—	300	80	—	300	80	—	300	Mbps
		×7	70	—	300	70	—	300	70	—	300	Mbps

continued...

True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications

Single Supply Devices True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications

Table 37. True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices

True **RSDS** transmitter is only supported at bottom I/O banks. Emulated **RSDS** transmitter is supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	—	50	5	—	50	5	—	50	MHz
		×8	5	—	50	5	—	50	5	—	50	MHz
		×7	5	—	50	5	—	50	5	—	50	MHz
		×4	5	—	50	5	—	50	5	—	50	MHz
		×2	5	—	50	5	—	50	5	—	50	MHz
		×1	5	—	100	5	—	100	5	—	100	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	—	100	100	—	100	100	—	100	Mbps
		×8	80	—	100	80	—	100	80	—	100	Mbps
		×7	70	—	100	70	—	100	70	—	100	Mbps
		×4	40	—	100	40	—	100	40	—	100	Mbps
		×2	20	—	100	20	—	100	20	—	100	Mbps
		×1	10	—	100	10	—	100	10	—	100	Mbps
f_{HSCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	—	50	5	—	50	5	—	50	MHz
		×8	5	—	50	5	—	50	5	—	50	MHz
		×7	5	—	50	5	—	50	5	—	50	MHz
		×4	5	—	50	5	—	50	5	—	50	MHz
		×2	5	—	50	5	—	50	5	—	50	MHz
		×1	5	—	100	5	—	100	5	—	100	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	—	100	100	—	100	100	—	100	Mbps

continued...

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		×8	80	—	100	80	—	100	80	—	100	Mbps
		×7	70	—	100	70	—	100	70	—	100	Mbps
		×4	40	—	100	40	—	100	40	—	100	Mbps
		×2	20	—	100	20	—	100	20	—	100	Mbps
		×1	10	—	100	10	—	100	10	—	100	Mbps
t_{DUTY}	Duty cycle on transmitter output clock	—	45	—	55	45	—	55	45	—	55	%
TCCS(55)	Transmitter channel-to-channel skew	—	—	—	300	—	—	300	—	—	300	ps
$t_{x\ Jitter}$(56)	Output jitter (high-speed I/O performance pin)	—	—	—	425	—	—	425	—	—	425	ps
	Output jitter (low-speed I/O performance pin)	—	—	—	470	—	—	470	—	—	470	ps
t_{RISE}	Rise time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	Fall time	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration	—	—	—	1	—	—	1	—	—	1	ms

(55) TCCS specifications apply to I/O banks from the same side only.

(56) TX jitter is the jitter induced from core noise and I/O switching noise.

Dual Supply Devices Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications

Table 44. Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

Emulated **LVDS_E_3R**, **SLVS**, and **Sub-LVDS** transmitters are supported at the output pin of all I/O banks.

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7			–A7			–C8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	Input clock frequency (high-speed I/O performance pin)	×10	5	—	300	5	—	275	5	—	275	MHz
		×8	5	—	300	5	—	275	5	—	275	MHz
		×7	5	—	300	5	—	275	5	—	275	MHz
		×4	5	—	300	5	—	275	5	—	275	MHz
		×2	5	—	300	5	—	275	5	—	275	MHz
		×1	5	—	300	5	—	275	5	—	275	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	—	600	100	—	550	100	—	550	Mbps
		×8	80	—	600	80	—	550	80	—	550	Mbps
		×7	70	—	600	70	—	550	70	—	550	Mbps
		×4	40	—	600	40	—	550	40	—	550	Mbps
		×2	20	—	600	20	—	550	20	—	550	Mbps
		×1	10	—	300	10	—	275	10	—	275	Mbps
f_{HSCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	—	150	5	—	150	5	—	150	MHz
		×8	5	—	150	5	—	150	5	—	150	MHz
		×7	5	—	150	5	—	150	5	—	150	MHz
		×4	5	—	150	5	—	150	5	—	150	MHz
		×2	5	—	150	5	—	150	5	—	150	MHz
		×1	5	—	300	5	—	300	5	—	300	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	—	300	100	—	300	100	—	300	Mbps
		×8	80	—	300	80	—	300	80	—	300	Mbps

continued...

Symbol	Parameter	Mode	–I6, –A6, –C7, –I7		–A7		–C8		Unit
			Min	Max	Min	Max	Min	Max	
		×2	5	360	5	320	5	320	MHz
		×1	5	360	5	320	5	320	MHz
HSIODR	Data rate (high-speed I/O performance pin)	×10	100	700	100	640	100	640	Mbps
		×8	80	720	80	640	80	640	Mbps
		×7	70	700	70	640	70	640	Mbps
		×4	40	720	40	640	40	640	Mbps
		×2	20	720	20	640	20	640	Mbps
		×1	10	360	10	320	10	320	Mbps
f_{HSCLK}	Input clock frequency (low-speed I/O performance pin)	×10	5	150	5	150	5	150	MHz
		×8	5	150	5	150	5	150	MHz
		×7	5	150	5	150	5	150	MHz
		×4	5	150	5	150	5	150	MHz
		×2	5	150	5	150	5	150	MHz
		×1	5	300	5	300	5	300	MHz
HSIODR	Data rate (low-speed I/O performance pin)	×10	100	300	100	300	100	300	Mbps
		×8	80	300	80	300	80	300	Mbps
		×7	70	300	70	300	70	300	Mbps
		×4	40	300	40	300	40	300	Mbps
		×2	20	300	20	300	20	300	Mbps
		×1	10	300	10	300	10	300	Mbps
SW	Sampling window (high-speed I/O performance pin)	—	—	510	—	510	—	510	ps

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Programmable IOE Delay for Column Pins

Table 58. IOE Programmable Delay on Column Pins for Intel MAX 10 Devices

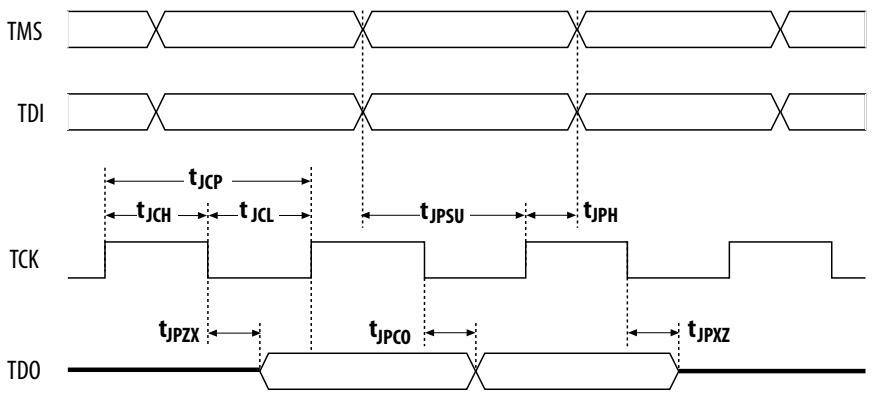
The incremental values for the settings are generally linear. For exact values of each setting, refer to the **Assignment Name** column in the latest version of the Intel Quartus Prime software.

The minimum and maximum offset timing numbers are in reference to setting '0' as available in the Intel Quartus Prime software.

Parameter	Paths Affected	Number of Settings	Minimum Offset	Maximum Offset							Unit
				Fast Corner		Slow Corner					
				–I7	–C8	–A6	–C7	–C8	–I7	–A7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	0.81	0.868	1.823	1.802	1.864	1.862	1.912	ns
Input delay from pin to input register	Pad to I/O input register	8	0	0.914	0.981	2.06	2.032	2.101	2.102	2.161	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.435	0.466	0.971	0.97	1.013	1.001	1.028	ns

Glossary

Table 59. Glossary

Term	Definition
JTAG Timing Specifications	
R_L	Receiver differential input discrete resistor (external to Intel MAX 10 devices).
RSKM (Receiver input skew margin)	HIGH-SPEED I/O block: The total margin left after accounting for the sampling window and TCCS. RSKM = (TUI – SW – TCCS) / 2.
Sampling window (SW)	HIGH-SPEED I/O Block: The period of time during which the data must be valid to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window.
Single-ended voltage referenced I/O standard	The AC input signal values indicate the voltage levels at which the receiver must meet its timing specifications. The DC input signal values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input crosses the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing.
t_C	High-speed receiver/transmitter input and output clock period.
TCCS (Channel-to- channel-skew)	HIGH-SPEED I/O block: The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
t_{cin}	Delay from clock pad to I/O input register.
t_{CO}	Delay from clock pad to I/O output.
t_{cout}	Delay from clock pad to I/O output register.

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Date	Version	Changes
January 2016	2016.01.22	• Added description about automotive temperature devices in the Programming/Erasure Specifications table. • Changed the pin capacitance to maximum values. • Updated maximum TCCS specifications from 410 ps to 300 ps in the following tables: — True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — Emulated RSDS_E_1R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — True LVDS Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices — True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices — Emulated LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices — Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices • Added new table: True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices. • Updated maximum f_{HSCLK} and HSIODR specifications for –A6, –C7, and –I7 speed grades in True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices table. • Updated SW specifications in the following tables: — LVDS Receiver Timing Specifications for Intel MAX 10 Single Supply Devices — LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices • Updated maximum f_{HSCLK} and HSIODR (high-speed I/O performance pin) specifications for –I6, –A6, –C7, –I7 speed grades in LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices table. • Removed Internal Configuration Time information in the Uncompressed .rbf Sizes for Intel MAX 10 Devices table. • Added Internal Configuration Time tables for uncompressed `.rbf` files and compressed `.rbf` files. • Removed Preliminary tags for all tables.
November 2015	2015.11.02	• Added description to *Maximum Allowed Overshoot During Transitions over a 11.4-Year Time Frame* topic. • Added ADC_VREF Pin Leakage Current for Intel MAX 10 Devices table. • Updated the condition for "Bus-hold high, sustaining current" parameter from "$V_{IN} < V_{IL}$ (minimum)" to "$V_{IN} < V_{IH}$ (minimum)" in Bus Hold Parameters table.

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Date	Version	Changes
		• Updated SSTL-2 Class I and II I/O standard specifications for JEDEC compliance as follows: — VIL(AC) Max: Updated from V_{REF} – 0.35 to V_{REF} – 0.31 — VIH(AC) Min: Updated from V_{REF} + 0.35 to V_{REF} + 0.31 • Added a note to BLVDS in Differential I/O Standards Specifications for Intel MAX 10 Devices table: BLVDS TX is not supported in single supply devices. • Added a link to MAX 10 High-Speed LVDS I/O User Guide for the list of I/O standards supported in single supply and dual supply devices. • Added a statement in PLL Specifications for Intel MAX 10 Single Supply Device table: For V36 package, the PLL specification is based on single supply devices. • Added Internal Oscillator Specifications from Intel MAX 10 Clocking and PLL User Guide. • Added UFM specifications for serial interface. • Updated total harmonic distortion (THD) specifications as follows: — Single supply devices: Updated from 65 dB to –65 dB — Dual supply devices: Updated from 70 dB to –70 dB (updated from 65 dB to –65 dB for dual function pin) • Added condition for On-Chip Temperature Sensor—Absolute accuracy parameter in ADC Performance Specifications for Intel MAX 10 Dual Supply Devices table. The condition is: with 64 samples averaging. • Updated the description in Periphery Performance Specifications to mention that proper timing closure is required in design. • Updated HSIODR and f_{HSCLK} specifications for x10 and x7 modes in True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices. • Added specifications for low-speed I/O performance pin sampling window in LVDS Receiver Timing Specifications for Intel MAX 10 Single Supply Devices table: Max = 900 ps for –C7, –I7, –A7, and –C8 speed grades. • Added $t_{RU\_nCONFIG}$ and $t_{RU\_nRSTIMER}$ specifications for different devices in Remote System Upgrade Circuitry Timing Specifications for Intel MAX 10 Devices table. • Removed the word "internal oscillator" in User Watchdog Timer Specifications for Intel MAX 10 Devices table to avoid confusion. • Added IOE programmable delay specifications.
September 2014	2014.09.22	Initial release.