Infineon Technologies - MB96F348TSAPMC-GSE2 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	82
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f348tsapmc-gse2

- Controller Area Network (CAN) - License of Robert Bosch GmbH

■ PIN DESCRIPTION FOR MB96(F)32x, MB96(F)34x, MB96(F)35x, MB96(F)36x

PIN DESCRIPTION FOR MB96(F)32x, MB96(F)34x, MB96(F)35x, MB96(F)36x

Pin no.					Pin name	Circuit type	Function
MB9632x	MB9634x		MB9635x	MB9636x			
LQFP80*5	LQFP100*2	QFP100*1	LQFP64*3	LQFP48*4			
58	90	92	46	28	X1	A	Oscillation output
59	91	93	47	27	X0		Oscillation input
55	52	54	45	23	RSTX	E	Reset input
30	75	77	24		P00_0	H	General purpose I/O
					AD00		External bus interface (non-multiplexed mode) data line External bus interface (multiplexed mode) address/ data line
					INT8		External interrupt request input pin for INT8
					SCK7_R		Relocated USART7 serial clock I/O (not available on MB96F348H/T)
					TTG8_R		Relocated PPG8 trigger
31	76	78	25		P00_1	H	General purpose I/O
					AD01		External bus interface (non-multiplexed mode) data line External bus interface (multiplexed mode) address/ data line
					INT9		External interrupt request input pin for INT9
					SOT7_R		Relocated USART 7 serial data output (not available on MB96F348H/T)
					TTG9_R		Relocated PPG9 trigger

PIN DESCRIPTION FOR MB96(F)32x, MB96(F)34x, MB96(F)35x, MB96(F)36x

Pin no.					Pin name	Circuit type	Function
MB9632x	MB9634x		MB9635x	MB9636x			
LQFP80*5	LQFP100*2	QFP100*1	LQFP64*3	LQFP48*4			
16	28	30	15	18	P05_6	I	General purpose IO
					AN14		A/D converter analog input
					INT4_R		Relocated External Interrupt INT4 input
17	29	31		19	P05_7	I	General purpose IO
					AN15		A/D converter analog input
					INT5_R		Relocated External Interrupt INT5 input
					OUT10_R		Output Compare Unit OCU10 waveform reloacted output pin
78,79, 3 to 5	34 to 38	36 to 40	62, 63, 3 to 5	62, 63, 3 to 5	P06_0 to P06_4	I	General purpose IO
					AN0 to AN4		A/D converter analog input
					PPG0 to PPG4		Programmable Pulse Generator outputs
					CS0_R to CS4_R		External Chip selects relocated output
6	39	41	6	6	P06_5	I	General purpose IO
					AN5		A/D converter analog input
					PPG5		Programmable Pulse Generator outputs
					CS5_R		External Chip select relocated output
7	40	42	7	7	P06_6	I	General purpose IO
					AN6		A/D converter analog input
					PPG6		Programmable Pulse Generator outputs

PIN DESCRIPTION FOR MB96(F)32x, MB96(F)34x, MB96(F)35x, MB96(F)36x

Pin no.					Pin name	Circuit type	Function
MB9632x	MB9634x		MB9635x	MB9636x			
LQFP80*5	LQFP100*2	QFP100*1	LQFP64*3	LQFP48*4			
63					P17_2	I	General purpose IO
					FRCK3		Free Running Timer3 input
					TTG17		Programmable Pulse Generators PPG17 trigger
20					P17_6	I	General purpose IO
					OCU11		Output Compare Unit OCU11 waveform output pin
					IN10		Input Capture Unit ICU10 data sample input
					TTG18		Programmable Pulse Generators PPG18 trigger
					INT3_R		Relocated input of external interrupt INT3
29					P17_7	I	General purpose IO
					IN11		Input Capture Unit ICU11 data sample input
					TTG19		Programmable Pulse Generators PPG19 trigger
80	30	32	64	1	AVCC	F	Analog circuits VCC power supply
2	31	33	2	2	AVRH	G	A/D converter upper reference voltage Supply voltage to AVCC pin must be kept higher than or equal to AVRH pin voltage specially when the supply voltage to AVRH is turned on or off
	32	34			AVRL	F	A/D converter lower reference voltage
1	33	35	1	48	AVSS	F	Analog circuits VSS power supply

PIN DESCRIPTION FOR MB96(F)38X

Pin no. MB96(F)38x LQFP120*1	Pin name	Circuit type	Function
86	P12_7	J	General purpose I/O
	INT1_R		Relocated external interrupt 1
	HRQ		External bus Hold Request
	SEG11		LCD controller / driver segment output
87	P00_0	J	General purpose I/O
	INT3_R		Relocated external interrupt 3
	HAKX		External bus Hold Acknowlegde
	SEG12		LCD controller / driver segment output
88	P00_1	J	General purpose I/O
	INT4_R		Relocated external interrupt 4
	WRHX		External bus High byte Write strobe
	SEG13		LCD controller / driver segment output
89	P00_2	J	General purpose I/O
	INT5_R		Relocated external interrupt 5
	RDY		External bus external wait state request
	SEG14		LCD controller / driver segment output
92	P00_3	J	General purpose I/O
	INT6_R		Relocated external interrupt 6
	A00		External bus (non-multiplexed mode) address line
	CS3_R		External bus relocated Chip Select 3
	SEG15		LCD controller / driver segment output
93	P00_4	J	General purpose I/O
	INT7_R		Relocated external interrupt 7
	ALE		External bus Address Latch Enable signal
	SEG16		LCD controller / driver segment output

PIN DESCRIPTION FOR MB96(F)38X

Pin no. MB96(F)38x LQFP120*1	Pin name	Circuit type	Function
26, 27	P05_0, P05_1	K	General purpose I/O
	AN8, AN9		A/D converter inputs
	ALARM0, ALARM1		Alarm comparator 0, 1 inputs
	SEG57, SEG58		LCD controller / driver segment outputs
28	P05_2	K	General purpose I/O
	AN10		A/D converter inputs
	OUT2		Output Compare Unit 2 and 3 waveform output pins
	SGO1		SGO output of Sound Generator 1
	SEG59		LCD controller / driver segment outputs
29	P05_3	K	General purpose I/O
	AN11		A/D converter inputs
	OUT3		Output Compare Unit 2 and 3 waveform output pins
	SGA1		SGA output of Sound Generator 1
	SEG60		LCD controller / driver segment outputs
32	P05_4	K	General purpose I/O
	AN12		A/D converter input
	RX1		CAN controller 1 data receive
	INT2_R		Relocated External Interrupt 2 input
	SEG61		LCD controller / driver segment output
33	P05_5	K	General purpose I/O
	AN13		A/D converter input
	TX1		CAN controller 1 data transmit
	SEG62		LCD controller / driver segment output

- Connect VCC and VSS to the device from the power supply with lowest possible impedance.
- As a measure against power supply noise, connect a capacitor of about 0.1 µF as a bypass capacitor between VCC and VSS as close as possible to VCC and VSS pins.

7. Crystal Oscillator Circuit

- Noise at X0 or X1 pins may possibly cause abnormal operation. Make sure to provide bypass capacitors with shortest distance to X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuit not cross the lines of other circuits.
- It is highly recommended to provide a printed circuit board art work surrounding X0 and X1 pins with a ground area for stabilizing the operation.

8. Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

- Make sure to turn on the A/D converter power supply (AVCC, AVRH, AVRL) and analog inputs (ANn) after turning-on the digital power supply (VCC).
- Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AVRH or AVCC (turning on/off the analog and digital power supplies simultaneously is acceptable).

9. Connection of Unused Pins of A/D Converter

- Connect unused pins of A/D converter as AVCC = VCC, AVSS = AVRH = AVRL = VSS.

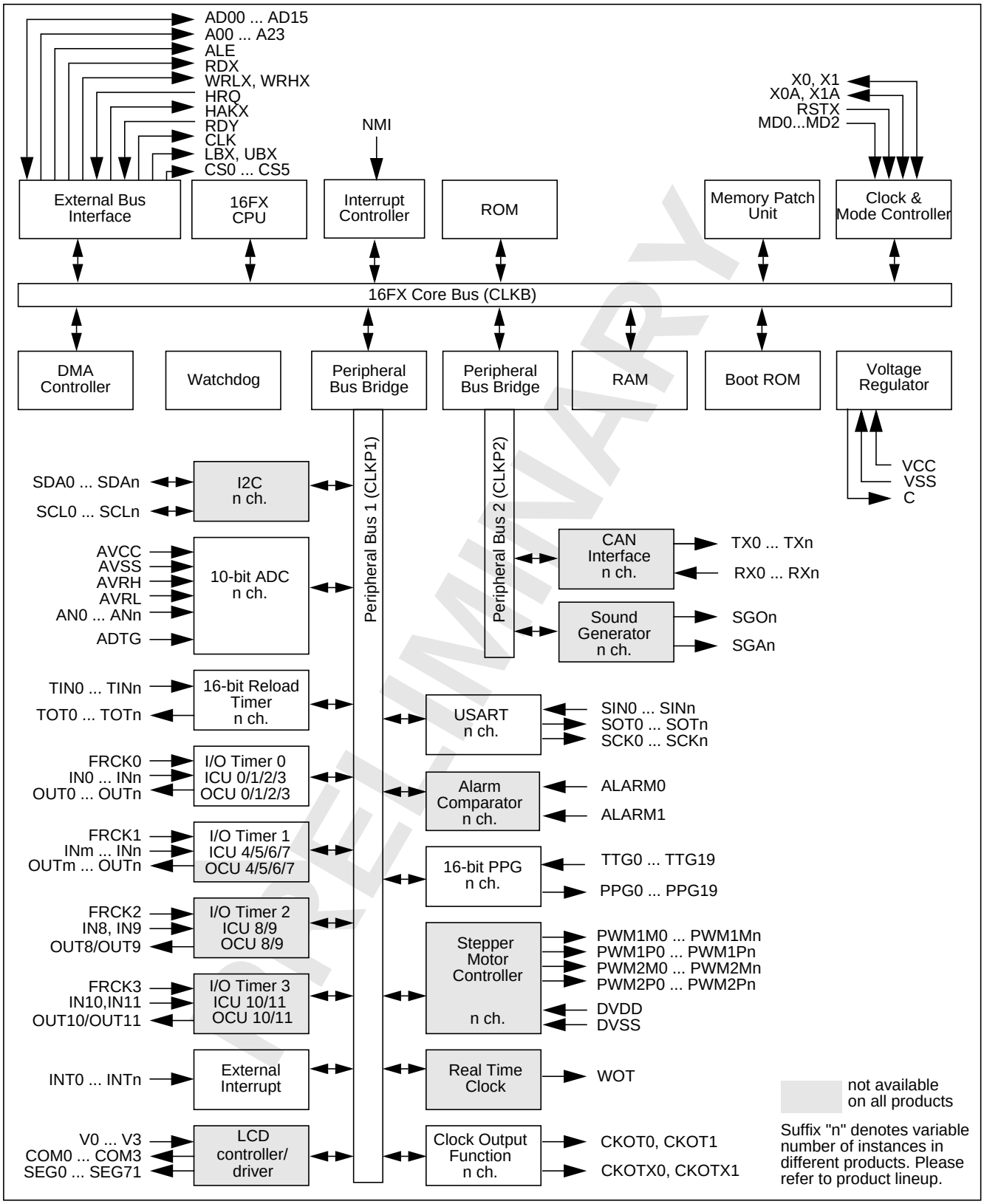
10. Notes on Energization

- To prevent malfunction of the internal voltage regulator, supply voltage profile while turning on the power supply should be slower than 50us from 0.2 V to 2.7 V.

11. Stabilization of power supply voltage

- If the power supply voltage varies acutely even within the operation assurance range of the Vcc power supply voltage, a malfunction may occur. The Vcc power supply voltage must therefore be stabilized. As stabilization guidelines, stabilize the power supply voltage so that Vcc ripple fluctuations (peak to peak value) in the commercial frequencies (50 to 60 Hz) fall within 10% of the standard Vcc power supply voltage and the transient fluctuation rate becomes 0.1V/µs or less in instantaneous fluctuation for power supply switching.

Block Diagram of MB963xx



■ RAMSTART for different RAM sizes

Devices	RAM size	RAMSTART
	1 kB	7E40
	2 kB	7A40
	3 kB	7640
	4 kB	7240
	5 kB	6E40
MB96344, MB96F365, MB96384, MB96385	6 kB	6A40
	7 kB	6640
	8 kB	6240
	9 kB	5E40
	10 kB	5A40
	11 kB	5640
MB96F326, MB96F356	12 kB	5240
	13 kB	4E40
	14 kB	4A40
	15 kB	4640
MB96(F)346, MB96(F)347, MB96(F)386, MB96(F)387	16 kB	4240
	17 kB	3E40
	18 kB	3A40
	19 kB	3640
	20 kB	3240
	21 kB	2E40
	22 kB	2A40
	23 kB	2640
MB96F348	24 kB	2240
	25 kB	1E40
	26 kB	1A40
	27 kB	1640
	28 kB	1240

Table 0-1 I/O map (3 / 53)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00003FH	OCU - Compare Register 7			RW
000040H	ICU - Control Status Register 0/1	ICS01		RW
000041H	ICU - Edge register 0/1	ICE01		RW
000042H	ICU - Capture Register 0	IPCPL0	IPCP0	R
000043H	ICU - Capture Register 0	IPCPH0		R
000044H	ICU - Capture Register 1	IPCPL1	IPCP1	R
000045H	ICU - Capture Register 1	IPCPH1		R
000046H	ICU - Control Status Register 2/3	ICS23		RW
000047H	ICU - Edge register 2/3	ICE23		RW
000048H	ICU - Capture Register 2	IPCPL2	IPCP2	R
000049H	ICU - Capture Register 2	IPCPH2		R
00004AH	ICU - Capture Register 3	IPCPL3	IPCP3	R
00004BH	ICU - Capture Register 3	IPCPH3		R
00004CH	ICU - Control Status Register 4/5	ICS45		RW
00004DH	ICU - Edge register 4/5	ICE45		RW
00004EH	ICU - Capture Register 4	IPCPL4	IPCP4	R
00004FH	ICU - Capture Register 4	IPCPH4		R
000050H	ICU - Capture Register 5	IPCPL5	IPCP5	R
000051H	ICU - Capture Register 5	IPCPH5		R
000052H	ICU - Control Status Register 6/7	ICS67		RW
000053H	ICU - Edge register 6/7	ICE67		RW
000054H	ICU - Capture Register 6	IPCPL6	IPCP6	R
000055H	ICU - Capture Register 6	IPCPH6		R
000056H	ICU - Capture Register 7	IPCPL7	IPCP7	R
000057H	ICU - Capture Register 7	IPCPH7		R
000058H	External Interrupt - Enable Register 0	ENIR0		RW
000059H	External Interrupt - Interrupt request Register 0	EIRR0		RW
00005AH	External Interrupt - Level Select 0	ELVRL0	ELVR0	RW
00005BH	External Interrupt - Level Select 0	ELVRH0		RW

Table 0-1 I/O map (10 / 53)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000108H	DMA - Buffer address pointer low byte	BAPL1		RW
000109H	DMA - Buffer address pointer middle byte	BAPM1		RW
00010AH	DMA - Buffer address pointer high byte	BAPH1		RW
00010BH	DMA - DMA control register	DMACS1		RW
00010CH	DMA - I/O register address pointer low byte	IOAL1	IOA1	RW
00010DH	DMA - I/O register address pointer high byte	IOAH1		RW
00010EH	DMA - Data counter low byte	DCTL1	DCT1	RW
00010FH	DMA - Data counter high byte	DCTH1		RW
000110H	DMA - Buffer address pointer low byte	BAPL2		RW
000111H	DMA - Buffer address pointer middle byte	BAPM2		RW
000112H	DMA - Buffer address pointer high byte	BAPH2		RW
000113H	DMA - DMA control register	DMACS2		RW
000114H	DMA - I/O register address pointer low byte	IOAL2	IOA2	RW
000115H	DMA - I/O register address pointer high byte	IOAH2		RW
000116H	DMA - Data counter low byte	DCTL2	DCT2	RW
000117H	DMA - Data counter high byte	DCTH2		RW
000118H	DMA - Buffer address pointer low byte	BAPL3		RW
000119H	DMA - Buffer address pointer middle byte	BAPM3		RW
00011AH	DMA - Buffer address pointer high byte	BAPH3		RW
00011BH	DMA - DMA control register	DMACS3		RW
00011CH	DMA - I/O register address pointer low byte	IOAL3	IOA3	RW
00011DH	DMA - I/O register address pointer high byte	IOAH3		RW
00011EH	DMA - Data counter low byte	DCTL3	DCT3	RW
00011FH	DMA - Data counter high byte	DCTH3		RW
000120H	DMA - Buffer address pointer low byte	BAPL4		RW
000121H	DMA - Buffer address pointer middle byte	BAPM4		RW

Table 0-1 I/O map (13 / 53)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000156H	DMA - Data counter low byte	DCTL10	DCT10	RW
000157H	DMA - Data counter high byte	DCTH10		RW
000158H	DMA - Buffer address pointer low byte	BAPL11		RW
000159H	DMA - Buffer address pointer middle byte	BAPM11		RW
00015AH	DMA - Buffer address pointer high byte	BAPH11		RW
00015BH	DMA - DMA control register	DMACS11		RW
00015CH	DMA - I/O register address pointer low byte	IOAL11	IOA11	RW
00015DH	DMA - I/O register address pointer high byte	IOAH11		RW
00015EH	DMA - Data counter low byte	DCTL11	DCT11	RW
00015FH	DMA - Data counter high byte	DCTH11		RW
000160H	DMA - Buffer address pointer low byte	BAPL12		RW
000161H	DMA - Buffer address pointer middle byte	BAPM12		RW
000162H	DMA - Buffer address pointer high byte	BAPH12		RW
000163H	DMA - DMA control register	DMACS12		RW
000164H	DMA - I/O register address pointer low byte	IOAL12	IOA12	RW
000165H	DMA - I/O register address pointer high byte	IOAH12		RW
000166H	DMA - Data counter low byte	DCTL12	DCT12	RW
000167H	DMA - Data counter high byte	DCTH12		RW
000168H	DMA - Buffer address pointer low byte	BAPL13		RW
000169H	DMA - Buffer address pointer middle byte	BAPM13		RW
00016AH	DMA - Buffer address pointer high byte	BAPH13		RW
00016BH	DMA - DMA control register	DMACS13		RW
00016CH	DMA - I/O register address pointer low byte	IOAL13	IOA13	RW
00016DH	DMA - I/O register address pointer high byte	IOAH13		RW
00016EH	DMA - Data counter low byte	DCTL13	DCT13	RW
00016FH	DMA - Data counter high byte	DCTH13		RW

Table 0-1 I/O map (24 / 53)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0004ADH	I/O Port - Pull-Up resistor Control Register Port 05	PUCR05		RW
0004AEH	I/O Port - Pull-Up resistor Control Register Port 06	PUCR06		RW
0004AFH	I/O Port - Pull-Up resistor Control Register Port 07	PUCR07		RW
0004B0H	I/O Port - Pull-Up resistor Control Register Port 08	PUCR08		RW
0004B1H	I/O Port - Pull-Up resistor Control Register Port 09	PUCR09		RW
0004B2H	I/O Port - Pull-Up resistor Control Register Port 10	PUCR10		RW
0004B3H	I/O Port - Pull-Up resistor Control Register Port 11	PUCR11		RW
0004B4H	I/O Port - Pull-Up resistor Control Register Port 12	PUCR12		RW
0004B5H	I/O Port - Pull-Up resistor Control Register Port 13	PUCR13		RW
0004B6H	I/O Port - Pull-Up resistor Control Register Port 14	PUCR14		RW
0004B7H	I/O Port - Pull-Up resistor Control Register Port 15	PUCR15		RW
0004B8H	I/O Port - Pull-Up resistor Control Register Port 16	PUCR16		RW
0004B9H	I/O Port - Pull-Up resistor Control Register Port 17	PUCR17		RW
0004BCH	I/O Port - External Pin State Register Port 00	EPSR00		R
0004BDH	I/O Port - External Pin State Register Port 01	EPSR01		R
0004BEH	I/O Port - External Pin State Register Port 02	EPSR02		R
0004BFH	I/O Port - External Pin State Register Port 03	EPSR03		R
0004C0H	I/O Port - External Pin State Register Port 04	EPSR04		R

Table 0-1 I/O map (27 / 53)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0004F2H	RLT - Timer Control Status Register 4 Low	TMCSRL4	TMCSR4	RW
0004F3H	RLT - Timer Control Status Register 4 High	TMCSRH4		RW
0004F4H	RLT - Reload Register 4 - for writing		TMRLR4	W
0004F4H	RLT - Reload Register 4 - for reading		TMR4	R
0004F5H	RLT - Reload Register 4 - for writing			W
0004F5H	RLT - Reload Register 4 - for reading			R
0004F6H	RLT - Timer Control Status Register 5 Low	TMCSRL5	TMCSR5	RW
0004F7H	RLT - Timer Control Status Register 5 High	TMCSRH5		RW
0004F8H	RLT - Reload Register 5 - for writing		TMRLR5	W
0004F8H	RLT - Reload Register 5 - for reading		TMR5	R
0004F9H	RLT - Reload Register 5 - for writing			W
0004F9H	RLT - Reload Register 5 - for reading			R
0004FAH	RLT - Timer input select (for Cascading)	TMISR		RW
000500H	FRT - Data register of free-running timer 2		TCDT2	RW
000501H	FRT - Data register of free-running timer 2			RW
000502H	FRT - Control status register of free-running timer 2	TCCSL2	TCCS2	RW
000503H	FRT - Control status register of free-running timer 2	TCCSH2		RW
000504H	FRT - Data register of free-running timer 3		TCDT3	RW
000505H	FRT - Data register of free-running timer 3			RW
000506H	FRT - Control status register of free-running timer 3	TCCSL3	TCCS3	RW
000507H	FRT - Control status register of free-running timer 3	TCCSH3		RW
000508H	OCU - Output Compare Control Status 8	OCS8		RW
000509H	OCU - Output Compare Control Status 9	OCS9		RW
00050AH	OCU - Compare Register 8		OCCP8	RW
00050BH	OCU - Compare Register 8			RW
00050CH	OCU - Compare Register 9		OCCP9	RW

Table 0-1 I/O map (30 / 53)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000545H	LIN USART - Baud Rate Generator Register 7	BGRH7		RW
000548H	LIN USART - Serial Mode Register 8	SMR8		RW
000549H	LIN USART - Serial Control Register 8	SCR8		RW
00054AH	LIN USART - Serial TX Register 8	TDR8		W
00054AH	LIN USART - Serial RX Register 8	RDR8		R
00054BH	LIN USART - Serial Status Register 8	SSR8		RW
00054CH	LIN USART - Ext. Control/Com. Register 8	ECCR8		RW
00054DH	LIN USART - Ext. Status Com. Register 8	ESCR8		RW
00054EH	LIN USART - Baud Rate Generator Register 8	BGRL8	BGR8	RW
00054FH	LIN USART - Baud Rate Generator Register 8	BGRH8		RW
000552H	LIN USART - Serial Mode Register 9	SMR9		RW
000553H	LIN USART - Serial Control Register 9	SCR9		RW
000554H	LIN USART - Serial TX Register 9	TDR9		W
000554H	LIN USART - Serial RX Register 9	RDR9		R
000555H	LIN USART - Serial Status Register 9	SSR9		RW
000556H	LIN USART - Ext. Control/Com. Register 9	ECCR9		RW
000557H	LIN USART - Ext. Status Com. Register 9	ESCR9		RW
000558H	LIN USART - Baud Rate Generator Register 9	BGRL9	BGR9	RW
000559H	LIN USART - Baud Rate Generator Register 9	BGRH9		RW
000560H	Alarm Comparator 0	ACSR0		RW
000561H	Alarm Comparator 0	AECSR0		RW
000562H	Alarm Comparator 1	ACSR1		RW
000563H	Alarm Comparator 1	AECSR1		RW
000564H	PPG - Timer register 6		PTMR6	R
000565H	PPG - Timer register 6			R
000566H	PPG - Period setting register 6		PCSR6	W
000567H	PPG - Period setting register 6			W

Table 0-1 I/O map (41 / 53)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000743H	CAN 0 - IF2 Command Mask register (reserved	IF2CMSKH0		R
000744H	CAN 0 - IF2 Mask Register	IF2MSK1L0	IF2MSK10	RW
000745H	CAN 0 - IF2 Mask Register	IF2MSK1H0		RW
000746H	CAN 0 - IF2 Mask Register	IF2MSK2L0	IF2MSK20	RW
000747H	CAN 0 - IF2 Mask Register	IF2MSK2H0		RW
000748H	CAN 0 - IF2 Arbitration register	IF2ARB1L0	IF2ARB10	RW
000749H	CAN 0 - IF2 Arbitration register	IF2ARB1H0		RW
00074AH	CAN 0 - IF2 Arbitration register	IF2ARB2L0	IF2ARB20	RW
00074BH	CAN 0 - IF2 Arbitration register	IF2ARB2H0		RW
00074CH	CAN 0 - IF2 Message Control Register	IF2MCTRL0	IF2MCTR0	RW
00074DH	CAN 0 - IF2 Message Control Register	IF2MCTRH0		RW
00074EH	CAN 0 - IF2 Data A1	IF2DTA1L0	IF2DTA10	RW
00074FH	CAN 0 - IF2 Data A1	IF2DTA1H0		RW
000750H	CAN 0 - IF2 Data A2	IF2DTA2L0	IF2DTA20	RW
000751H	CAN 0 - IF2 Data A2	IF2DTA2H0		RW
000752H	CAN 0 - IF2 Data B1	IF2DTB1L0	IF2DTB10	RW
000753H	CAN 0 - IF2 Data B1	IF2DTB1H0		RW
000754H	CAN 0 - IF2 Data B2	IF2DTB2L0	IF2DTB20	RW
000755H	CAN 0 - IF2 Data B2	IF2DTB2H0		RW
000780H	CAN 0 - Transmission Request Register	TREQR1L0	TREQR10	R
000781H	CAN 0 - Transmission Request Register	TREQR1H0		R
000782H	CAN 0 - Transmission Request Register	TREQR2L0	TREQR20	R
000783H	CAN 0 - Transmission Request Register	TREQR2H0		R
000790H	CAN 0 - New Data Register	NEWDT1L0	NEWDT10	R
000791H	CAN 0 - New Data Register	NEWDT1H0		R
000792H	CAN 0 - New Data Register	NEWDT2L0	NEWDT20	R
000793H	CAN 0 - New Data Register	NEWDT2H0		R
0007A0H	CAN 0 - Interrupt Pending Register	INTPND1L0	INTPND10	R
0007A1H	CAN 0 - Interrupt Pending Register	INTPND1H0		R

Table 0-1 I/O map (42 / 53)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0007A2H	CAN 0 - Interrupt Pending Register	INTPND2L0	INTPND20	R
0007A3H	CAN 0 - Interrupt Pending Register	INTPND2H0		R
0007B0H	CAN 0 - Message Valid Register	MSGVAL1L0	MSGVAL10	R
0007B1H	CAN 0 - Message Valid Register	MSGVAL1H0		R
0007B2H	CAN 0 - Message Valid Register	MSGVAL2L0	MSGVAL20	R
0007B3H	CAN 0 - Message Valid Register	MSGVAL2H0		R
0007CEH	CAN 0 - Output enable register	COER0		RW
0007D0H	Sound Generator 0 - Control Register Low	SGCRL0	SGCR0	RW
0007D1H	Sound Generator 0 - Control Register High	SGCRH0		RW
0007D2H	Sound Generator 0 - Frequency Register	SGFR0		RW
0007D3H	Sound Generator 0 - Amplitude Register	SGAR0		RW
0007D4H	Sound Generator 0 - Decrement Register	SGDR0		RW
0007D5H	Sound Generator 0 - Tone Register	SGTR0		RW
0007D6H	Sound Generator 1 - Control Register Low	SGCRL1	SGCR1	RW
0007D7H	Sound Generator 1 - Control Register High	SGCRH1		RW
0007D8H	Sound Generator 1 - Frequency Register	SGFR1		RW
0007D9H	Sound Generator 1 - Amplitude Register	SGAR1		RW
0007DAH	Sound Generator 1 - Decrement Register	SGDR1		RW
0007DBH	Sound Generator 1 - Tone Register	SGTR1		RW
000800H	CAN 1 - Control register	CTRLRL1	CTRLR1	RW
000801H	CAN 1 - Control register (reserved)	CTRLRH1		R
000802H	CAN 1 - Status register	STATRL1	STATR1	RW
000803H	CAN 1 - Status register (reserved)	STATRH1		R
000804H	CAN 1 - Error Counter (Transmit)	ERRCNTL1	ERRCNT1	R
000805H	CAN 1 - Error Counter (Receive)	ERRCNTH1		R
000806H	CAN 1 - Bit Timing Register	BTRL1	BTR1	RW
000807H	CAN 1 - Bit Timing Register	BTRH1		RW
000808H	CAN 1 - Interrupt Register	INTRL1	INTR1	R

Table 0-1 I/O map (43 / 53)

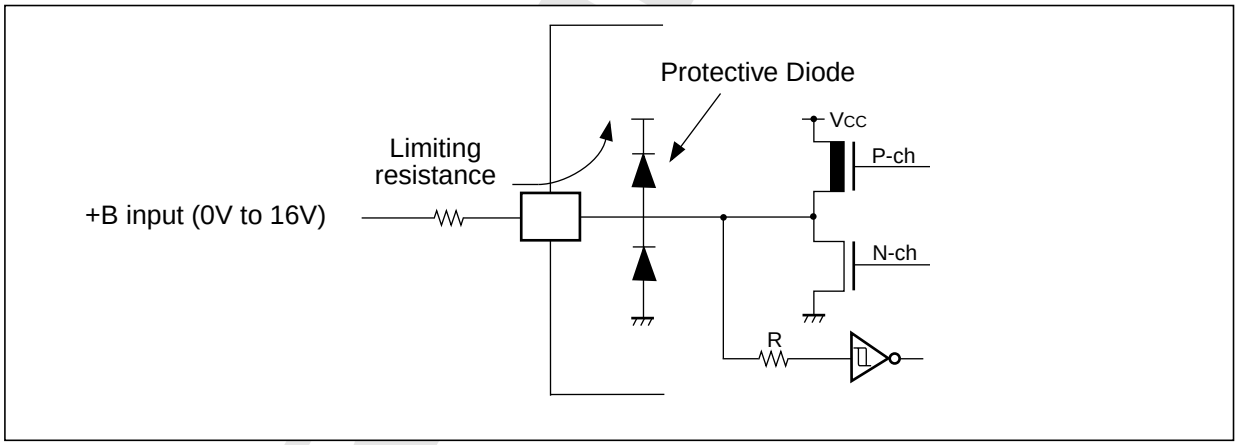
Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000809H	CAN 1 - Interrupt Register	INTRH1		R
00080AH	CAN 1 - Test Register	TESTRL1	TESTR1	RW
00080BH	CAN 1 - Test Register (reserved)	TESTRH1		R
00080CH	CAN 1 - BRP Extension register	BRPERL1	BRPER1	RW
00080DH	CAN 1 - BRP Extension register (reserved)	BRPERH1		R
000810H	CAN 1 - IF1 Command request register	IF1CREQL1	IF1CREQ1	RW
000811H	CAN 1 - IF1 Command request register	IF1CREQH1		RW
000812H	CAN 1 - IF1 Command Mask register	IF1CMSKL1	IF1CMSK1	RW
000813H	CAN 1 - IF1 Command Mask register (reserved)	IF1CMSKH1		R
000814H	CAN 1 - IF1 Mask Register	IF1MSK1L1	IF1MSK11	RW
000815H	CAN 1 - IF1 Mask Register	IF1MSK1H1		RW
000816H	CAN 1 - IF1 Mask Register	IF1MSK2L1	IF1MSK21	RW
000817H	CAN 1 - IF1 Mask Register	IF1MSK2H1		RW
000818H	CAN 1 - IF1 Arbitration register	IF1ARB1L1	IF1ARB11	RW
000819H	CAN 1 - IF1 Arbitration register	IF1ARB1H1		RW
00081AH	CAN 1 - IF1 Arbitration register	IF1ARB2L1	IF1ARB21	RW
00081BH	CAN 1 - IF1 Arbitration register	IF1ARB2H1		RW
00081CH	CAN 1 - IF1 Message Control Register	IF1MCTRL1	IF1MCTR1	RW
00081DH	CAN 1 - IF1 Message Control Register	IF1MCTRH1		RW
00081EH	CAN 1 - IF1 Data A1	IF1DTA1L1	IF1DTA11	RW
00081FH	CAN 1 - IF1 Data A1	IF1DTA1H1		RW
000820H	CAN 1 - IF1 Data A2	IF1DTA2L1	IF1DTA21	RW
000821H	CAN 1 - IF1 Data A2	IF1DTA2H1		RW
000822H	CAN 1 - IF1 Data B1	IF1DTB1L1	IF1DTB11	RW
000823H	CAN 1 - IF1 Data B1	IF1DTB1H1		RW
000824H	CAN 1 - IF1 Data B2	IF1DTB2L1	IF1DTB21	RW
000825H	CAN 1 - IF1 Data B2	IF1DTB2H1		RW
000840H	CAN 1 - IF2 Command request register	IF2CREQL1	IF2CREQ1	RW

*1: Set AV_{CC} and V_{CC} to the same voltage. Make sure that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

*2: If DV_{CC} is powered before V_{CC}, then SMC I/O pin state is undefined. To avoid this, we recommend to always power V_{CC} before DV_{CC}. It is not necessary to set V_{CC} and DV_{CC} to the same value.

*3: V_I and V_O should not exceed (D)V_{CC} + 0.3 V. V_I should not exceed the specified ratings. However if the maximun current to/from a input is limited by some means with external components, the I_{CLAMP} rating supercedes the V_I rating. Input/output voltages of high current ports depend on DV_{CC}, of other ports on V_{CC}.

*4:
- Applicable to all general purpose I/O pins (GP00_0 to GP17_7)
- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persitant low voltage reset in internal vector mode).
- When using the LCD controller, No +B signal must be applied to any LCD I/O pin (including unused SEG/COM pins).
- Sample recommended circuits:



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

(10) I2C Timing

TBD