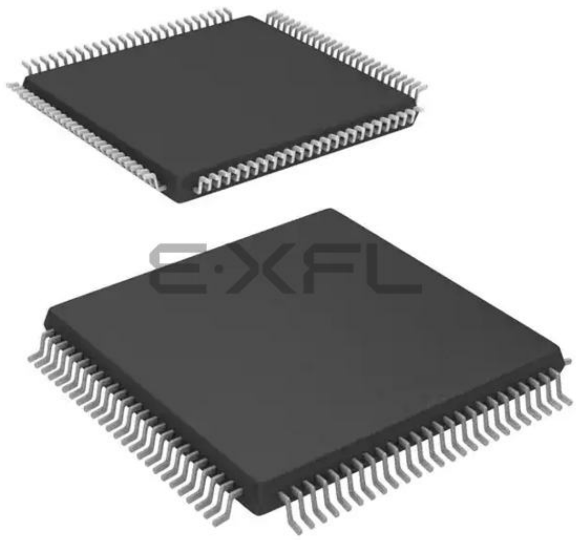

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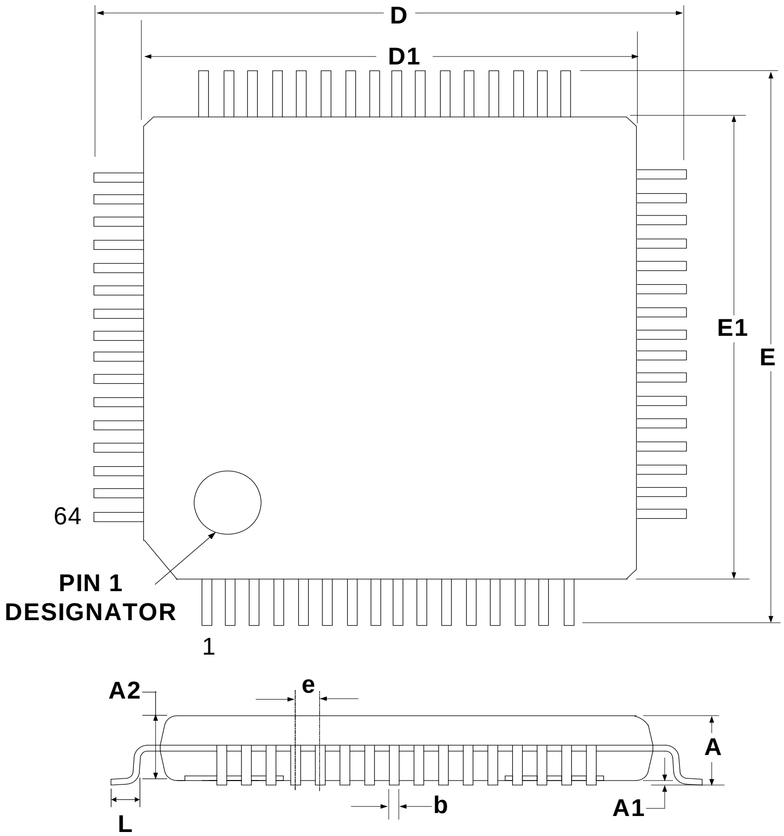
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	100MHz
Connectivity	EBI/EMI, SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	64
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8.25K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x8b, 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f120-gq

Table 4.1. Pin Definitions (Continued)

Name	Pin Numbers				Type	Description
	‘F120 ‘F122 ‘F124 ‘F126	‘F121 ‘F123 ‘F125 ‘F127	‘F130 ‘F132	‘F131 ‘F133		
ALE/P4.5	93		93		D I/O	ALE Strobe for External Memory Address bus (multiplexed mode) Port 4.5 See Port Input/Output section for complete description.
$\overline{RD}$/P4.6	92		92		D I/O	/RD Strobe for External Memory Address bus Port 4.6 See Port Input/Output section for complete description.
$\overline{WR}$/P4.7	91		91		D I/O	/WR Strobe for External Memory Address bus Port 4.7 See Port Input/Output section for complete description.
A8/P5.0	88		88		D I/O	Bit 8 External Memory Address bus (Non-multiplexed mode) Port 5.0 See Port Input/Output section for complete description.
A9/P5.1	87		87		D I/O	Port 5.1. See Port Input/Output section for complete description.
A10/P5.2	86		86		D I/O	Port 5.2. See Port Input/Output section for complete description.
A11/P5.3	85		85		D I/O	Port 5.3. See Port Input/Output section for complete description.
A12/P5.4	84		84		D I/O	Port 5.4. See Port Input/Output section for complete description.
A13/P5.5	83		83		D I/O	Port 5.5. See Port Input/Output section for complete description.
A14/P5.6	82		82		D I/O	Port 5.6. See Port Input/Output section for complete description.
A15/P5.7	81		81		D I/O	Port 5.7. See Port Input/Output section for complete description.



	MIN (mm)	NOM (mm)	MAX (mm)
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
D	-	12.00	-
D1	-	10.00	-
e	-	0.50	-
E	-	12.00	-
E1	-	10.00	-
L	0.45	0.60	0.75

Figure 4.6. TQFP-64 Package Drawing

5. ADC0 (12-Bit ADC, C8051F120/1/4/5 Only)

The ADC0 subsystem for the C8051F120/1/4/5 consists of a 9-channel, configurable analog multiplexer (AMUX0), a programmable gain amplifier (PGA0), and a 100 ksps, 12-bit successive-approximation-register ADC with integrated track-and-hold and Programmable Window Detector (see block diagram in Figure 5.1). The AMUX0, PGA0, Data Conversion Modes, and Window Detector are all configurable under software control via the Special Function Registers shown in Figure 5.1. The voltage reference used by ADC0 is selected as described in **Section "9. Voltage Reference" on page 113**. The ADC0 subsystem (ADC0, track-and-hold and PGA0) is enabled only when the AD0EN bit in the ADC0 Control register (ADC0CN) is set to logic 1. The ADC0 subsystem is in low power shutdown when this bit is logic 0.

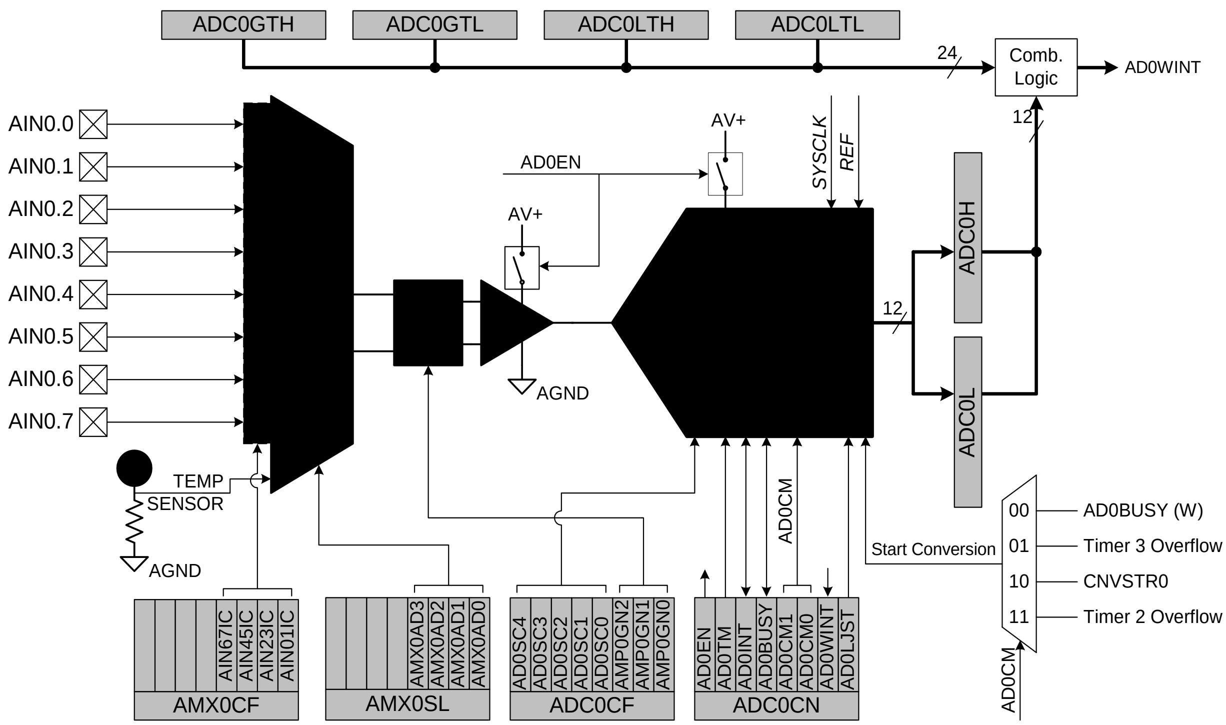


Figure 5.1. 12-Bit ADC0 Functional Block Diagram

5.1. Analog Multiplexer and PGA

Eight of the AMUX channels are available for external measurements while the ninth channel is internally connected to an on-chip temperature sensor (temperature transfer function is shown in Figure 5.2). AMUX input pairs can be programmed to operate in either differential or single-ended mode. This allows the user to select the best measurement technique for each input channel, and even accommodates mode changes "on-the-fly". The AMUX defaults to all single-ended inputs upon reset. There are two registers associated with the AMUX: the Channel Selection register AMX0SL (SFR Definition 5.2), and the Configuration register AMX0CF (SFR Definition 5.1). The table in SFR Definition 5.2 shows AMUX functionality by channel, for each possible configuration. The PGA amplifies the AMUX output signal by an amount determined by the states of the AMP0GN2-0 bits in the ADC0 Configuration register, ADC0CF (SFR Definition 5.3). The PGA can be software-programmed for gains of 0.5, 2, 4, 8 or 16. Gain defaults to unity on reset.

SFR Definition 5.4. ADC0CN: ADC0 Control

SFR Page: 0
SFR Address: 0xE8 (bit addressable)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
AD0EN	AD0TM	AD0INT	AD0BUSY	AD0CM1	AD0CM0	AD0WINT	AD0LJST	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bit7: AD0EN: ADC0 Enable Bit.
0: ADC0 Disabled. ADC0 is in low-power shutdown.
1: ADC0 Enabled. ADC0 is active and ready for data conversions.

Bit6: AD0TM: ADC Track Mode Bit.
0: When the ADC is enabled, tracking is continuous unless a conversion is in process.
1: Tracking Defined by ADCM1-0 bits.

Bit5: AD0INT: ADC0 Conversion Complete Interrupt Flag.
This flag must be cleared by software.
0: ADC0 has not completed a data conversion since the last time this flag was cleared.
1: ADC0 has completed a data conversion.

Bit4: AD0BUSY: ADC0 Busy Bit.
Read:
0: ADC0 Conversion is complete or a conversion is not currently in progress. AD0INT is set to logic 1 on the falling edge of AD0BUSY.
1: ADC0 Conversion is in progress.
Write:
0: No Effect.
1: Initiates ADC0 Conversion if AD0CM1-0 = 00b.

Bits3–2: AD0CM1–0: ADC0 Start of Conversion Mode Select.
If AD0TM = 0:
00: ADC0 conversion initiated on every write of ‘1’ to AD0BUSY.
01: ADC0 conversion initiated on overflow of Timer 3.
10: ADC0 conversion initiated on rising edge of external CNVSTR0.
11: ADC0 conversion initiated on overflow of Timer 2.
If AD0TM = 1:
00: Tracking starts with the write of ‘1’ to AD0BUSY and lasts for 3 SAR clocks, followed by conversion.
01: Tracking started by the overflow of Timer 3 and lasts for 3 SAR clocks, followed by conversion.
10: ADC0 tracks only when CNVSTR0 input is logic low; conversion starts on rising CNVSTR0 edge.
11: Tracking started by the overflow of Timer 2 and lasts for 3 SAR clocks, followed by conversion.

Bit1: AD0WINT: ADC0 Window Compare Interrupt Flag.
This bit must be cleared by software.
0: ADC0 Window Comparison Data match has not occurred since this flag was last cleared.
1: ADC0 Window Comparison Data match has occurred.

Bit0: AD0LJST: ADC0 Left Justify Select.
0: Data in ADC0H:ADC0L registers are right-justified.
1: Data in ADC0H:ADC0L registers are left-justified.

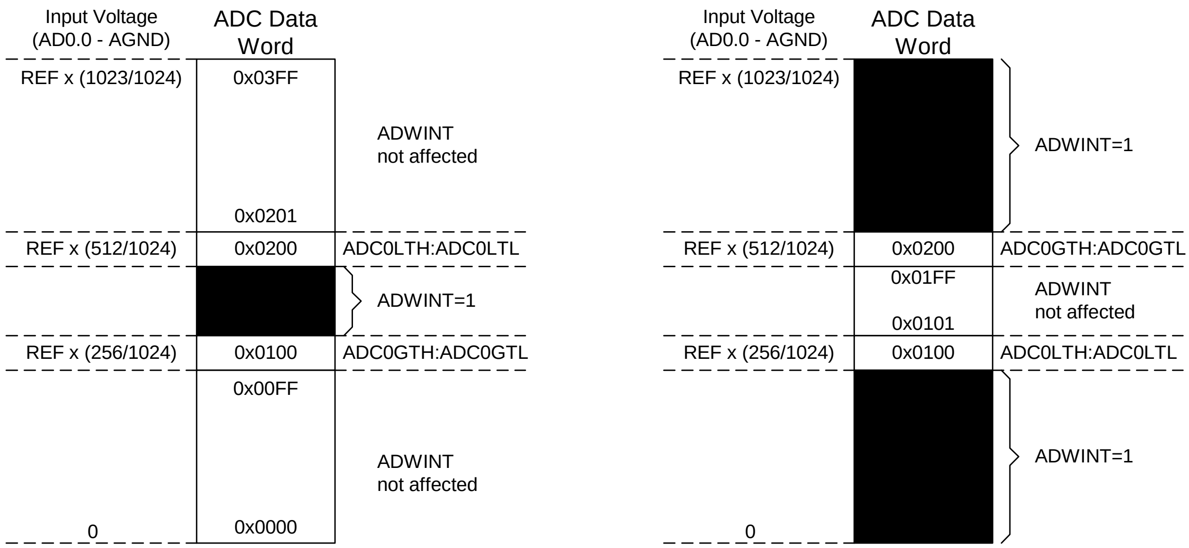
SFR Definition 6.2. AMX0SL: AMUX0 Channel Select

SFR Page: 0
SFR Address: 0xBB

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	AMX0AD3	AMX0AD2	AMX0AD1	AMX0AD0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits7–4: UNUSED. Read = 0000b; Write = don't care.
Bits3–0: AMX0AD3–0: AMX0 Address Bits.
0000-1111b: ADC Inputs selected per chart below.

AMX0CF Bits 3-0	AMX0AD3-0: 0000	0001	0010	0011	0100	0101	0110	0111	1xxx
0000	AIN0.0	AIN0.1	AIN0.2	AIN0.3	AIN0.4	AIN0.5	AIN0.6	AIN0.7	TEMP SENSOR
0001	+(AIN0.0) –(AIN0.1)		AIN0.2	AIN0.3	AIN0.4	AIN0.5	AIN0.6	AIN0.7	TEMP SENSOR
0010	AIN0.0	AIN0.1	+(AIN0.2) –(AIN0.3)		AIN0.4	AIN0.5	AIN0.6	AIN0.7	TEMP SENSOR
0011	+(AIN0.0) –(AIN0.1)		+(AIN0.2) –(AIN0.3)		AIN0.4	AIN0.5	AIN0.6	AIN0.7	TEMP SENSOR
0100	AIN0.0	AIN0.1	AIN0.2	AIN0.3	+(AIN0.4) –(AIN0.5)		AIN0.6	AIN0.7	TEMP SENSOR
0101	+(AIN0.0) –(AIN0.1)		AIN0.2	AIN0.3	+(AIN0.4) –(AIN0.5)		AIN0.6	AIN0.7	TEMP SENSOR
0110	AIN0.0	AIN0.1	+(AIN0.2) –(AIN0.3)		+(AIN0.4) –(AIN0.5)		AIN0.6	AIN0.7	TEMP SENSOR
0111	+(AIN0.0) –(AIN0.1)		+(AIN0.2) –(AIN0.3)		+(AIN0.4) –(AIN0.5)		AIN0.6	AIN0.7	TEMP SENSOR
1000	AIN0.0	AIN0.1	AIN0.2	AIN0.3	AIN0.4	AIN0.5	+(AIN0.6) –(AIN0.7)		TEMP SENSOR
1001	+(AIN0.0) –(AIN0.1)		AIN0.2	AIN0.3	AIN0.4	AIN0.5	+(AIN0.6) –(AIN0.7)		TEMP SENSOR
1010	AIN0.0	AIN0.1	+(AIN0.2) –(AIN0.3)		AIN0.4	AIN0.5	+(AIN0.6) –(AIN0.7)		TEMP SENSOR
1011	+(AIN0.0) –(AIN0.1)		+(AIN0.2) –(AIN0.3)		AIN0.4	AIN0.5	+(AIN0.6) –(AIN0.7)		TEMP SENSOR
1100	AIN0.0	AIN0.1	AIN0.2	AIN0.3	+(AIN0.4) –(AIN0.5)		+(AIN0.6) –(AIN0.7)		TEMP SENSOR
1101	+(AIN0.0) –(AIN0.1)		AIN0.2	AIN0.3	+(AIN0.4) –(AIN0.5)		+(AIN0.6) –(AIN0.7)		TEMP SENSOR
1110	AIN0.0	AIN0.1	+(AIN0.2) –(AIN0.3)		+(AIN0.4) –(AIN0.5)		+(AIN0.6) –(AIN0.7)		TEMP SENSOR
1111	+(AIN0.0) –(AIN0.1)		+(AIN0.2) –(AIN0.3)		+(AIN0.4) –(AIN0.5)		+(AIN0.6) –(AIN0.7)		TEMP SENSOR



Given:
AMX0SL = 0x00, AMX0CF = 0x00
AD0LJST = ‘0’,
ADC0LTH:ADC0LTL = 0x0200,
ADC0GTH:ADC0GTL = 0x0100.
An ADC0 End of Conversion will cause an ADC0 Window Compare Interrupt (AD0WINT = ‘1’) if the resulting ADC0 Data Word is < 0x0200 and > 0x0100.

Given:
AMX0SL = 0x00, AMX0CF = 0x00,
AD0LJST = ‘0’,
ADC0LTH:ADC0LTL = 0x0100,
ADC0GTH:ADC0GTL = 0x0200.
An ADC0 End of Conversion will cause an ADC0 Window Compare Interrupt (AD0WINT = ‘1’) if the resulting ADC0 Data Word is > 0x0200 or < 0x0100.

Figure 6.6. 10-Bit ADC0 Window Interrupt Example: Right Justified Single-Ended Data

8.1.1. Update Output On-Demand

In its default mode (DAC0CN.[4:3] = ‘00’) the DAC0 output is updated “on-demand” on a write to the high-byte of the DAC0 data register (DAC0H). It is important to note that writes to DAC0L are held, and have no effect on the DAC0 output until a write to DAC0H takes place. If writing a full 12-bit word to the DAC data registers, the 12-bit data word is written to the low byte (DAC0L) and high byte (DAC0H) data registers. Data is latched into DAC0 after a write to the corresponding DAC0H register, **so the write sequence should be DAC0L followed by DAC0H** if the full 12-bit resolution is required. The DAC can be used in 8-bit mode by initializing DAC0L to the desired value (typically 0x00), and writing data to only DAC0H (also see **Section 8.2** for information on formatting the 12-bit DAC data word within the 16-bit SFR space).

8.1.2. Update Output Based on Timer Overflow

Similar to the ADC operation, in which an ADC conversion can be initiated by a timer overflow independently of the processor, the DAC outputs can use a Timer overflow to schedule an output update event. This feature is useful in systems where the DAC is used to generate a waveform of a defined sampling rate by eliminating the effects of variable interrupt latency and instruction execution on the timing of the DAC output. When the DAC0MD bits (DAC0CN.[4:3]) are set to ‘01’, ‘10’, or ‘11’, writes to both DAC data registers (DAC0L and DAC0H) are held until an associated Timer overflow event (Timer 3, Timer 4, or Timer 2, respectively) occurs, at which time the DAC0H:DAC0L contents are copied to the DAC input latches allowing the DAC output to change to the new value.

8.2. DAC Output Scaling/Justification

In some instances, input data should be shifted prior to a DAC0 write operation to properly justify data within the DAC input registers. This action would typically require one or more load and shift operations, adding software overhead and slowing DAC throughput. To alleviate this problem, the data-formatting feature provides a means for the user to program the orientation of the DAC0 data word within data registers DAC0H and DAC0L. The three DAC0DF bits (DAC0CN.[2:0]) allow the user to specify one of five data word orientations as shown in the DAC0CN register definition.

DAC1 is functionally the same as DAC0 described above. The electrical specifications for both DAC0 and DAC1 are given in Table 8.1.

SFR Definition 10.3. CPT1CN: Comparator1 Control

SFR Page: 2
SFR Address: 0x88

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
CP1EN	CP1OUT	CP1RIF	CP1FIF	CP1HYP1	CP1HYP0	CP1HYN1	CP1HYN0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bit7: CP1EN: Comparator1 Enable Bit.
0: Comparator1 Disabled.
1: Comparator1 Enabled.

Bit6: CP1OUT: Comparator1 Output State Flag.
0: Voltage on CP1+ < CP1–.
1: Voltage on CP1+ > CP1–.

Bit5: CP1RIF: Comparator1 Rising-Edge Flag.
0: No Comparator1 Rising Edge has occurred since this flag was last cleared.
1: Comparator1 Rising Edge has occurred.

Bit4: CP1FIF: Comparator1 Falling-Edge Flag.
0: No Comparator1 Falling-Edge has occurred since this flag was last cleared.
1: Comparator1 Falling-Edge Interrupt has occurred.

Bits3–2: CP1HYP1–0: Comparator1 Positive Hysteresis Control Bits.
00: Positive Hysteresis Disabled.
01: Positive Hysteresis = 5 mV.
10: Positive Hysteresis = 10 mV.
11: Positive Hysteresis = 15 mV.

Bits1–0: CP1HYN1–0: Comparator1 Negative Hysteresis Control Bits.
00: Negative Hysteresis Disabled.
01: Negative Hysteresis = 5 mV.
10: Negative Hysteresis = 10 mV.
11: Negative Hysteresis = 15 mV.

SFR Definition 11.1. PSBANK: Program Space Bank Select

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	COBANK		-	-	IFBANK		00010001
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xB1
SFR Page: All Pages

Bits 7–6: Reserved.
Bits 5–4: COBANK: Constant Operations Bank Select.
These bits select which Flash bank is targeted during constant operations (MOVC and Flash MOVX) involving addresses 0x8000 to 0xFFFF. These bits are ignored when accessing the Scratchpad memory areas (see **Section “15. Flash Memory” on page 199**).
00: Constant Operations Target Bank 0 (note that Bank 0 is also mapped between 0x0000 to 0x7FFF).
01: Constant Operations Target Bank 1.
10: Constant Operations Target Bank 2.
11: Constant Operations Target Bank 3.
Bits 3–2: Reserved.
Bits 1–0: IFBANK: Instruction Fetch Operations Bank Select.
These bits select which Flash bank is used for instruction fetches involving addresses 0x8000 to 0xFFFF. These bits can only be changed from code in Bank 0 (see Figure 11.3).
00: Instructions Fetch From Bank 0 (note that Bank 0 is also mapped between 0x0000 to 0x7FFF).
01: Instructions Fetch From Bank 1.
10: Instructions Fetch From Bank 2.
11: Instructions Fetch From Bank 3.

***Note:** On the C8051F132/3, the COBANK and IFBANK bits should both remain set to the default setting of ‘01’ to ensure proper device functionality.

Internal Address	IFBANK = 0	IFBANK = 1	IFBANK = 2	IFBANK = 3
0xFFFF – 0x8000	Bank 0	Bank 1	Bank 2	Bank 3
0x7FFF – 0x0000	Bank 0	Bank 0	Bank 0	Bank 0

Figure 11.3. Address Memory Map for Instruction Fetches (128 kB Flash Only)

11.3.2. External Interrupts

Two of the external interrupt sources (/INT0 and /INT1) are configurable as active-low level-sensitive or active-low edge-sensitive inputs depending on the setting of bits IT0 (TCON.0) and IT1 (TCON.2). IE0 (TCON.1) and IE1 (TCON.3) serve as the interrupt-pending flag for the /INT0 and /INT1 external interrupts, respectively. If an /INT0 or /INT1 external interrupt is configured as edge-sensitive, the corresponding interrupt-pending flag is automatically cleared by the hardware when the CPU vectors to the ISR. When configured as level sensitive, the interrupt-pending flag follows the state of the external interrupt's input pin. The external interrupt source must hold the input active until the interrupt request is recognized. It must then deactivate the interrupt request before execution of the ISR completes or another interrupt request will be generated.

Table 11.4. Interrupt Summary

Interrupt Source	Interrupt Vector	Priority Order	Pending Flags	Bit addressable?	Cleared by HW?	SFRPAGE (SFRPGEN = 1)	Enable Flag	Priority Control
Reset	0x0000	Top	None	N/A	N/A	0	Always Enabled	Always Highest
External Interrupt 0 (/INT0)	0x0003	0	IE0 (TCON.1)	Y	Y	0	EX0 (IE.0)	PX0 (IP.0)
Timer 0 Overflow	0x000B	1	TF0 (TCON.5)	Y	Y	0	ET0 (IE.1)	PT0 (IP.1)
External Interrupt 1 (/INT1)	0x0013	2	IE1 (TCON.3)	Y	Y	0	EX1 (IE.2)	PX1 (IP.2)
Timer 1 Overflow	0x001B	3	TF1 (TCON.7)	Y	Y	0	ET1 (IE.3)	PT1 (IP.3)
UART0	0x0023	4	RI0 (SCON0.0) TI0 (SCON0.1)	Y		0	ES0 (IE.4)	PS0 (IP.4)
Timer 2	0x002B	5	TF2 (TMR2CN.7) EXF2 (TMR2CN.6)	Y		0	ET2 (IE.5)	PT2 (IP.5)
Serial Peripheral Interface	0x0033	6	SPIF (SPI0CN.7) WCOL (SPI0CN.6) MODF (SPI0CN.5) RXOVRN (SPI0CN.4)	Y		0	ESPI0 (EIE1.0)	PSPI0 (EIP1.0)
SMBus Interface	0x003B	7	SI (SMB0CN.3)	Y		0	ESMB0 (EIE1.1)	PSMB0 (EIP1.1)
ADC0 Window Comparator	0x0043	8	AD0WINT (ADC0CN.1)	Y		0	EWADC0 (EIE1.2)	PWADC0 (EIP1.2)
Programmable Counter Array	0x004B	9	CF (PCA0CN.7) CCFn (PCA0CN.n)	Y		0	EPCA0 (EIE1.3)	PPCA0 (EIP1.3)
Comparator 0 Falling Edge	0x0053	10	CP0FIF (CPT0CN.4)	Y		1	ECP0F (EIE1.4)	PCP0F (EIP1.4)
Comparator 0 Rising Edge	0x005B	11	CP0RIF (CPT0CN.5)	Y		1	ECP0R (EIE1.5)	PCP0R (EIP1.5)
Comparator 1 Falling Edge	0x0063	12	CP1FIF (CPT1CN.4)	Y		2	ECP1F (EIE1.6)	PCP1F (EIP1.6)

Electrical specifications for the precision internal oscillator are given in Table 14.1. Note that the system clock may be derived from the programmed internal oscillator divided by 1, 2, 4, or 8, as defined by the IFCN bits in register OSCICN.

SFR Definition 14.1. OSCICL: Internal Oscillator Calibration.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								Variable
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x8B
SFR Page: F

Bits 7–0: OSCICL: Internal Oscillator Calibration Register.
This register calibrates the internal oscillator period. The reset value for OSCICL defines the internal oscillator base frequency. The reset value is factory calibrated to generate an internal oscillator frequency of 24.5 MHz.

SFR Definition 14.2. OSCICN: Internal Oscillator Control

R/W	R	R/W	R	R/W	R/W	R/W	R/W	Reset Value
IOSCEN	IFRDY	-	-	-	-	IFCN1	IFCN0	11000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x8A
SFR Page: F

Bit 7: IOSCEN: Internal Oscillator Enable Bit.
0: Internal Oscillator Disabled.
1: Internal Oscillator Enabled.
Bit 6: IFRDY: Internal Oscillator Frequency Ready Flag.
0: Internal Oscillator not running at programmed frequency.
1: Internal Oscillator running at programmed frequency.
Bits 5–2: Reserved.
Bits 1–0: IFCN1-0: Internal Oscillator Frequency Control Bits.
00: Internal Oscillator is divided by 8.
01: Internal Oscillator is divided by 4.
10: Internal Oscillator is divided by 2.
11: Internal Oscillator is divided by 1.

SFR Definition 14.8. PLL0FLT: PLL Filter

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	PLLICO1	PLLICO0	PLLLP3	PLLLP2	PLLLP1	PLLLP0	00110001
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x8F
SFR Page: F

Bits 7–6: UNUSED: Read = 00b; Write = don't care.
Bits 5–4: PLLICO1-0: PLL Current-Controlled Oscillator Control Bits.
Selection is based on the desired output frequency, according to the following table:

PLL Output Clock	PLLICO1-0
65–100 MHz	00
45–80 MHz	01
30–60 MHz	10
25–50 MHz	11

Bits 3–0: PLLLP3-0: PLL Loop Filter Control Bits.
Selection is based on the divided PLL reference clock, according to the following table:

Divided PLL Reference Clock	PLLLP3-0
19–30 MHz	0001
12.2–19.5 MHz	0011
7.8–12.5 MHz	0111
5–8 MHz	1111

Table 14.2. PLL Frequency Characteristics

–40 to +85 °C unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Input Frequency (Divided Reference Frequency)		5		30	MHz
PLL Output Frequency		25		100*	MHz
***Note:** The maximum operating frequency of the C8051F124/5/6/7 is 50 MHz					

17.6.2.2. 8-bit MOVX without Bank Select: EMI0CF[4:2] = ‘001’ or ‘011’.

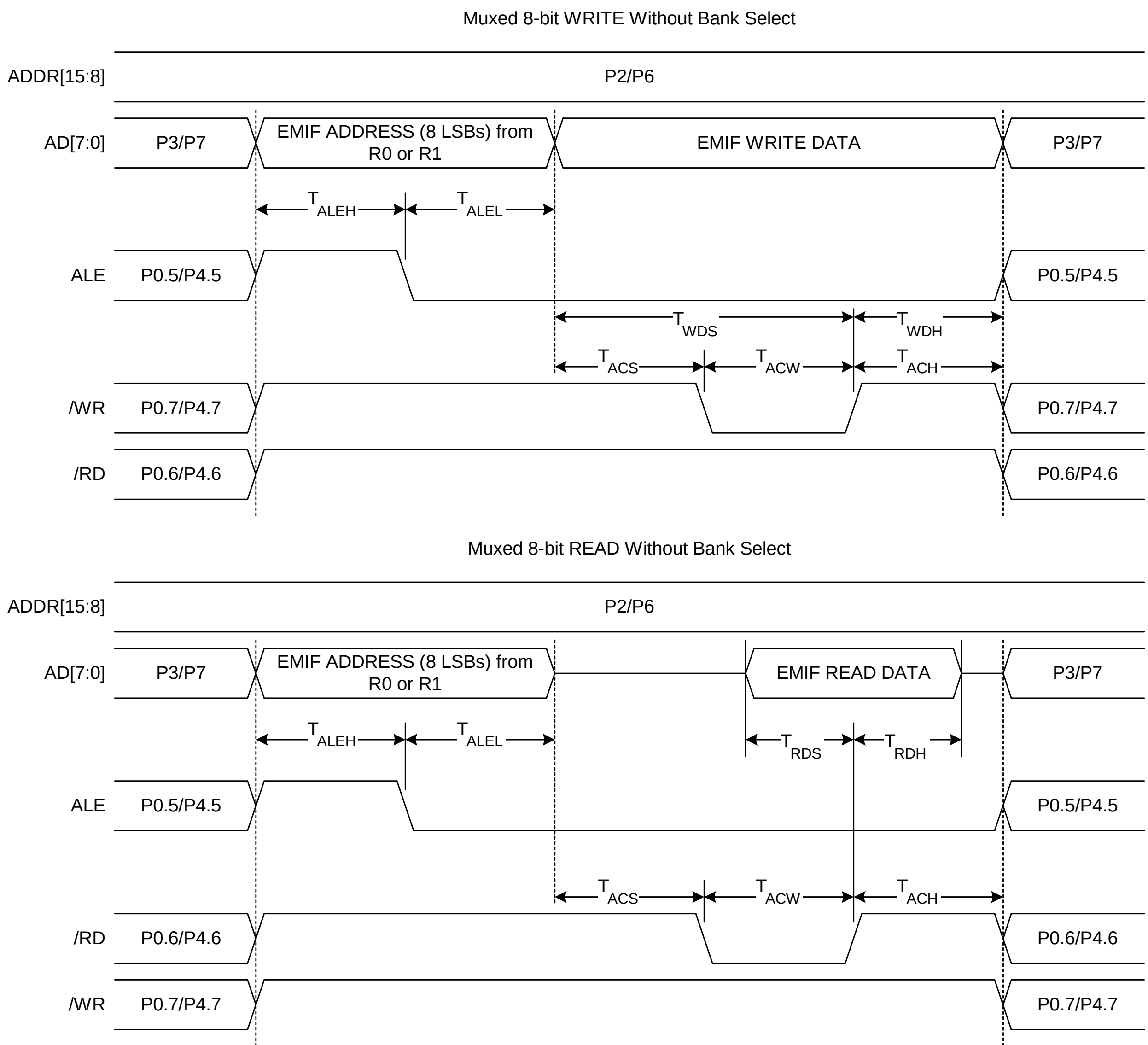


Figure 17.8. Multiplexed 8-bit MOVX without Bank Select Timing

Table 18.1. Port I/O DC Electrical Characteristics

V_{DD} = 2.7 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Output High Voltage (V_{OH})	I_{OH} = -3 mA, Port I/O Push-Pull I_{OH} = -10 µA, Port I/O Push-Pull I_{OH} = -10 mA, Port I/O Push-Pull	V_{DD} – 0.7 V_{DD} – 0.1	 V_{DD} – 0.8		V
Output Low Voltage (V_{OL})	I_{OL} = 8.5 mA I_{OL} = 10 µA I_{OL} = 25 mA		 1.0	0.6 0.1	V
Input High Voltage (VIH)		0.7 x V_{DD}			
Input Low Voltage (VIL)				0.3 x V_{DD}	
Input Leakage Current	DGND < Port Pin < V_{DD}, Pin Tri-state Weak Pullup Off Weak Pullup On		 10	 ± 1	µA
Input Capacitance			5		pF

The PnMDOUT registers control the output modes of the port pins regardless of whether the Crossbar has allocated the Port pin for a digital peripheral or not. The exceptions to this rule are: the Port pins connected to SDA, SCL, RX0 (if UART0 is in Mode 0), and RX1 (if UART1 is in Mode 0) are always configured as Open-Drain outputs, regardless of the settings of the associated bits in the PnMDOUT registers.

18.1.3. Configuring Port Pins as Digital Inputs

A Port pin is configured as a digital input by setting its output mode to “Open-Drain” and writing a logic 1 to the associated bit in the Port Data register. For example, P3.7 is configured as a digital input by setting P3MDOUT.7 to a logic 0 and P3.7 to a logic 1.

If the Port pin has been assigned to a digital peripheral by the Crossbar and that pin functions as an input (for example RX0, the UART0 receive pin), then the output drivers on that pin are automatically disabled.

18.1.4. Weak Pullups

By default, each Port pin has an internal weak pullup device enabled which provides a resistive connection (about 100 kΩ) between the pin and V_{DD}. The weak pullup devices can be globally disabled by writing a logic 1 to the Weak Pullup Disable bit, (WEAKPUD, XBR2.7). The weak pullup is automatically deactivated on any pin that is driving a logic 0; that is, an output pin will not contend with its own pullup device. The weak pullup device can also be explicitly disabled on any Port 1 pin by configuring the pin as an Analog Input, as described below.

18.1.5. Configuring Port 1 Pins as Analog Inputs

The pins on Port 1 can serve as analog inputs to the ADC2 analog MUX on the C8051F12x devices. A Port pin is configured as an Analog Input by writing a logic 0 to the associated bit in the PnMDIN registers. All Port pins default to a Digital Input mode. Configuring a Port pin as an analog input:

1. Disables the digital input path from the pin. This prevents additional power supply current from being drawn when the voltage at the pin is near V_{DD} / 2. A read of the Port Data bit will return a logic 0 regardless of the voltage at the Port pin.
2. Disables the weak pullup device on the pin.
3. Causes the Crossbar to “skip over” the pin when allocating Port pins for digital peripherals.

Note that the output drivers on a pin configured as an Analog Input are not explicitly disabled. Therefore, the associated P1MDOUT bits of pins configured as Analog Inputs should explicitly be set to logic 0 (Open-Drain output mode), and the associated Port1 Data bits should be set to logic 1 (high-impedance). Also note that it is not required to configure a Port pin as an Analog Input in order to use it as an input to ADC2, however, it is strongly recommended. See the ADC2 section in this datasheet for further information.

	P0								P1								P2								P3								Crossbar Register Bits
PIN I/O	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	
TX0	●																																
RX0		●																															
SCK	●		●																														
MISO		●		●																													
MOSI			●		●																												
NSS				●		●																											
SDA	●		●	●	●	●																											
SCL		●		●	●	●																											
TX1	●		●	●	●	●																											
RX1		●		●	●	●																											
CEX0	●		●	●	●	●																											
CEX1		●		●	●	●																											
CEX2			●		●	●																											
CEX3				●		●																											
CEX4					●																												
CEX5						●																											
ECI	●	●	●	●	●	●																											
CP0	●	●	●	●	●	●																											
CP1	●	●	●	●	●	●																											
T0	●	●	●	●	●	●																											
/INT0	●	●	●	●	●	●																											
T1	●	●	●	●	●	●																											
/INT1	●	●	●	●	●	●																											
T2	●	●	●	●	●	●																											
T2EX	●	●	●	●	●	●																											
T4	●	●	●	●	●	●																											
T4EX	●	●	●	●	●	●																											
/SYSCLK	●	●	●	●	●	●																											
CNVSTR0	●	●	●	●	●	●																											
CNVSTR2	●	●	●	●	●	●																											

Figure 18.5. Priority Crossbar Decode Table (EMIFLE = 1; EMIF in Non-Multiplexed Mode; P1MDIN = 0xFF)

SFR Definition 18.4. P0: Port0 Data

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0x80
SFR Page: All Pages

Bits7–0: P0.[7:0]: Port0 Output Latch Bits.
(Write - Output appears on I/O pins per XBR0, XBR1, and XBR2 Registers)
0: Logic Low Output.
1: Logic High Output (open if corresponding P0MDOUT.n bit = 0).
(Read - Regardless of XBR0, XBR1, and XBR2 Register settings).
0: P0.n pin is logic low.
1: P0.n pin is logic high.

Note: P0.7 (/WR), P0.6 (/RD), and P0.5 (ALE) can be driven by the External Data Memory Interface. See **Section "17. External Data Memory Interface and On-Chip XRAM" on page 219** for more information. See also SFR Definition 18.3 for information about configuring the Crossbar for External Memory accesses.

SFR Definition 18.5. P0MDOUT: Port0 Output Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xA4
SFR Page: F

Bits7–0: P0MDOUT.[7:0]: Port0 Output Mode Bits.
0: Port Pin output mode is configured as Open-Drain.
1: Port Pin output mode is configured as Push-Pull.

Note: SDA, SCL, and RX0 (when UART0 is in Mode 0) and RX1 (when UART1 is in Mode 0) are always configured as Open-Drain when they appear on Port pins.

23.2. Timer 2, Timer 3, and Timer 4

Timers 2, 3, and 4 are 16-bit counter/timers, each formed by two 8-bit SFR's: TMRnL (low byte) and TMRnH (high byte) where n = 2, 3, and 4 for timers 2, 3, and 4 respectively. Timers 2 and 4 feature auto-reload, capture, and toggle output modes with the ability to count up or down. Timer 3 features auto-reload and capture modes, with the ability to count up or down. Capture Mode and Auto-reload mode are selected using bits in the Timer 2, 3, and 4 Control registers (TMRnCN). Toggle output mode is selected using the Timer 2 or 4 Configuration registers (TMRnCF). These timers may also be used to generate a square-wave at an external pin. As with Timers 0 and 1, Timers 2, 3, and 4 can use either the system clock (divided by one, two, or twelve), external clock (divided by eight) or transitions on an external input pin as its clock source. Timer 2 and 3 can be used to start an ADC Data Conversion and Timers 2, 3, and 4 can schedule DAC outputs. Timers 1, 2, 3, or 4 may be used to generate baud rates for UART 0. Only Timer 1 can be used to generate baud rates for UART 1.

The Counter/Timer Select bit C/Tn bit (TMRnCN.1) configures the peripheral as a counter or timer. Clearing C/Tn configures the Timer to be in a timer mode (i.e., the system clock or transitions on an external pin as the input for the timer). When C/Tn is set to 1, the timer is configured as a counter (i.e., high-to-low transitions at the Tn input pin increment (or decrement) the counter/timer register. Timer 3 and Timer 2 share the T2 input pin. Refer to **Section "18.1. Ports 0 through 3 and the Priority Crossbar Decoder" on page 238** for information on selecting and configuring external I/O pins for digital peripherals, such as the Tn pin.

Timer 2, 3, and 4 can use either SYSCLK, SYSCLK divided by 2, SYSCLK divided by 12, an external clock divided by 8, or high-to-low transitions on the Tn input pin as its clock source when operating in Counter/Timer with Capture mode. Clearing the C/Tn bit (TMRnCN.1) selects the system clock/external clock as the input for the timer. The Timer Clock Select bits TnM0 and TnM1 in TMRnCF can be used to select the system clock undivided, system clock divided by two, system clock divided by 12, or an external clock provided at the XTAL1/XTAL2 pins divided by 8 (see SFR Definition 23.13). When C/Tn is set to logic 1, a high-to-low transition at the Tn input pin increments the counter/timer register (i.e., configured as a counter).

23.2.1. Configuring Timer 2, 3, and 4 to Count Down

Timers 2, 3, and 4 have the ability to count down. When the timer's Decrement Enable Bit (DCENn) in the Timer Configuration Register (See SFR Definition 23.13) is set to '1', the timer can then count *up* or *down*. When DCENn = 1, the direction of the timer's count is controlled by the TnEX pin's logic level (Timer 3 shares the T2EX pin with Timer 2). When TnEX = 1, the counter/timer will count up; when TnEX = 0, the counter/timer will count down. To use this feature, TnEX must be enabled in the digital crossbar and configured as a digital input.

Note: When DCENn = 1, other functions of the TnEX input (i.e., capture and auto-reload) are not available. TnEX will only control the direction of the timer when DCENn = 1.