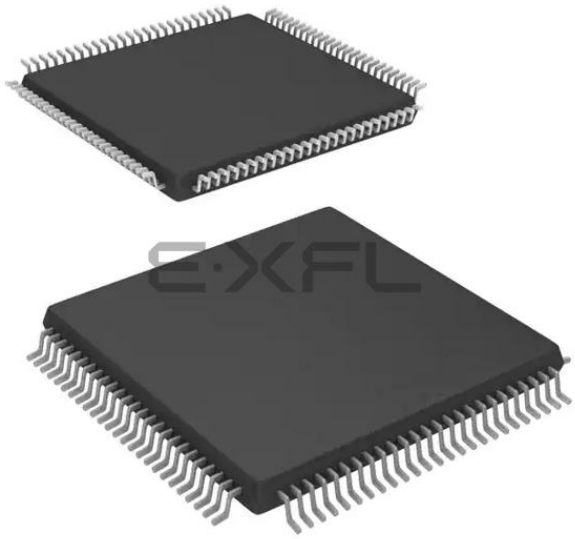


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	100MHz
Connectivity	EBI/EMI, SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	64
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8.25K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x8b, 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f120

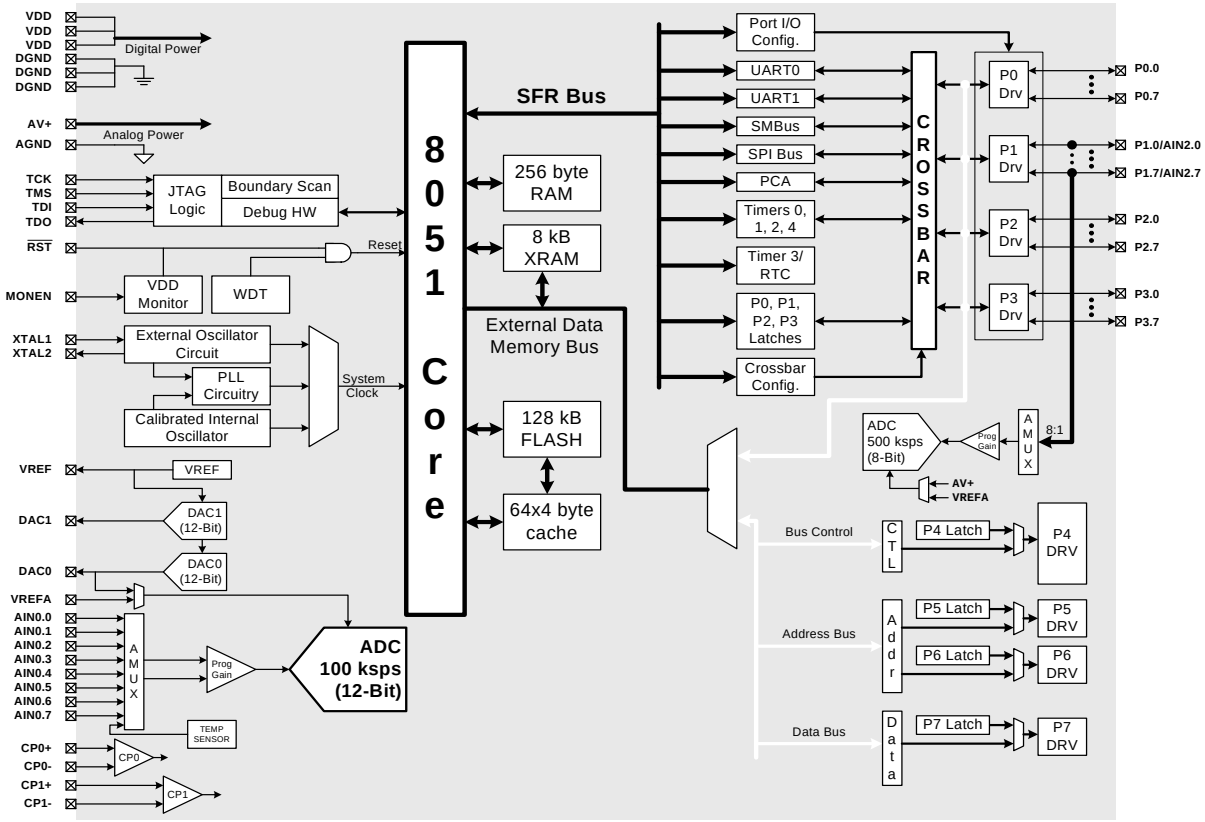


Figure 1.2. C8051F121/125 Block Diagram

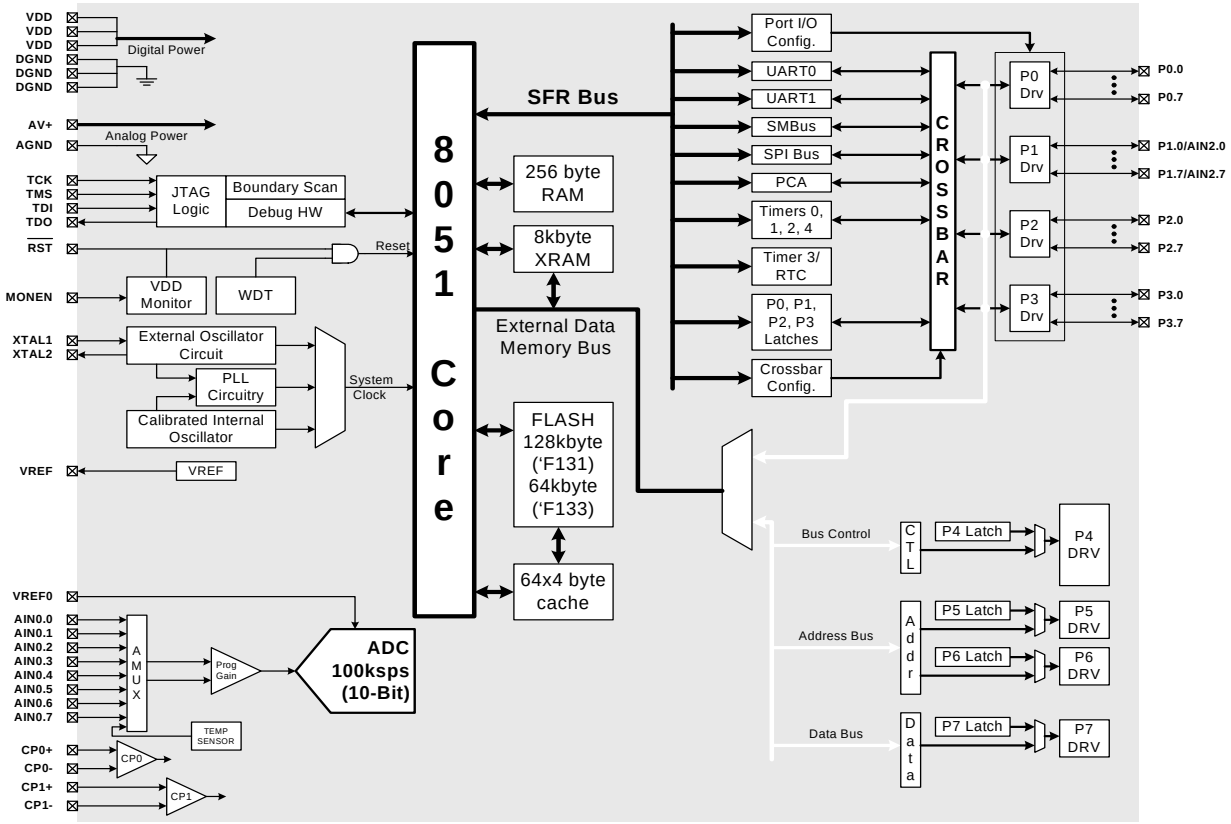


Figure 1.6. C8051F131/133 Block Diagram

1.3. JTAG Debug and Boundary Scan

JTAG boundary scan and debug circuitry is included which provides *non-intrusive, full speed, in-circuit debugging using the production part installed in the end application*, via the four-pin JTAG interface. The JTAG port is fully compliant to IEEE 1149.1, providing full boundary scan for test and manufacturing purposes.

Silicon Labs' debugging system supports inspection and modification of memory and registers, breakpoints, watchpoints, a stack monitor, and single stepping. No additional target RAM, program memory, timers, or communications channels are required. All the digital and analog peripherals are functional and work correctly while debugging. All the peripherals (except for the ADC and SMBus) are stalled when the MCU is halted, during single stepping, or at a breakpoint in order to keep them synchronized.

The C8051F120DK development kit provides all the hardware and software necessary to develop application code and perform in-circuit debugging with the C8051F12x or C8051F13x MCUs.

The kit includes a Windows (95 or later) development environment, a serial adapter for connecting to the JTAG port, and a target application board with a C8051F120 MCU installed. All of the necessary communication cables and a wall-mount power supply are also supplied with the development kit. Silicon Labs' debug environment is a vastly superior configuration for developing and debugging embedded applications compared to standard MCU emulators, which use on-board "ICE Chips" and target cables and require the MCU in the application board to be socketed. Silicon Labs' debug environment both increases ease of use and preserves the performance of the precision, on-chip analog peripherals.

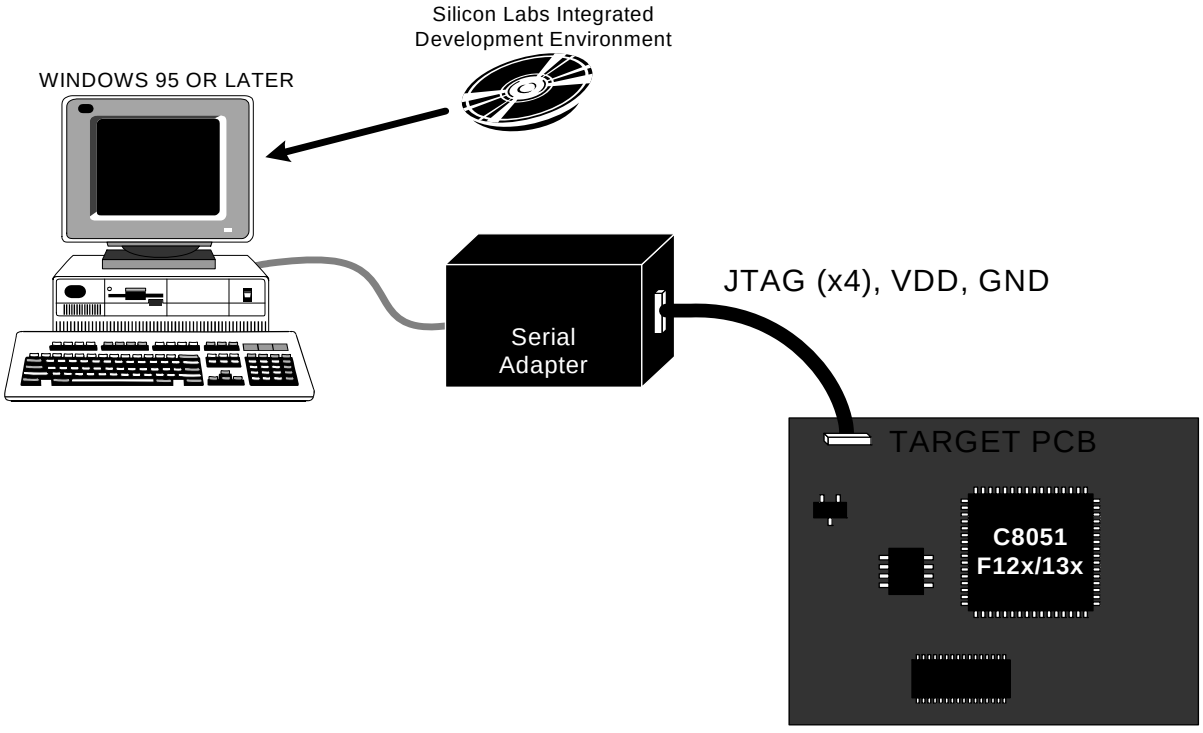


Figure 1.9. Development/In-System Debug Diagram

1.4. 16 x 16 MAC (Multiply and Accumulate) Engine

The C8051F120/1/2/3 and C8051F130/1/2/3 devices include a multiply and accumulate engine which can be used to speed up many mathematical operations. MAC0 contains a 16-by-16 bit multiplier and a 40-bit adder, which can perform integer or fractional multiply-accumulate and multiply operations on signed input values in two SYSCLK cycles. A rounding engine provides a rounded 16-bit fractional result after an additional (third) SYSCLK cycle. MAC0 also contains a 1-bit arithmetic shifter that will left or right-shift the contents of the 40-bit accumulator in a single SYSCLK cycle.

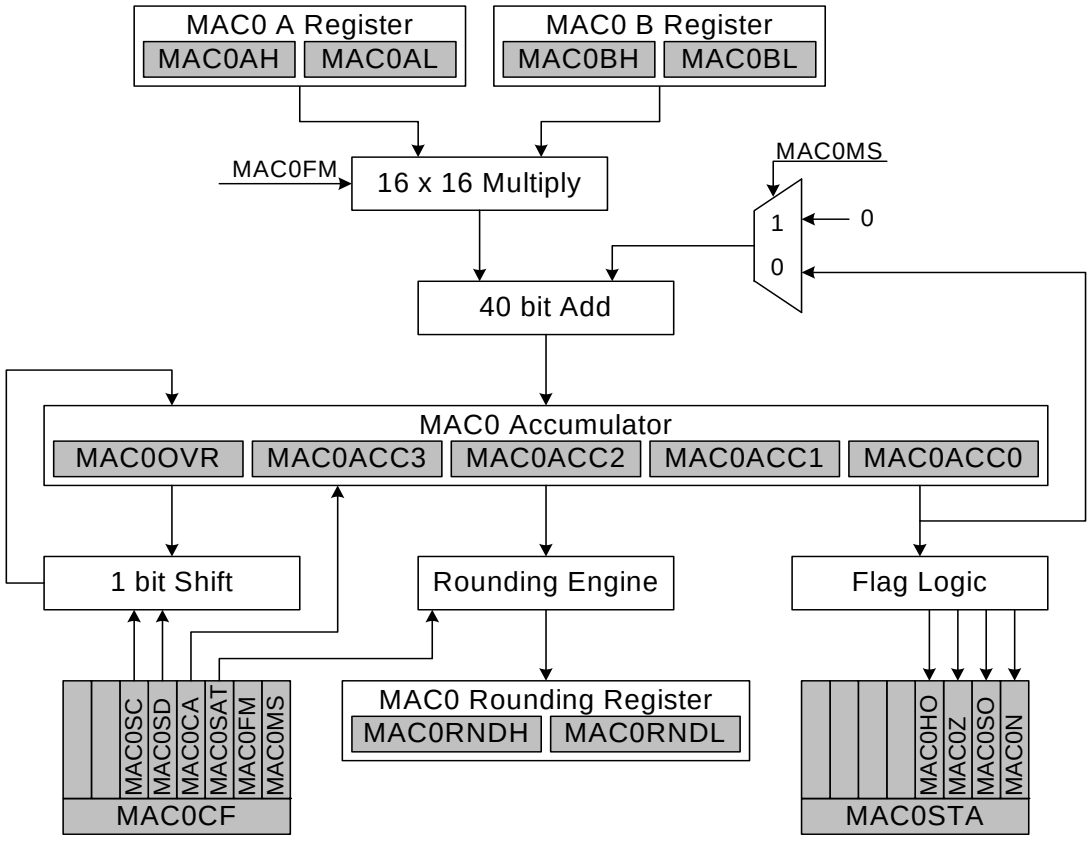


Figure 1.10. MAC0 Block Diagram

1.10. 12-bit Digital to Analog Converters

The C8051F12x devices have two integrated 12-bit Digital to Analog Converters (DACs). The MCU data and control interface to each DAC is via the Special Function Registers. The MCU can place either or both of the DACs in a low power shutdown mode.

The DACs are voltage output mode and include a flexible output scheduling mechanism. This scheduling mechanism allows DAC output updates to be forced by a software write or scheduled on a Timer 2, 3, or 4 overflow. The DAC voltage reference is supplied from the dedicated VREFD input pin on the 100-pin TQFP devices or via the internal Voltage reference on the 64-pin TQFP devices. The DACs are especially useful as references for the comparators or offsets for the differential inputs of the ADCs.

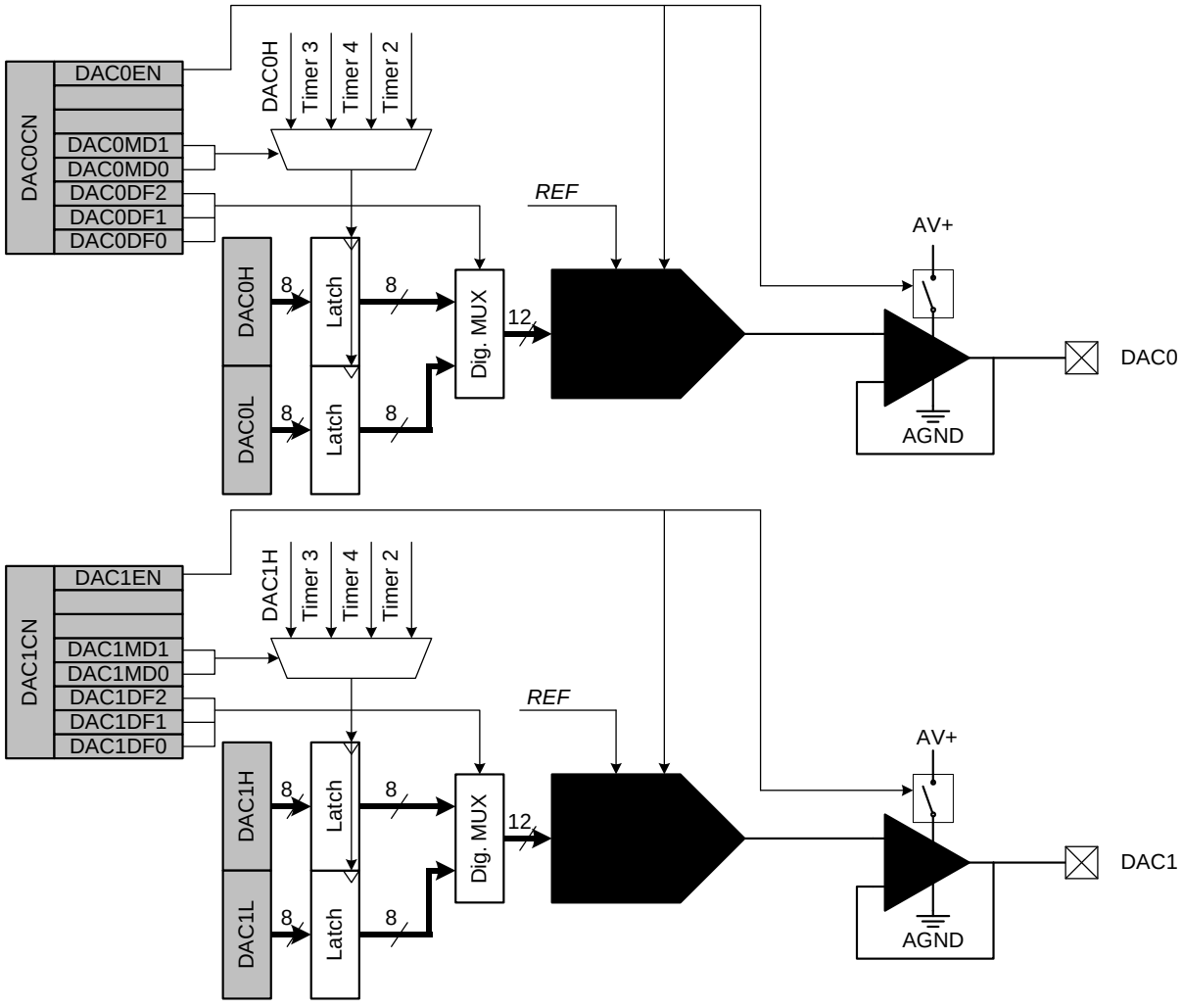


Figure 1.15. DAC System Block Diagram

Table 3.2. Global DC Electrical Characteristics (C8051F124/5/6/7)

–40 to +85 °C, 50 MHz System Clock unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Analog Supply Voltage[1]		2.7	3.0	3.6	V
Analog Supply Current	Internal REF, ADC, DAC, Comparators all active	—	1.7	—	mA
Analog Supply Current with analog sub-systems inactive	Internal REF, ADC, DAC, Comparators all disabled, oscillator disabled	—	0.2	—	µA
Analog-to-Digital Supply Delta ($\|V_{DD} – AV+\|$)		—	—	0.5	V
Digital Supply Voltage		2.7	3.0	3.6	V
Digital Supply Current with CPU active	V_{DD} = 3.0 V, Clock = 50 MHz V_{DD} = 3.0 V, Clock = 1 MHz V_{DD} = 3.0 V, Clock = 32 kHz	—	35 1 33	—	mA mA µA
Digital Supply Current with CPU inactive (not accessing Flash)	V_{DD} = 3.0 V, Clock = 50 MHz V_{DD} = 3.0 V, Clock = 1 MHz V_{DD} = 3.0 V, Clock = 32 kHz	—	27 0.4 15	—	mA mA µA
Digital Supply Current (shutdown)	Oscillator not running	—	0.4	—	µA
Digital Supply RAM Data Retention Voltage		—	1.5	—	V
SYSCLK (System Clock)[2,3]		0	—	50	MHz
Specified Operating Temperature Range		–40	—	+85	°C

Notes:

1. Analog Supply AV+ must be greater than 1 V for V_{DD} monitor to operate.
2. SYSCLK is the internal device clock. For operational speeds in excess of 30 MHz, SYSCLK must be derived from the phase-locked loop (PLL).
3. SYSCLK must be at least 32 kHz to enable debugging.

SFR Definition 8.4. DAC1H: DAC1 High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xD3
SFR Page: 1

Bits7–0: DAC1 Data Word Most Significant Byte.

SFR Definition 8.5. DAC1L: DAC1 Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xD2
SFR Page: 1

Bits7–0: DAC1 Data Word Least Significant Byte.

Table 9.1. Voltage Reference Electrical Characteristics

V_{DD} = 3.0 V, AV+ = 3.0 V, –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Analog Bias Generator Power Supply Current	BIASE = 1	—	100	—	µA
Internal Reference (REFBE = 1)					
Output Voltage	25 °C ambient	2.36	2.43	2.48	V
VREF Short-Circuit Current		—	—	30	mA
VREF Temperature Coefficient		—	15	—	ppm/°C
Load Regulation	Load = 0 to 200 µA to AGND	—	0.5	—	ppm/µA
VREF Turn-on Time 1	4.7 µF tantalum, 0.1 µF ceramic bypass	—	2	—	ms
VREF Turn-on Time 2	0.1 µF ceramic bypass	—	20	—	µs
VREF Turn-on Time 3	no bypass cap	—	10	—	µs
Reference Buffer Power Supply Current		—	40	—	µA
Power Supply Rejection		—	140	—	ppm/V
External Reference (REFBE = 0)					
Input Voltage Range		1.00	—	(AV+) – 0.3	V
Input Current		—	0	1	µA

and a RET pops two record bits, also.) The stack record circuitry can also detect an overflow or underflow on the 32-bit shift register, and can notify the debug software even with the MCU running at speed.

11.2.6. Special Function Registers

The direct-access data memory locations from 0x80 to 0xFF constitute the special function registers (SFR's). The SFR's provide control and data exchange with the CIP-51's resources and peripherals. The CIP-51 duplicates the SFR's found in a typical 8051 implementation as well as implementing additional SFR's used to configure and access the sub-systems unique to the MCU. This allows the addition of new functionality while retaining compatibility with the MCS-51™ instruction set. Table 11.2 lists the SFR's implemented in the CIP-51 System Controller.

The SFR registers are accessed whenever the direct addressing mode is used to access memory locations from 0x80 to 0xFF. SFR's with addresses ending in 0x0 or 0x8 (e.g. P0, TCON, P1, SCON, IE, etc.) are bit-addressable as well as byte-addressable. All other SFR's are byte-addressable only. Unoccupied addresses in the SFR space are reserved for future use. Accessing these areas will have an indeterminate effect and should be avoided. Refer to the corresponding pages of the datasheet, as indicated in Table 11.3, for a detailed description of each register.

11.2.6.1.SFR Paging

The CIP-51 features *SFR paging,* allowing the device to map many SFR's into the 0x80 to 0xFF memory address space. The SFR memory space has 256 *pages*. In this way, each memory location from 0x80 to 0xFF can access up to 256 SFR's. The C8051F12x family of devices utilizes five SFR pages: 0, 1, 2, 3, and F. SFR pages are selected using the Special Function Register Page Selection register, SFRPAGE (see SFR Definition 11.3). The procedure for reading and writing an SFR is as follows:

1. Select the appropriate SFR page number using the SFRPAGE register.
2. Use direct accessing mode to read or write the special function register (MOV instruction).

11.2.6.2.Interrupts and SFR Paging

When an interrupt occurs, the SFR Page Register will automatically switch to the SFR page containing the flag bit that caused the interrupt. The automatic SFR Page switch function conveniently removes the burden of switching SFR pages from the interrupt service routine. Upon execution of the RETI instruction, the SFR page is automatically restored to the SFR Page in use prior to the interrupt. This is accomplished via a three-byte *SFR Page Stack*. The top byte of the stack is SFRPAGE, the current SFR Page. The second byte of the SFR Page Stack is SFRNEXT. The third, or bottom byte of the SFR Page Stack is SFRLAST. On interrupt, the current SFRPAGE value is pushed to the SFRNEXT byte, and the value of SFRNEXT is pushed to SFRLAST. Hardware then loads SFRPAGE with the SFR Page containing the flag bit associated with the interrupt. On a return from interrupt, the SFR Page Stack is popped resulting in the value of SFRNEXT returning to the SFRPAGE register, thereby restoring the SFR page context without software intervention. The value in SFRLAST (0x00 if there is no SFR Page value in the bottom of the stack) of the stack is placed in SFRNEXT register. If desired, the values stored in SFRNEXT and SFRLAST may be modified during an interrupt, enabling the CPU to return to a different SFR Page upon execution of the RETI instruction (on interrupt exit). Modifying registers in the SFR Page Stack does not cause a push or pop of the stack. Only interrupt calls and returns will cause push/pop operations on the SFR Page Stack.

13.1. Power-on Reset

The C8051F120/1/2/3/4/5/6/7 family incorporates a power supply monitor that holds the MCU in the reset state until V_{DD} rises above the V_{RST} level during power-up. See Figure 13.2 for timing diagram, and refer to Table 13.1 for the Electrical Characteristics of the power supply monitor circuit. The $\overline{RST}$ pin is asserted low until the end of the 100 ms V_{DD} Monitor timeout in order to allow the V_{DD} supply to stabilize. The V_{DD} Monitor reset is enabled and disabled using the external V_{DD} monitor enable pin (MONEN). When the V_{DD} Monitor is enabled, it is selected as a reset source using the PORSF bit. If the RSTSRC register is written by firmware, PORSF (RSTSRC.1) must be written to '1' for the V_{DD} Monitor to be effective.

On exit from a power-on reset, the PORSF flag (RSTSRC.1) is set by hardware to logic 1. All of the other reset flags in the RSTSRC Register are indeterminate. PORSF is cleared by all other resets. Since all resets cause program execution to begin at the same location (0x0000) software can read the PORSF flag to determine if a power-up was the cause of reset. The contents of internal data memory should be assumed to be undefined after a power-on reset.

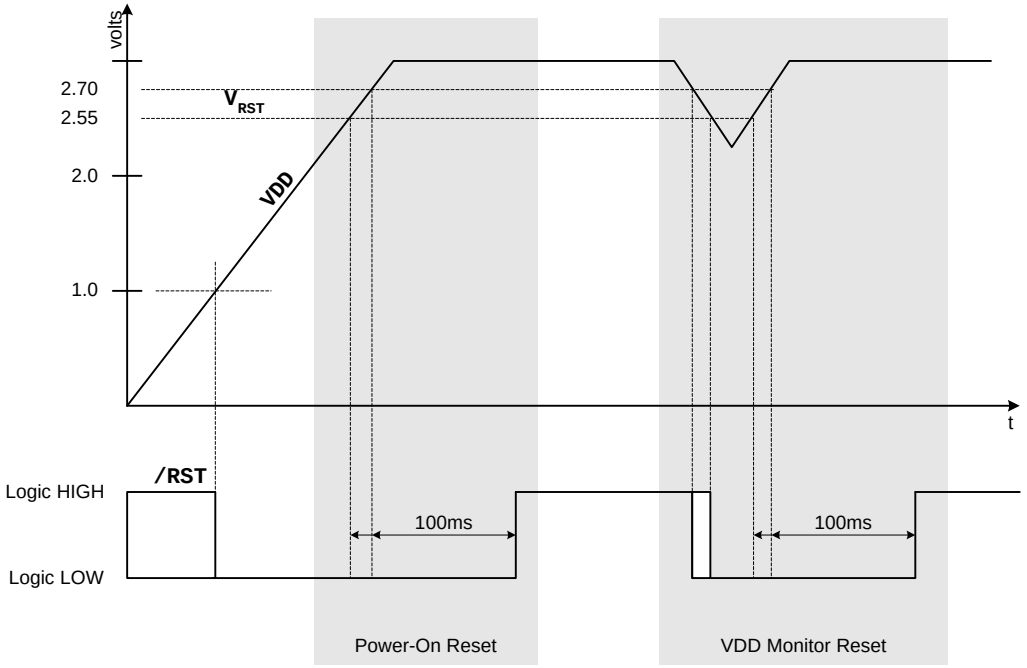


Figure 13.2. Reset Timing

13.2. Power-fail Reset

When a power-down transition or power irregularity causes V_{DD} to drop below V_{RST}, the power supply monitor will drive the $\overline{RST}$ pin low and return the CIP-51 to the reset state. When V_{DD} returns to a level above VRST, the CIP-51 will leave the reset state in the same manner as that for the power-on reset (see Figure 13.2). Note that even though internal data memory contents are not altered by the power-fail reset, it is impossible to determine if V_{DD} dropped below the level required for data retention. If the PORSF flag is set to logic 1, the data may no longer be valid.

The Flash Access Limit security feature (see SFR Definition 15.1) protects proprietary program code and data from being read by software running on the device. This feature provides support for OEMs that wish to program the MCU with proprietary value-added firmware before distribution. The value-added firmware can be protected while allowing additional code to be programmed in remaining program memory space later.

The Flash Access Limit (FAL) is a 17-bit address that establishes two logical partitions in the program memory space. The first is an upper partition consisting of all the program memory locations at or above the FAL address, and the second is a lower partition consisting of all the program memory locations starting at 0x00000 up to (but excluding) the FAL address. Software in the upper partition can execute code in the lower partition, but is prohibited from reading locations in the lower partition using the MOVC instruction. (Executing a MOVC instruction from the upper partition with a source address in the lower partition will return indeterminate data.) Software running in the lower partition can access locations in both the upper and lower partition without restriction.

The Value-added firmware should be placed in the lower partition. On reset, control is passed to the value-added firmware via the reset vector. Once the value-added firmware completes its initial execution, it branches to a predetermined location in the upper partition. If entry points are published, software running in the upper partition may execute program code in the lower partition, but it cannot read or change the contents of the lower partition. Parameters may be passed to the program code running in the lower partition either through the typical method of placing them on the stack or in registers before the call or by placing them in prescribed memory locations in the upper partition.

The FAL address is specified using the contents of the Flash Access Limit Register. The 8 MSBs of the 17-bit FAL address are determined by the setting of the FLACL register. Thus, the FAL can be located on 512-byte boundaries anywhere in program memory space. However, the 1024-byte erase sector size essentially requires that a 1024 boundary be used. The contents of a non-initialized FLACL security byte are 0x00, thereby setting the FAL address to 0x00000 and allowing read access to all locations in program memory space by default.

SFR Definition 15.1. FLACL: Flash Access Limit

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:

SFR Address: 0xB7
SFR Page: F

Bits 7–0: FLACL: Flash Access Limit.
This register holds the most significant 8 bits of the 17-bit program memory read/write/erase limit address. The lower 9 bits of the read/write/erase limit are always set to 0. A write to this register sets the Flash Access Limit. This register can only be written once after any reset. Any subsequent writes are ignored until the next reset. **To fully protect all addresses below this limit, bit 0 of FLACL should be set to '0' to align the FAL on a 1024-byte Flash page boundary.**

SFR Definition 17.2. EMI0CF: External Memory Configuration

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	PRTSEL	EMD2	EMD1	EMD0	EALE1	EALE0	00000011
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xA3
SFR Page: 0

Bits7–6: Unused. Read = 00b. Write = don't care.

Bit5: PRTSEL: EMIF Port Select.
0: EMIF active on P0–P3.
1: EMIF active on P4–P7.

Bit4: EMD2: EMIF Multiplex Mode Select.
0: EMIF operates in multiplexed address/data mode.
1: EMIF operates in non-multiplexed mode (separate address and data pins).

Bits3–2: EMD1-0: EMIF Operating Mode Select.
These bits control the operating mode of the External Memory Interface.
00: Internal Only: MOVX accesses on-chip XRAM only. All effective addresses alias to on-chip memory space.
01: Split Mode without Bank Select: Accesses below the 8 k boundary are directed on-chip. Accesses above the 8 k boundary are directed off-chip. 8-bit off-chip MOVX operations use the current contents of the Address High port latches to resolve upper address byte. Note that in order to access off-chip space, EMI0CN must be set to a page that is not contained in the on-chip address space.
10: Split Mode with Bank Select: Accesses below the 8 k boundary are directed on-chip. Accesses above the 8k boundary are directed off-chip. 8-bit off-chip MOVX operations use the contents of EMI0CN to determine the high-byte of the address.
11: External Only: MOVX accesses off-chip XRAM only. On-chip XRAM is not visible to the CPU.

Bits1–0: EALE1–0: ALE Pulse-Width Select Bits (only has effect when EMD2 = 0).
00: ALE high and ALE low pulse width = 1 SYSCLK cycle.
01: ALE high and ALE low pulse width = 2 SYSCLK cycles.
10: ALE high and ALE low pulse width = 3 SYSCLK cycles.
11: ALE high and ALE low pulse width = 4 SYSCLK cycles.

Table 18.1. Port I/O DC Electrical Characteristics

V_{DD} = 2.7 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Output High Voltage (V_{OH})	I_{OH} = -3 mA, Port I/O Push-Pull I_{OH} = -10 µA, Port I/O Push-Pull I_{OH} = -10 mA, Port I/O Push-Pull	V_{DD} – 0.7 V_{DD} – 0.1	 V_{DD} – 0.8		V
Output Low Voltage (V_{OL})	I_{OL} = 8.5 mA I_{OL} = 10 µA I_{OL} = 25 mA		 1.0	0.6 0.1	V
Input High Voltage (VIH)		0.7 x V_{DD}			
Input Low Voltage (VIL)				0.3 x V_{DD}	
Input Leakage Current	DGND < Port Pin < V_{DD}, Pin Tri-state Weak Pullup Off Weak Pullup On		 10	± 1	µA
Input Capacitance			5		pF

18.1.7. Crossbar Pin Assignment Example

In this example (Figure 18.6), we configure the Crossbar to allocate Port pins for UART0, the SMBus, UART1, /INT0, and /INT1 (8 pins total). Additionally, we configure the External Memory Interface to operate in Multiplexed mode and to appear on the Low ports. Further, we configure P1.2, P1.3, and P1.4 for Analog Input mode so that the voltages at these pins can be measured by ADC2. The configuration steps are as follows:

1. XBR0, XBR1, and XBR2 are set such that UART0EN = 1, SMB0EN = 1, INT0E = 1, INT1E = 1, and EMIFLE = 1. Thus: XBR0 = 0x05, XBR1 = 0x14, and XBR2 = 0x02.
2. We configure the External Memory Interface to use Multiplexed mode and to appear on the Low ports. PRTSEL = 0, EMD2 = 0.
3. We configure the desired Port 1 pins to Analog Input mode by setting P1MDIN to 0xE3 (P1.4, P1.3, and P1.2 are Analog Inputs, so their associated P1MDIN bits are set to logic 0).
4. We enable the Crossbar by setting XBARE = 1: XBR2 = 0x42.
   - UART0 has the highest priority, so P0.0 is assigned to TX0, and P0.1 is assigned to RX0.
   - The SMBus is next in priority order, so P0.2 is assigned to SDA, and P0.3 is assigned to SCL.
   - UART1 is next in priority order, so P0.4 is assigned to TX1. Because the External Memory Interface is selected on the lower Ports, EMIFLE = 1, which causes the Crossbar to skip P0.6 (/RD) and P0.7 (/WR). Because the External Memory Interface is configured in Multiplexed mode, the Crossbar will also skip P0.5 (ALE). RX1 is assigned to the next non-skipped pin, which in this case is P1.0.
   - /INT0 is next in priority order, so it is assigned to P1.1.
   - P1MDIN is set to 0xE3, which configures P1.2, P1.3, and P1.4 as Analog Inputs, causing the Crossbar to skip these pins.
   - /INT1 is next in priority order, so it is assigned to the next non-skipped pin, which is P1.5.
   - The External Memory Interface will drive Ports 2 and 3 (denoted by red dots in Figure 18.6) during the execution of an off-chip MOVX instruction.
5. We set the UART0 TX pin (TX0, P0.0) and UART1 TX pin (TX1, P0.4) outputs to Push-Pull by setting P0MDOUT = 0x11.
6. We configure all EMIF-controlled pins to push-pull output mode by setting P0MDOUT |= 0xE0; P2MDOUT = 0xFF; P3MDOUT = 0xFF.
7. We explicitly disable the output drivers on the 3 Analog Input pins by setting P1MDOUT = 0x00 (configure outputs to Open-Drain) and P1 = 0xFF (a logic 1 selects the high-impedance state).

SFR Definition 18.6. P1: Port1 Data

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0x90
SFR Page: All Pages

Bits7–0: P1.[7:0]: Port1 Output Latch Bits.
(Write - Output appears on I/O pins per XBR0, XBR1, and XBR2 Registers)
0: Logic Low Output.
1: Logic High Output (open if corresponding P1MDOUT.n bit = 0).
(Read - Regardless of XBR0, XBR1, and XBR2 Register settings).
0: P1.n pin is logic low.
1: P1.n pin is logic high.

Notes:

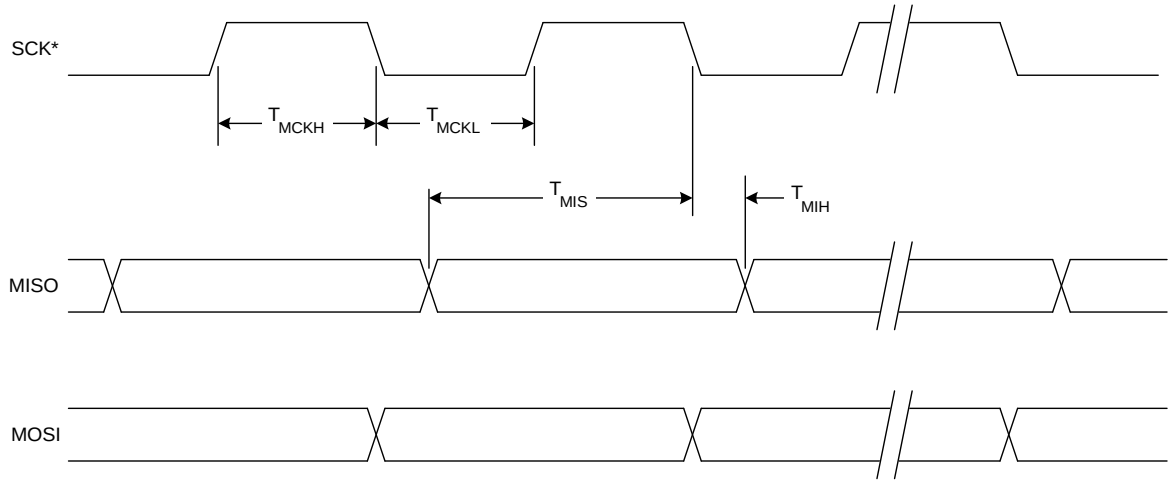
1. On C8051F12x devices, P1.[7:0] can be configured as inputs to ADC2 as AIN2.[7:0], in which case they are 'skipped' by the Crossbar assignment process and their digital input paths are disabled, depending on P1MDIN (See SFR Definition 18.7**)**. Note that in analog mode, the output mode of the pin is determined by the Port 1 latch and P1MDOUT (SFR Definition 18.8). See **Section "7. ADC2 (8-Bit ADC, C8051F12x Only)" on page 91** for more information about ADC2.
2. P1.[7:0] can be driven by the External Data Memory Interface (as Address[15:8] in Non-multiplexed mode). See **Section "17. External Data Memory Interface and On-Chip XRAM" on page 219** for more information about the External Memory Interface.

SFR Definition 18.7. P1MDIN: Port1 Input Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

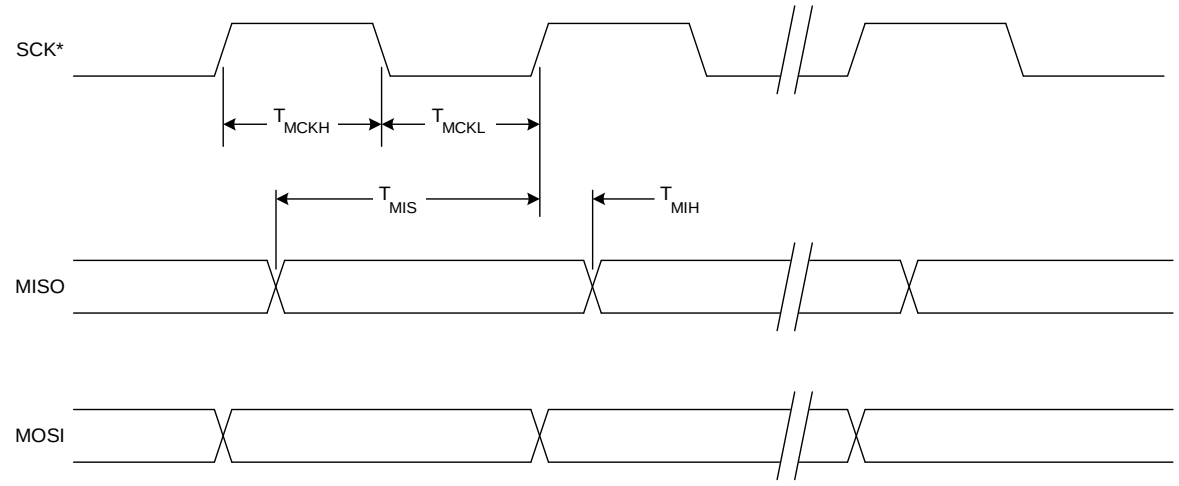
SFR Address: 0xAD
SFR Page: F

Bits7–0: P1MDIN.[7:0]: Port 1 Input Mode Bits.
0: Port Pin is configured in Analog Input mode. The digital input path is disabled (a read from the Port bit will always return '0'). The weak pullup on the pin is disabled.
1: Port Pin is configured in Digital Input mode. A read from the Port bit will return the logic level at the Pin. When configured as a digital input, the state of the weak pullup for the port pin is determined by the WEAKPUD bit (XBR2.7, see SFR Definition 18.3).



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 20.8. SPI Master Timing (CKPHA = 0)



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 20.9. SPI Master Timing (CKPHA = 1)

21.2. Multiprocessor Communications

Modes 2 and 3 support multiprocessor communication between a master processor and one or more slave processors by special use of the ninth data bit and the built-in UART0 address recognition hardware. When a master processor wants to transmit to one or more slaves, it first sends an address byte to select the target(s). An address byte differs from a data byte in that its ninth bit is logic 1; in a data byte, the ninth bit is always set to logic 0. UART0 will recognize as “valid” (i.e., capable of causing an interrupt) **two** types of addresses: (1) a *masked* address and (2) a *broadcast* address **at any given time**. Both are described below.

21.2.1. Configuration of a Masked Address

The UART0 address is configured via two SFR’s: SADDR0 (Serial Address) and SADEN0 (Serial Address Enable). SADEN0 sets the bit mask for the address held in SADDR0: bits set to logic 1 in SADEN0 correspond to bits in SADDR0 that are checked against the received address byte; bits set to logic 0 in SADEN0 correspond to “don’t care” bits in SADDR0.

Example 1, SLAVE #1	
SADDR0	= 00110101
SADEN0	= 00001111
UART0 Address	= xxxx0101

Example 2, SLAVE #2	
SADDR0	= 00110101
SADEN0	= 11110011
UART0 Address	= 0011xx01

Example 3, SLAVE #3	
SADDR0	= 00110101
SADEN0	= 11000000
UART0 Address	= 00xxxxxx

Setting the SM20 bit (SCON0.5) configures UART0 such that when a stop bit is received, UART0 will generate an interrupt only if the ninth bit is logic 1 (RB80 = ‘1’) and the received data byte matches the UART0 slave address. Following the received address interrupt, the slave will clear its SM20 bit to enable interrupts on the reception of the following data byte(s). Once the entire message is received, the addressed slave resets its SM20 bit to ignore all transmissions until it receives the next address byte. While SM20 is logic 1, UART0 ignores all bytes that do not match the UART0 address and include a ninth bit that is logic 1.

21.2.2. Broadcast Addressing

Multiple addresses can be assigned to a single slave and/or a single address can be assigned to multiple slaves, thereby enabling "broadcast" transmissions to more than one slave simultaneously. The broadcast address is the logical OR of registers SADDR0 and SADEN0, and ‘0’s of the result are treated as “don’t cares”. Typically a broadcast address of 0xFF (hexadecimal) is acknowledged by all slaves, assuming “don’t care” bits as ‘1’s. The master processor can be configured to receive all transmissions or a protocol can be implemented such that the master/slave role is temporarily reversed to enable half-duplex transmission between the original master and slave(s)..

Example 4, SLAVE #1	
SADDR0	= 00110101
SADEN0	= 00001111
Broadcast Address	= 00111111

Example 5, SLAVE #2	
SADDR0	= 00110101
SADEN0	= 11110011
Broadcast Address	= 11110111

Example 6, SLAVE #3	
SADDR0	= 00110101
SADEN0	= 11000000
Broadcast Address	= 11110101

Where all ZEROES in the Broadcast address are don’t cares.

Note in the above examples 4, 5, and 6, each slave would recognize as “valid” an address of 0xFF as a broadcast address. Also note that examples 4, 5, and 6 uses the same SADDR0 and SADEN0 register values as shown in the examples 1, 2, and 3 respectively (slaves #1, 2, and 3). Thus, a master could address each slave device individually using a masked address, and also broadcast to all three slave devices. For example, if a Master were to send an address “11110101”, only slave #1 would recognize the address as valid. If a master were to then send an address of “11111111”, all three slave devices would recognize the address as a valid broadcast address.

22. UART1

UART1 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates (details in **Section "22.1. Enhanced Baud Rate Generation" on page 300**). Received data buffering allows UART1 to start reception of a second incoming data byte before software has finished reading the previous data byte.

UART1 has two associated SFRs: Serial Control Register 1 (SCON1) and Serial Data Buffer 1 (SBUF1). The single SBUF1 location provides access to both transmit and receive registers. Reading SBUF1 accesses the buffered Receive register; writing SBUF1 accesses the Transmit register.

With UART1 interrupts enabled, an interrupt is generated each time a transmit is completed (TI1 is set in SCON1), or a data byte has been received (RI1 is set in SCON1). The UART1 interrupt flags are not cleared by hardware when the CPU vectors to the interrupt service routine. They must be cleared manually by software, allowing software to determine the cause of the UART1 interrupt (transmit complete or receive complete).

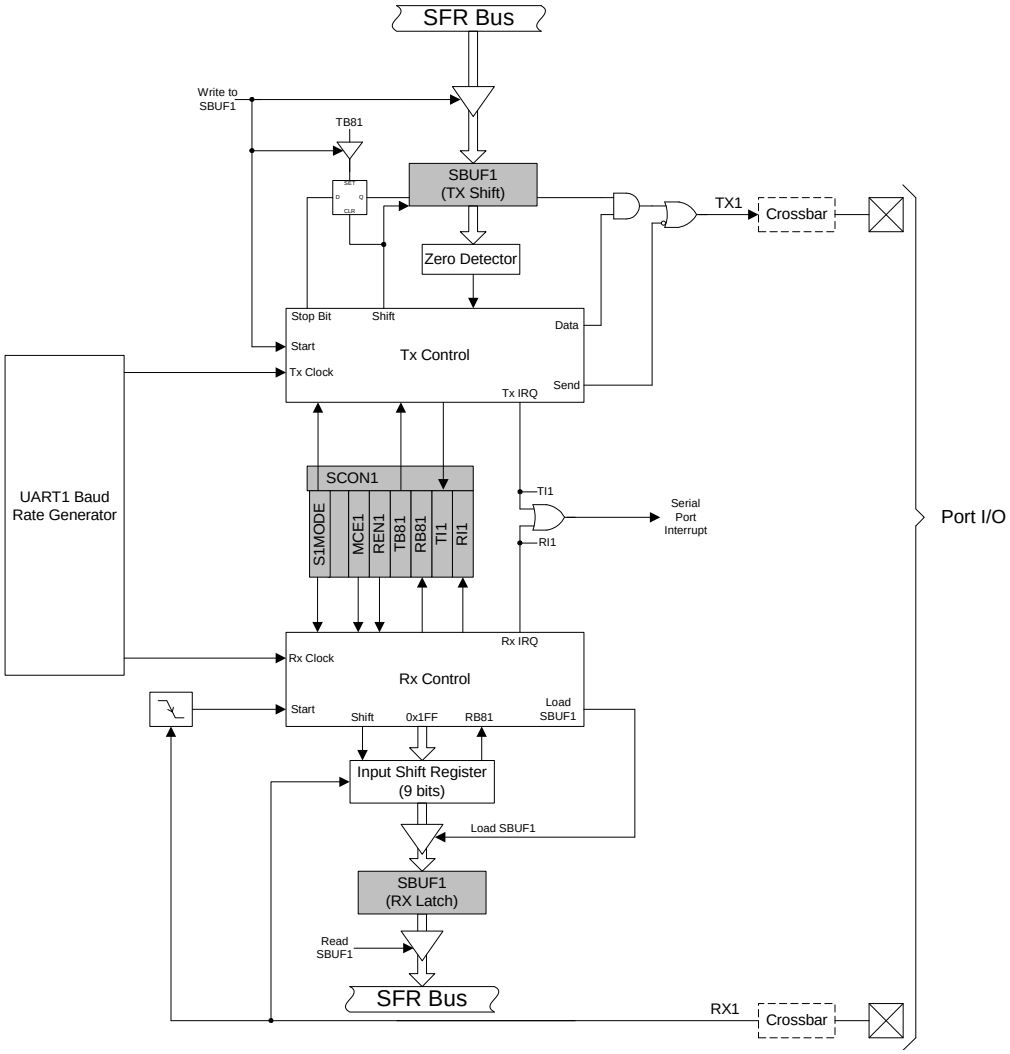


Figure 22.1. UART1 Block Diagram

23.2.3. Auto-Reload Mode

In Auto-Reload Mode, the counter/timer can be configured to count up or down and cause an interrupt/flag to occur upon an overflow/underflow event. When counting up, the counter/timer will set its overflow/underflow flag (TFn) and cause an interrupt (if enabled) upon overflow/underflow, and the values in the Reload/Capture Registers (RCAPnH and RCAPnL) are loaded into the timer and the timer is restarted. When the Timer External Enable Bit (EXENn) bit is set to '1' and the Decrement Enable Bit (DCENn) is '0', a falling edge ('1'-to-'0' transition) on the TnEX pin will cause a timer reload. Note that timer overflows will also cause auto-reloads. When DCENn is set to '1', the state of the TnEX pin controls whether the counter/timer counts *up* (increments) or *down* (decrements), and will not cause an auto-reload or interrupt event (Timer 3 shares the T2EX pin with Timer 2). See **Section 23.2.1** for information concerning configuration of a timer to count down.

When counting down, the counter/timer will set its overflow/underflow flag (TFn) and cause an interrupt (if enabled) when the value in the TMRnH and TMRnL registers matches the 16-bit value in the Reload/Capture Registers (RCAPnH and RCAPnL). This is considered an underflow event, and will cause the timer to load the value 0xFFFF. The timer is automatically restarted when an underflow occurs.

Counter/Timer with Auto-Reload mode is selected by clearing the CP/RLn bit. Setting TRn to logic 1 enables and starts the timer.

In Auto-Reload Mode, the External Flag (EXFn) toggles upon every overflow or underflow and does not cause an interrupt. The EXFn flag can be used as the most significant bit (MSB) of a 17-bit counter.

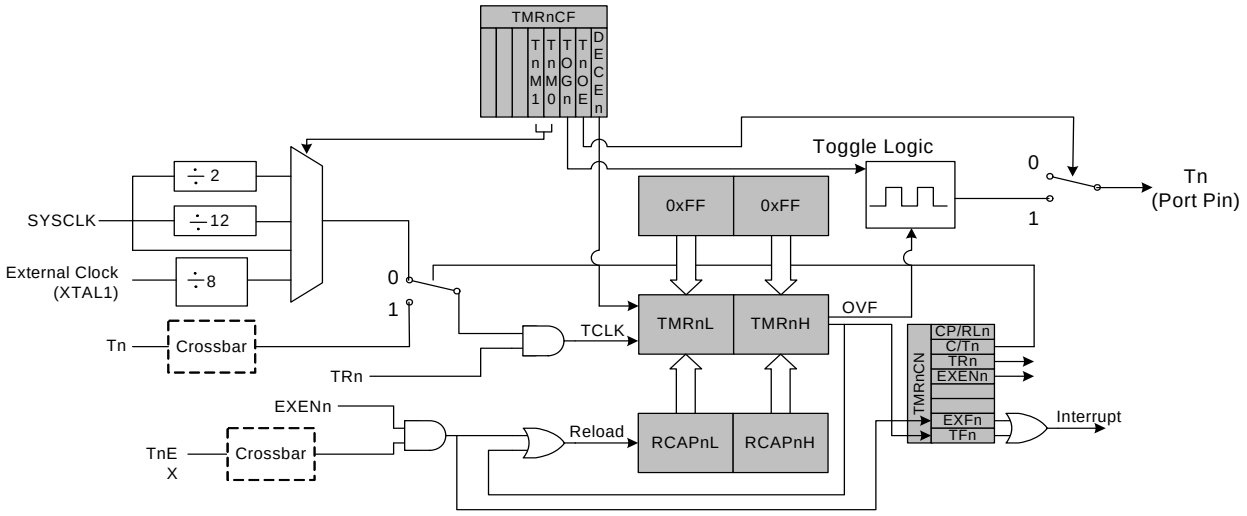


Figure 23.5. Tn Auto-reload (T2,3,4) and Toggle Mode (T2,4) Block Diagram

Important Note About the PCA0CN Register: If the main PCA counter (PCA0H : PCA0L) overflows during the execution phase of a read-modify-write instruction (bit-wise SETB or CLR, ANL, ORL, XRL) that targets the PCA0CN register, the CF (Counter Overflow) bit will not be set. If the CF flag is used by software to keep track of counter overflows, the following steps should be taken when performing a bit-wise operation on the PCA0CN register:

Step 1. Disable global interrupts.
Step 2. Read PCA0L. This will latch the value of PCA0H.
Step 3. Read PCA0H, saving the value.
Step 4. Execute the bit-wise operation on CCFn (for example, CLR CCF0, or CCF0 = 0;).
Step 5. Read PCA0L.
Step 6. Read PCA0H, saving the value.
Step 7. If the value of PCA0H read in Step 3 is 0xFF and the value for PCA0H read in Step 6 is 0x00, then manually set the CF bit in software (for example, SETB CF, or CF = 1;).
Step 8. Re-enable interrupts.