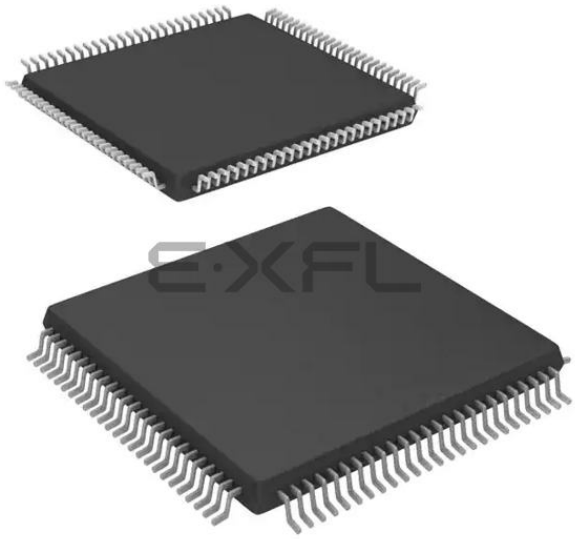

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	100MHz
Connectivity	EBI/EMI, SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	64
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8.25K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x8b, 8x10b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f122-gqr

Table 1.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	Flash Memory	RAM	2-cycle 16 by 16 MAC	External Memory Interface	SMBus/I2C	SPI	UARTS	Timers (16-bit)	Programmable Counter Array	Digital Port I/O's	12-bit 100ksps ADC Inputs	10-bit 100ksps ADC Inputs	8-bit 500ksps ADC Inputs	Voltage Reference	Temperature Sensor	DAC Resolution (bits)	DAC Outputs	Analog Comparators	Lead-Free (RoHS Compliant)	Package
C8051F120	100	128 k	8448	✓	✓	✓	✓	2	5	✓	64	8	-	8	✓	✓	12	2	2	-	100TQFP
C8051F120-GQ	100	128 k	8448	✓	✓	✓	✓	2	5	✓	64	8	-	8	✓	✓	12	2	2	✓	100TQFP
C8051F121	100	128 k	8448	✓	✓	✓	✓	2	5	✓	32	8	-	8	✓	✓	12	2	2	-	64TQFP
C8051F121-GQ	100	128 k	8448	✓	✓	✓	✓	2	5	✓	32	8	-	8	✓	✓	12	2	2	✓	64TQFP
C8051F122	100	128 k	8448	✓	✓	✓	✓	2	5	✓	64	-	8	8	✓	✓	12	2	2	-	100TQFP
C8051F122-GQ	100	128 k	8448	✓	✓	✓	✓	2	5	✓	64	-	8	8	✓	✓	12	2	2	✓	100TQFP
C8051F123	100	128 k	8448	✓	✓	✓	✓	2	5	✓	32	-	8	8	✓	✓	12	2	2	-	64TQFP
C8051F123-GQ	100	128 k	8448	✓	✓	✓	✓	2	5	✓	32	-	8	8	✓	✓	12	2	2	✓	64TQFP
C8051F124	50	128 k	8448	-	✓	✓	✓	2	5	✓	64	8	-	8	✓	✓	12	2	2	-	100TQFP
C8051F124-GQ	50	128 k	8448	-	✓	✓	✓	2	5	✓	64	8	-	8	✓	✓	12	2	2	✓	100TQFP
C8051F125	50	128 k	8448	-	✓	✓	✓	2	5	✓	32	8	-	8	✓	✓	12	2	2	-	64TQFP
C8051F125-GQ	50	128 k	8448	-	✓	✓	✓	2	5	✓	32	8	-	8	✓	✓	12	2	2	✓	64TQFP
C8051F126	50	128 k	8448	-	✓	✓	✓	2	5	✓	64	-	8	8	✓	✓	12	2	2	-	100TQFP
C8051F126-GQ	50	128 k	8448	-	✓	✓	✓	2	5	✓	64	-	8	8	✓	✓	12	2	2	✓	100TQFP
C8051F127	50	128 k	8448	-	✓	✓	✓	2	5	✓	32	-	8	8	✓	✓	12	2	2	-	64TQFP
C8051F127-GQ	50	128 k	8448	-	✓	✓	✓	2	5	✓	32	-	8	8	✓	✓	12	2	2	✓	64TQFP
C8051F130	100	128 k	8448	✓	✓	✓	✓	2	5	✓	64	-	8	-	✓	✓	-	-	2	-	100TQFP
C8051F130-GQ	100	128 k	8448	✓	✓	✓	✓	2	5	✓	64	-	8	-	✓	✓	-	-	2	✓	100TQFP
C8051F131	100	128 k	8448	✓	✓	✓	✓	2	5	✓	32	-	8	-	✓	✓	-	-	2	-	64TQFP
C8051F131-GQ	100	128 k	8448	✓	✓	✓	✓	2	5	✓	32	-	8	-	✓	✓	-	-	2	✓	64TQFP
C8051F132	100	64 k	8448	✓	✓	✓	✓	2	5	✓	64	-	8	-	✓	✓	-	-	2	-	100TQFP
C8051F132-GQ	100	64 k	8448	✓	✓	✓	✓	2	5	✓	64	-	8	-	✓	✓	-	-	2	✓	100TQFP
C8051F133	100	64 k	8448	✓	✓	✓	✓	2	5	✓	32	-	8	-	✓	✓	-	-	2	-	64TQFP
C8051F133-GQ	100	64 k	8448	✓	✓	✓	✓	2	5	✓	32	-	8	-	✓	✓	-	-	2	✓	64TQFP

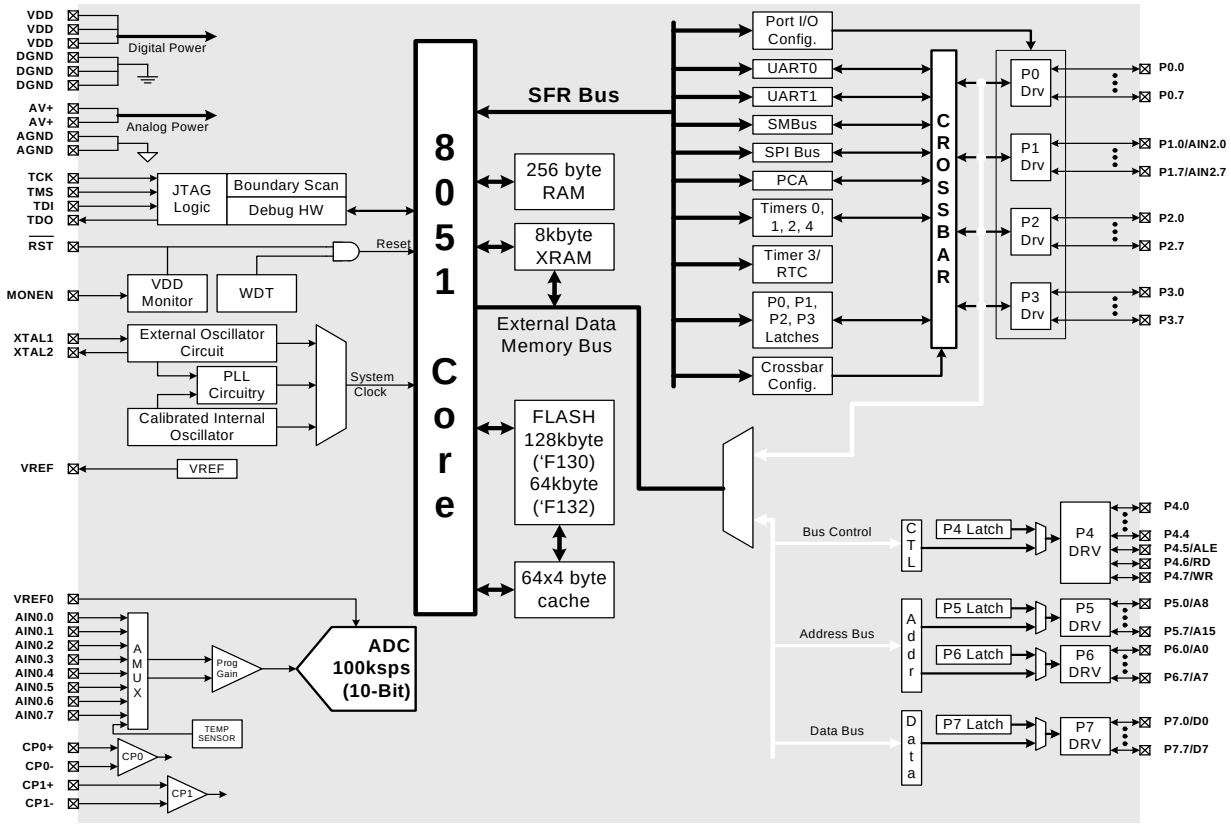

Figure 1.5. C8051F130/132 Block Diagram

1.9. 8-Bit Analog to Digital Converter

The C8051F12x devices have an on-board 8-bit SAR ADC (ADC2) with an 8-channel input multiplexer and programmable gain amplifier. This ADC features a 500 ksps maximum throughput and true 8-bit linearity with an INL of ±1LSB. Eight input pins are available for measurement. The ADC is under full control of the CIP-51 microcontroller via the Special Function Registers. The ADC2 voltage reference is selected between the analog power supply (AV+) and an external VREF pin. On the 100-pin TQFP devices, ADC2 has its own dedicated Voltage Reference input pin; on the 64-pin TQFP devices, ADC2 shares a Voltage Reference input pin with ADC0. User software may put ADC2 into shutdown mode to save power.

A programmable gain amplifier follows the analog multiplexer. The gain stage can be especially useful when different ADC input channels have widely varied input voltage signals, or when it is necessary to "zoom in" on a signal with a large DC offset (in differential mode, a DAC could be used to provide the DC offset). The PGA gain can be set in software to 0.5, 1, 2, or 4.

A flexible conversion scheduling system allows ADC2 conversions to be initiated by software commands, timer overflows, or an external input signal. ADC2 conversions may also be synchronized with ADC0 software-commanded conversions. Conversion completions are indicated by a status bit and an interrupt (if enabled), and the resulting 8-bit data word is latched into an SFR upon completion.

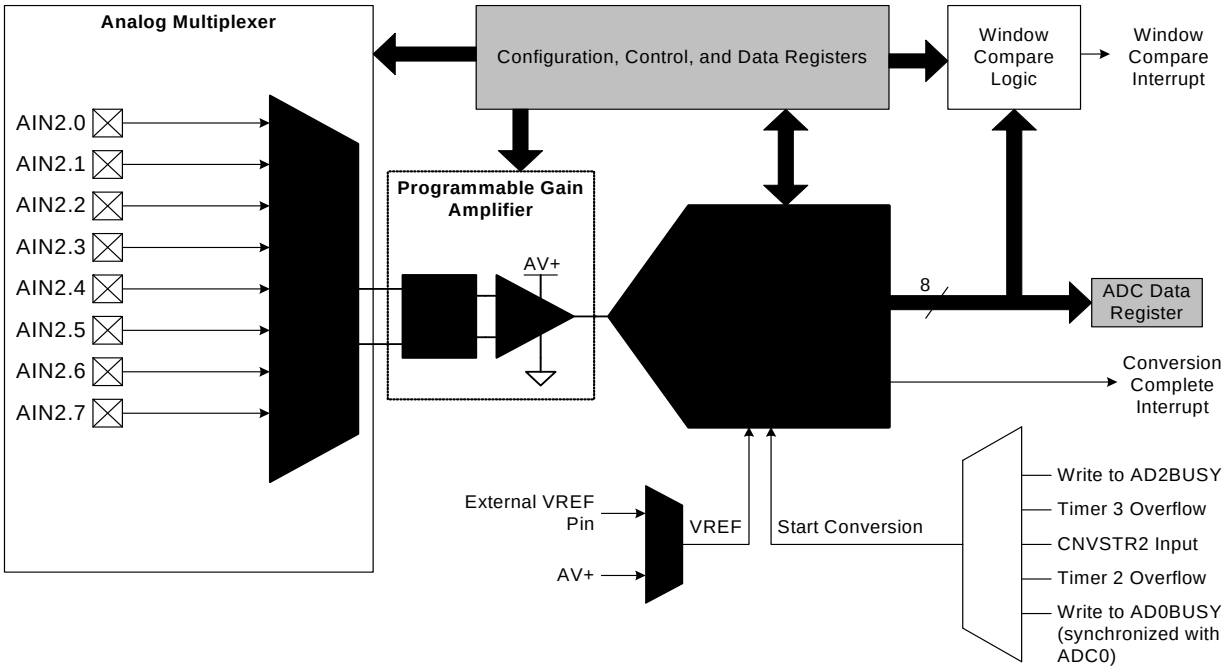

Figure 1.14. 8-Bit ADC Diagram

Table 4.1. Pin Definitions (Continued)

Name	Pin Numbers				Type	Description
	‘F120 ‘F122 ‘F124 ‘F126	‘F121 ‘F123 ‘F125 ‘F127	‘F130 ‘F132	‘F131 ‘F133		
A8m/A0/P6.0	80		80		D I/O	Bit 8 External Memory Address bus (Multiplexed mode) Bit 0 External Memory Address bus (Non-multiplexed mode) Port 6.0 See Port Input/Output section for complete description.
A9m/A1/P6.1	79		79		D I/O	Port 6.1. See Port Input/Output section for complete description.
A10m/A2/P6.2	78		78		D I/O	Port 6.2. See Port Input/Output section for complete description.
A11m/A3/P6.3	77		77		D I/O	Port 6.3. See Port Input/Output section for complete description.
A12m/A4/P6.4	76		76		D I/O	Port 6.4. See Port Input/Output section for complete description.
A13m/A5/P6.5	75		75		D I/O	Port 6.5. See Port Input/Output section for complete description.
A14m/A6/P6.6	74		74		D I/O	Port 6.6. See Port Input/Output section for complete description.
A15m/A7/P6.7	73		73		D I/O	Port 6.7. See Port Input/Output section for complete description.
AD0/D0/P7.0	72		72		D I/O	Bit 0 External Memory Address/Data bus (Multiplexed mode) Bit 0 External Memory Data bus (Non-multiplexed mode) Port 7.0 See Port Input/Output section for complete description.
AD1/D1/P7.1	71		71		D I/O	Port 7.1. See Port Input/Output section for complete description.
AD2/D2/P7.2	70		70		D I/O	Port 7.2. See Port Input/Output section for complete description.
AD3/D3/P7.3	69		69		D I/O	Port 7.3. See Port Input/Output section for complete description.
AD4/D4/P7.4	68		68		D I/O	Port 7.4. See Port Input/Output section for complete description.

SFR Definition 5.2. AMX0SL: AMUX0 Channel Select

SFR Page: 0
SFR Address: 0xBB

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	AMX0AD3	AMX0AD2	AMX0AD1	AMX0AD0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits7–4: UNUSED. Read = 0000b; Write = don't care.
Bits3–0: AMX0AD3–0: AMX0 Address Bits.
0000-1111b: ADC Inputs selected per chart below.

		AMX0AD3–0								
		0000	**0001**	**0010**	**0011**	**0100**	**0101**	**0110**	**0111**	**1xxx**
AMX0CF Bits 3–0	**0000**	AIN0.0	AIN0.1	AIN0.2	AIN0.3	AIN0.4	AIN0.5	AIN0.6	AIN0.7	TEMP SENSOR
	0001	+(AIN0.0) –(AIN0.1)		AIN0.2	AIN0.3	AIN0.4	AIN0.5	AIN0.6	AIN0.7	TEMP SENSOR
	0010	AIN0.0	AIN0.1	+(AIN0.2) –(AIN0.3)		AIN0.4	AIN0.5	AIN0.6	AIN0.7	TEMP SENSOR
	0011	+(AIN0.0) –(AIN0.1)		+(AIN0.2) –(AIN0.3)		AIN0.4	AIN0.5	AIN0.6	AIN0.7	TEMP SENSOR
	0100	AIN0.0	AIN0.1	AIN0.2	AIN0.3	+(AIN0.4) –(AIN0.5)		AIN0.6	AIN0.7	TEMP SENSOR
	0101	+(AIN0.0) –(AIN0.1)		AIN0.2	AIN0.3	+(AIN0.4) –(AIN0.5)		AIN0.6	AIN0.7	TEMP SENSOR
	0110	AIN0.0	AIN0.1	+(AIN0.2) –(AIN0.3)		+(AIN0.4) –(AIN0.5)		AIN0.6	AIN0.7	TEMP SENSOR
	0111	+(AIN0.0) –(AIN0.1)		+(AIN0.2) –(AIN0.3)		+(AIN0.4) –(AIN0.5)		AIN0.6	AIN0.7	TEMP SENSOR
	1000	AIN0.0	AIN0.1	AIN0.2	AIN0.3	AIN0.4	AIN0.5	+(AIN0.6) –(AIN0.7)		TEMP SENSOR
	1001	+(AIN0.0) –(AIN0.1)		AIN0.2	AIN0.3	AIN0.4	AIN0.5	+(AIN0.6) –(AIN0.7)		TEMP SENSOR
	1010	AIN0.0	AIN0.1	+(AIN0.2) –(AIN0.3)		AIN0.4	AIN0.5	+(AIN0.6) –(AIN0.7)		TEMP SENSOR
	1011	+(AIN0.0) –(AIN0.1)		+(AIN0.2) –(AIN0.3)		AIN0.4	AIN0.5	+(AIN0.6) –(AIN0.7)		TEMP SENSOR
	1100	AIN0.0	AIN0.1	AIN0.2	AIN0.3	+(AIN0.4) –(AIN0.5)		+(AIN0.6) –(AIN0.7)		TEMP SENSOR
	1101	+(AIN0.0) –(AIN0.1)		AIN0.2	AIN0.3	+(AIN0.4) –(AIN0.5)		+(AIN0.6) –(AIN0.7)		TEMP SENSOR
	1110	AIN0.0	AIN0.1	+(AIN0.2) –(AIN0.3)		+(AIN0.4) –(AIN0.5)		+(AIN0.6) –(AIN0.7)		TEMP SENSOR
	1111	+(AIN0.0) –(AIN0.1)		+(AIN0.2) –(AIN0.3)		+(AIN0.4) –(AIN0.5)		+(AIN0.6) –(AIN0.7)		TEMP SENSOR

SFR Definition 6.2. AMX0SL: AMUX0 Channel Select

SFR Page: 0
SFR Address: 0xBB

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	AMX0AD3	AMX0AD2	AMX0AD1	AMX0AD0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits7–4: UNUSED. Read = 0000b; Write = don't care.
Bits3–0: AMX0AD3–0: AMX0 Address Bits.
0000-1111b: ADC Inputs selected per chart below.

		AMX0AD3-0								
		0000	**0001**	**0010**	**0011**	**0100**	**0101**	**0110**	**0111**	**1xxx**
AMX0CF Bits 3-0	**0000**	AIN0.0	AIN0.1	AIN0.2	AIN0.3	AIN0.4	AIN0.5	AIN0.6	AIN0.7	TEMP SENSOR
	0001	+(AIN0.0) –(AIN0.1)		AIN0.2	AIN0.3	AIN0.4	AIN0.5	AIN0.6	AIN0.7	TEMP SENSOR
	0010	AIN0.0	AIN0.1	+(AIN0.2) –(AIN0.3)		AIN0.4	AIN0.5	AIN0.6	AIN0.7	TEMP SENSOR
	0011	+(AIN0.0) –(AIN0.1)		+(AIN0.2) –(AIN0.3)		AIN0.4	AIN0.5	AIN0.6	AIN0.7	TEMP SENSOR
	0100	AIN0.0	AIN0.1	AIN0.2	AIN0.3	+(AIN0.4) –(AIN0.5)		AIN0.6	AIN0.7	TEMP SENSOR
	0101	+(AIN0.0) –(AIN0.1)		AIN0.2	AIN0.3	+(AIN0.4) –(AIN0.5)		AIN0.6	AIN0.7	TEMP SENSOR
	0110	AIN0.0	AIN0.1	+(AIN0.2) –(AIN0.3)		+(AIN0.4) –(AIN0.5)		AIN0.6	AIN0.7	TEMP SENSOR
	0111	+(AIN0.0) –(AIN0.1)		+(AIN0.2) –(AIN0.3)		+(AIN0.4) –(AIN0.5)		AIN0.6	AIN0.7	TEMP SENSOR
	1000	AIN0.0	AIN0.1	AIN0.2	AIN0.3	AIN0.4	AIN0.5	+(AIN0.6) –(AIN0.7)		TEMP SENSOR
	1001	+(AIN0.0) –(AIN0.1)		AIN0.2	AIN0.3	AIN0.4	AIN0.5	+(AIN0.6) –(AIN0.7)		TEMP SENSOR
	1010	AIN0.0	AIN0.1	+(AIN0.2) –(AIN0.3)		AIN0.4	AIN0.5	+(AIN0.6) –(AIN0.7)		TEMP SENSOR
	1011	+(AIN0.0) –(AIN0.1)		+(AIN0.2) –(AIN0.3)		AIN0.4	AIN0.5	+(AIN0.6) –(AIN0.7)		TEMP SENSOR
	1100	AIN0.0	AIN0.1	AIN0.2	AIN0.3	+(AIN0.4) –(AIN0.5)		+(AIN0.6) –(AIN0.7)		TEMP SENSOR
	1101	+(AIN0.0) –(AIN0.1)		AIN0.2	AIN0.3	+(AIN0.4) –(AIN0.5)		+(AIN0.6) –(AIN0.7)		TEMP SENSOR
	1110	AIN0.0	AIN0.1	+(AIN0.2) –(AIN0.3)		+(AIN0.4) –(AIN0.5)		+(AIN0.6) –(AIN0.7)		TEMP SENSOR
	1111	+(AIN0.0) –(AIN0.1)		+(AIN0.2) –(AIN0.3)		+(AIN0.4) –(AIN0.5)		+(AIN0.6) –(AIN0.7)		TEMP SENSOR

Table 6.1. 10-Bit ADC0 Electrical Characteristics (C8051F122/3/6/7 and C8051F13x)

V_{DD} = 3.0 V, AV+ = 3.0 V, VREF = 2.40 V (REFBE = 0), PGA Gain = 1, –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
DC Accuracy					
Resolution			10		bits
Integral Nonlinearity		—	—	±1	LSB
Differential Nonlinearity	Guaranteed Monotonic	—	—	±1	LSB
Offset Error		—	±0.5	—	LSB
Full Scale Error	Differential mode	—	–1.5±0.5	—	LSB
Offset Temperature Coefficient		—	±0.25	—	ppm/°C
Dynamic Performance (10 kHz sine-wave input, 0 to 1 dB below Full Scale, 100 ksps					
Signal-to-Noise Plus Distortion		59	—	—	dB
Total Harmonic Distortion	Up to the 5th harmonic	—	–70	—	dB
Spurious-Free Dynamic Range		—	80	—	dB
Conversion Rate					
SAR Clock Frequency		—	—	2.5	MHz
Conversion Time in SAR Clocks		16	—	—	clocks
Track/Hold Acquisition Time		1.5	—	—	µs
Throughput Rate		—	—	100	ksps
Analog Inputs					
Input Voltage Range	Single-ended operation	0	—	VREF	V
***Common-mode Voltage Range**	Differential operation	AGND	—	AV+	V
Input Capacitance		—	10	—	pF
Temperature Sensor					
Linearity[1]		—	±0.2	—	°C
Offset	(Temp = 0 °C)	—	776	—	mV
Offset Error[1,2]	(Temp = 0 °C)	—	±8.5	—	mV
Slope		—	2.86	—	mV/°C
Slope Error[2]		—	±0.034	—	mV/°C
Power Specifications					
Power Supply Current (AV+ supplied to ADC)	Operating Mode, 100 ksps	—	450	900	µA
Power Supply Rejection		—	±0.3	—	mV/V

Notes:
1. Includes ADC offset, gain, and linearity variations.
2. Represents one standard deviation from the mean.

8. DACs, 12-Bit Voltage Mode (C8051F12x Only)

The C8051F12x devices include two on-chip 12-bit voltage-mode Digital-to-Analog Converters (DACs). Each DAC has an output swing of 0 V to (VREF-1LSB) for a corresponding input code range of 0x000 to 0xFFF. The DACs may be enabled/disabled via their corresponding control registers, DAC0CN and DAC1CN. While disabled, the DAC output is maintained in a high-impedance state, and the DAC supply current falls to 1 µA or less. The voltage reference for each DAC is supplied at the VREFD pin (C8051F120/2/4/6 devices) or the VREF pin (C8051F121/3/5/7 devices). Note that the VREF pin on C8051F121/3/5/7 devices may be driven by the internal voltage reference or an external source. If the internal voltage reference is used it must be enabled in order for the DAC outputs to be valid. See **Section "9. Voltage Reference" on page 113** for more information on configuring the voltage reference for the DACs.

8.1. DAC Output Scheduling

Each DAC features a flexible output update mechanism which allows for seamless full-scale changes and supports jitter-free updates for waveform generation. The following examples are written in terms of DAC0, but DAC1 operation is identical.

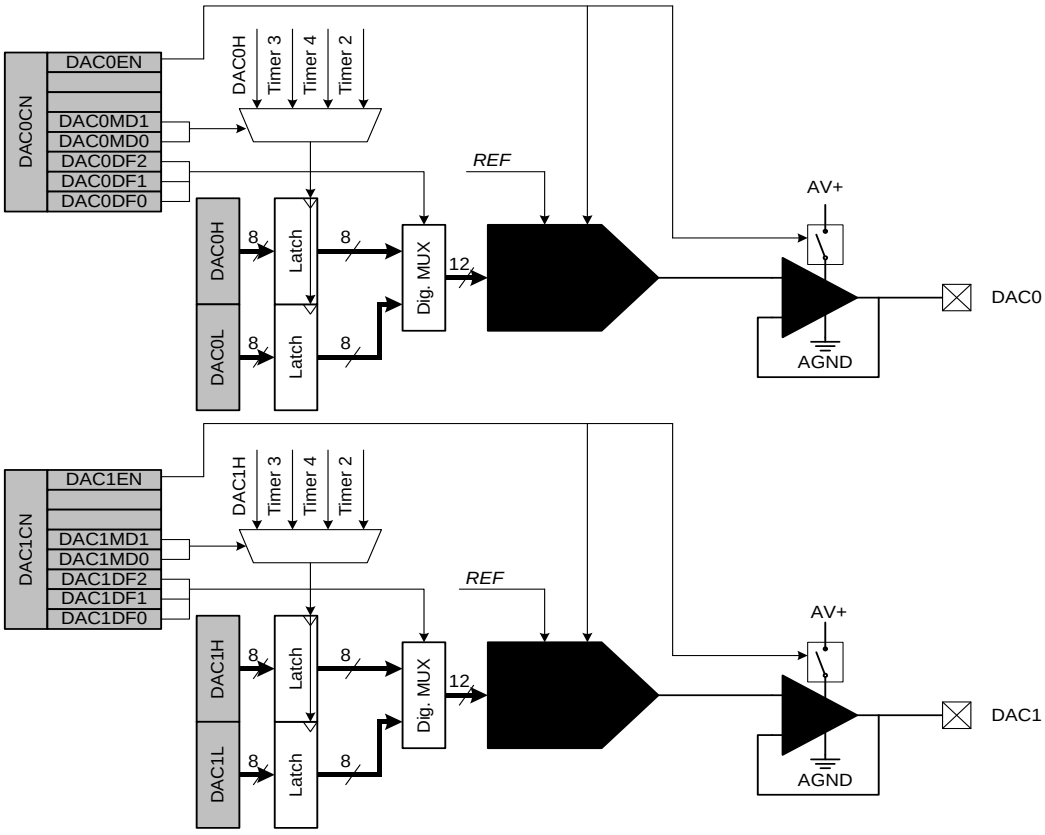

Figure 8.1. DAC Functional Block Diagram

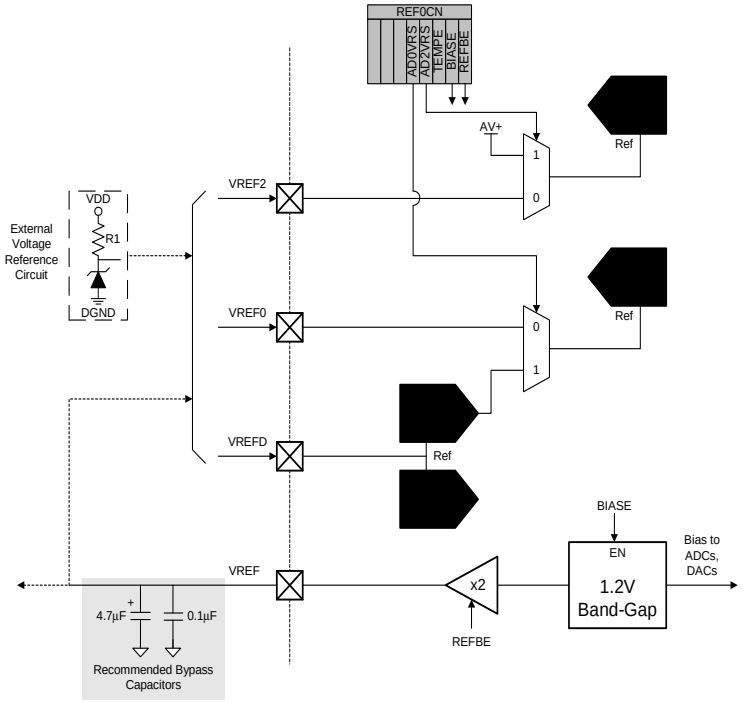

Figure 9.1. Voltage Reference Functional Block Diagram (C8051F120/2/4/6)

SFR Definition 9.1. REF0CN: Reference Control (C8051F120/2/4/6)

SFR Page: 0
SFR Address: 0xD1

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	AD0VRS	AD2VRS	TEMPE	BIASE	REFBE	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits7–5: UNUSED. Read = 000b; Write = don't care.
Bit4: AD0VRS: ADC0 Voltage Reference Select.
0: ADC0 voltage reference from VREF0 pin.
1: ADC0 voltage reference from DAC0 output.
Bit3: AD2VRS: ADC2 Voltage Reference Select.
0: ADC2 voltage reference from VREF2 pin.
1: ADC2 voltage reference from AV+.
Bit2: TEMPE: Temperature Sensor Enable Bit.
0: Internal Temperature Sensor Off.
1: Internal Temperature Sensor On.
Bit1: BIASE: ADC/DAC Bias Generator Enable Bit. (Must be '1' if using ADC, DAC, or VREF).
0: Internal Bias Generator Off.
1: Internal Bias Generator On.
Bit0: REFBE: Internal Reference Buffer Enable Bit.
0: Internal Reference Buffer Off.
1: Internal Reference Buffer On. Internal voltage reference is driven on the VREF pin.

SFR Definition 12.7. MAC0ACC3: MAC0 Accumulator Byte 3

R	R	R	R	R	R	R	R	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x96
SFR Page: 3

Bits 7–0: Byte 3 (bits 31–24) of MAC0 Accumulator.

***Note:** The contents of this register should not be changed by software during the first two MAC0 pipeline stages.

SFR Definition 12.8. MAC0ACC2: MAC0 Accumulator Byte 2

R	R	R	R	R	R	R	R	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x95
SFR Page: 3

Bits 7–0: Byte 2 (bits 23–16) of MAC0 Accumulator.

***Note:** The contents of this register should not be changed by software during the first two MAC0 pipeline stages.

SFR Definition 12.9. MAC0ACC1: MAC0 Accumulator Byte 1

R	R	R	R	R	R	R	R	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x94
SFR Page: 3

Bits 7–0: Byte 1 (bits 15–8) of MAC0 Accumulator.

***Note:** The contents of this register should not be changed by software during the first two MAC0 pipeline stages.

13.1. Power-on Reset

The C8051F120/1/2/3/4/5/6/7 family incorporates a power supply monitor that holds the MCU in the reset state until V_{DD} rises above the V_{RST} level during power-up. See Figure 13.2 for timing diagram, and refer to Table 13.1 for the Electrical Characteristics of the power supply monitor circuit. The $\overline{RST}$ pin is asserted low until the end of the 100 ms V_{DD} Monitor timeout in order to allow the V_{DD} supply to stabilize. The V_{DD} Monitor reset is enabled and disabled using the external V_{DD} monitor enable pin (MONEN). When the V_{DD} Monitor is enabled, it is selected as a reset source using the PORSF bit. If the RSTSRC register is written by firmware, PORSF (RSTSRC.1) must be written to '1' for the V_{DD} Monitor to be effective.

On exit from a power-on reset, the PORSF flag (RSTSRC.1) is set by hardware to logic 1. All of the other reset flags in the RSTSRC Register are indeterminate. PORSF is cleared by all other resets. Since all resets cause program execution to begin at the same location (0x0000) software can read the PORSF flag to determine if a power-up was the cause of reset. The contents of internal data memory should be assumed to be undefined after a power-on reset.

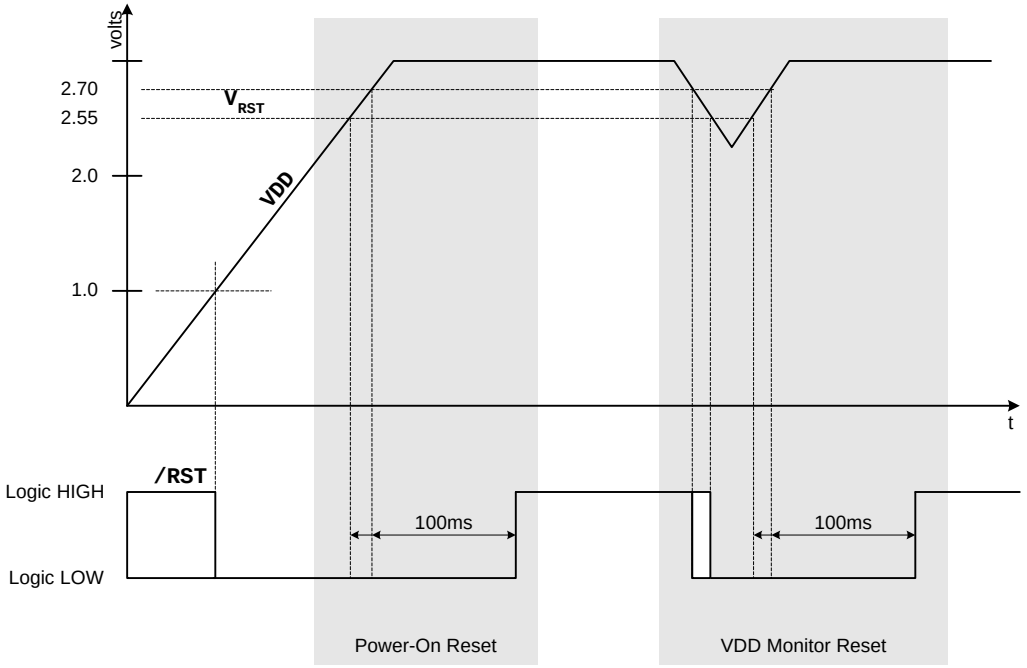

Figure 13.2. Reset Timing

13.2. Power-fail Reset

When a power-down transition or power irregularity causes V_{DD} to drop below V_{RST}, the power supply monitor will drive the $\overline{RST}$ pin low and return the CIP-51 to the reset state. When V_{DD} returns to a level above VRST, the CIP-51 will leave the reset state in the same manner as that for the power-on reset (see Figure 13.2). Note that even though internal data memory contents are not altered by the power-fail reset, it is impossible to determine if V_{DD} dropped below the level required for data retention. If the PORSF flag is set to logic 1, the data may no longer be valid.

Electrical specifications for the precision internal oscillator are given in Table 14.1. Note that the system clock may be derived from the programmed internal oscillator divided by 1, 2, 4, or 8, as defined by the IFCN bits in register OSCICN.

SFR Definition 14.1. OSCICL: Internal Oscillator Calibration.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								Variable
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x8B
SFR Page: F

Bits 7–0: OSCICL: Internal Oscillator Calibration Register.
This register calibrates the internal oscillator period. The reset value for OSCICL defines the internal oscillator base frequency. The reset value is factory calibrated to generate an internal oscillator frequency of 24.5 MHz.

SFR Definition 14.2. OSCICN: Internal Oscillator Control

R/W	R	R/W	R	R/W	R/W	R/W	R/W	Reset Value
IOSCEN	IFRDY	-	-	-	-	IFCN1	IFCN0	11000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x8A
SFR Page: F

Bit 7: IOSCEN: Internal Oscillator Enable Bit.
0: Internal Oscillator Disabled.
1: Internal Oscillator Enabled.
Bit 6: IFRDY: Internal Oscillator Frequency Ready Flag.
0: Internal Oscillator not running at programmed frequency.
1: Internal Oscillator running at programmed frequency.
Bits 5–2: Reserved.
Bits 1–0: IFCN1-0: Internal Oscillator Frequency Control Bits.
00: Internal Oscillator is divided by 8.
01: Internal Oscillator is divided by 4.
10: Internal Oscillator is divided by 2.
11: Internal Oscillator is divided by 1.

Table 15.1. Flash Electrical Characteristics

V_{DD} = 2.7 to 3.6 V; –40 to +85 °C

Parameter	Conditions	Min	Typ	Max	Units
Flash Size[1]	C8051F12x and C8051F130/1		131328[2]		Bytes
Flash Size[1]	C8051F132/3		65792		Bytes
Endurance		20k	100k		Erase/Write
Erase Cycle Time		10	12	14	ms
Write Cycle Time		40	50	60	µs

Notes:
1. Includes 256-byte Scratch Pad Area
2. 1024 Bytes at location 0x1FC00 to 0x1FFFF are reserved.

15.1.1. Non-volatile Data Storage

The Flash memory can be used for non-volatile data storage as well as program code. This allows data such as calibration coefficients to be calculated and stored at run time. Data is written and erased using the MOVX write instruction (as described in **Section 15.1.2** and **Section 15.1.3**) and read using the MOVC instruction. The COBANK bits in register PSBANK (SFR Definition 11.1) control which portion of the Flash memory is targeted by writes and erases of addresses above 0x07FFF. For devices with 64 kB of Flash. the COBANK bits should always remain set to '01' to ensure that Flash write, erase, and read operations are valid.

Two additional 128-byte sectors (256 bytes total) of Flash memory are included for non-volatile data storage. The smaller sector size makes them particularly well suited as general purpose, non-volatile scratch-pad memory. Even though Flash memory can be written a single byte at a time, an entire sector must be erased first. In order to change a single byte of a multi-byte data set, the data must be moved to temporary storage. The 128-byte sector-size facilitates updating data without wasting program memory or RAM space. The 128-byte sectors are double-mapped over the normal Flash memory for MOVC reads and MOVX writes only; their addresses range from 0x00 to 0x7F and from 0x80 to 0xFF (see Figure 15.2). To access the 128-byte sectors, the SFLE bit in PSCTL must be set to logic 1. Code execution from the 128-byte Scratchpad areas is not permitted. The 128-byte sectors can be erased individually, or both at the same time. To erase both sectors simultaneously, the address 0x0400 should be targeted during the erase operation with SFLE set to '1'. See Figure 15.1 for the memory map under different COBANK and SFLE settings.

NOTES:

The replacement algorithm is selected with the Cache Algorithm bit, CHALGM (CCH0TN.3). When CHALGM is cleared to ‘0’, the cache will use the rebound algorithm to replace cache locations. The rebound algorithm replaces locations in order from the beginning of cache memory to the end, and then from the end of cache memory to the beginning. When CHALGM is set to ‘1’, the cache will use the pseudo-random algorithm to replace cache locations. The pseudo-random algorithm uses a pseudo-random number to determine which cache location to replace. The cache can be manually emptied by writing a ‘1’ to the CHFLUSH bit (CCH0CN.4).

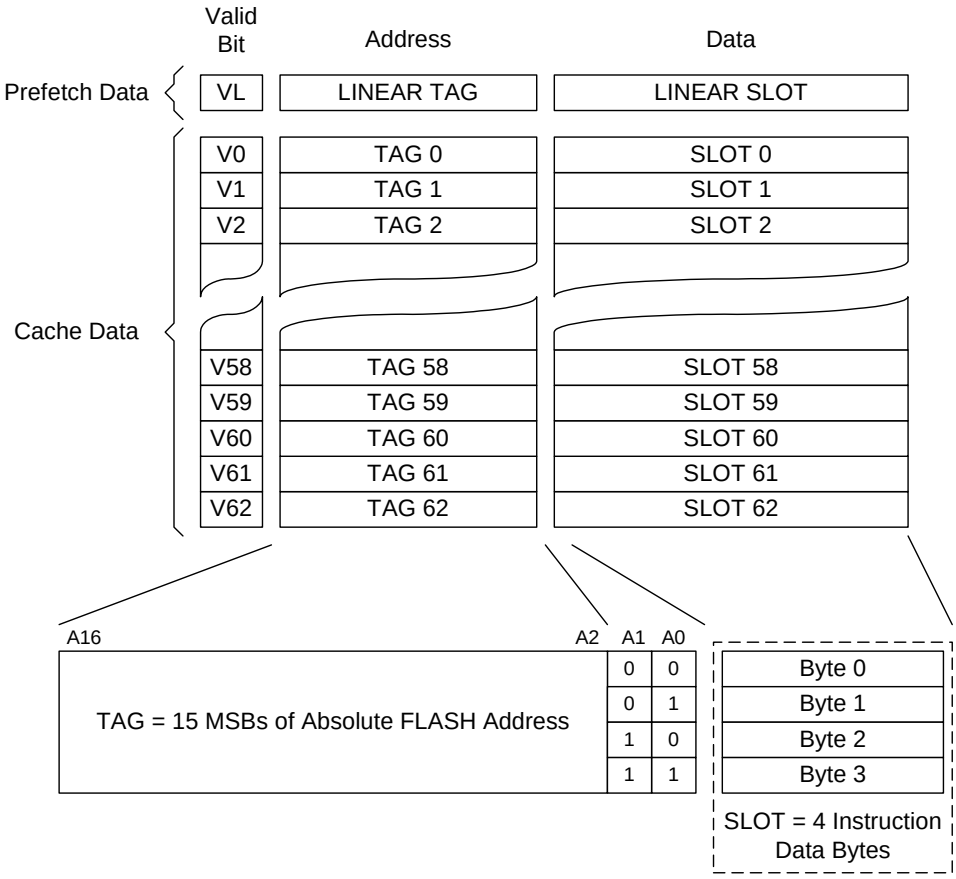

Figure 16.2. Branch Target Cache Organiztion

16.2. Cache and Prefetch Optimization

By default, the branch target cache is configured to provide code speed improvements for a broad range of circumstances. **In most applications, the cache control registers should be left in their reset states.** Sometimes it is desirable to optimize the execution time of a specific routine or critical timing loop. The branch target cache includes options to exclude caching of certain types of data, as well as the ability to pre-load and lock time-critical branch locations to optimize execution speed.

The most basic level of cache control is implemented with the Cache Miss Penalty Threshold bits, CHMSTH (CCH0TN.1-0). If the processor is stalled during a prefetch operation for more clock cycles than the number stored in CHMSTH, the requested data will be cached when it becomes available. The CHMSTH bits are set to zero by default, meaning that any time the processor is stalled, the new data will be cached. If, for example, CHMSTH is equal to 2, any cache miss causing a delay of 3 or 4 clock cycles will be cached, while a cache miss causing a delay of 1-2 clock cycles will not be cached.

17.6.2.3.8-bit MOVX with Bank Select: EMI0CF[4:2] = ‘010’.

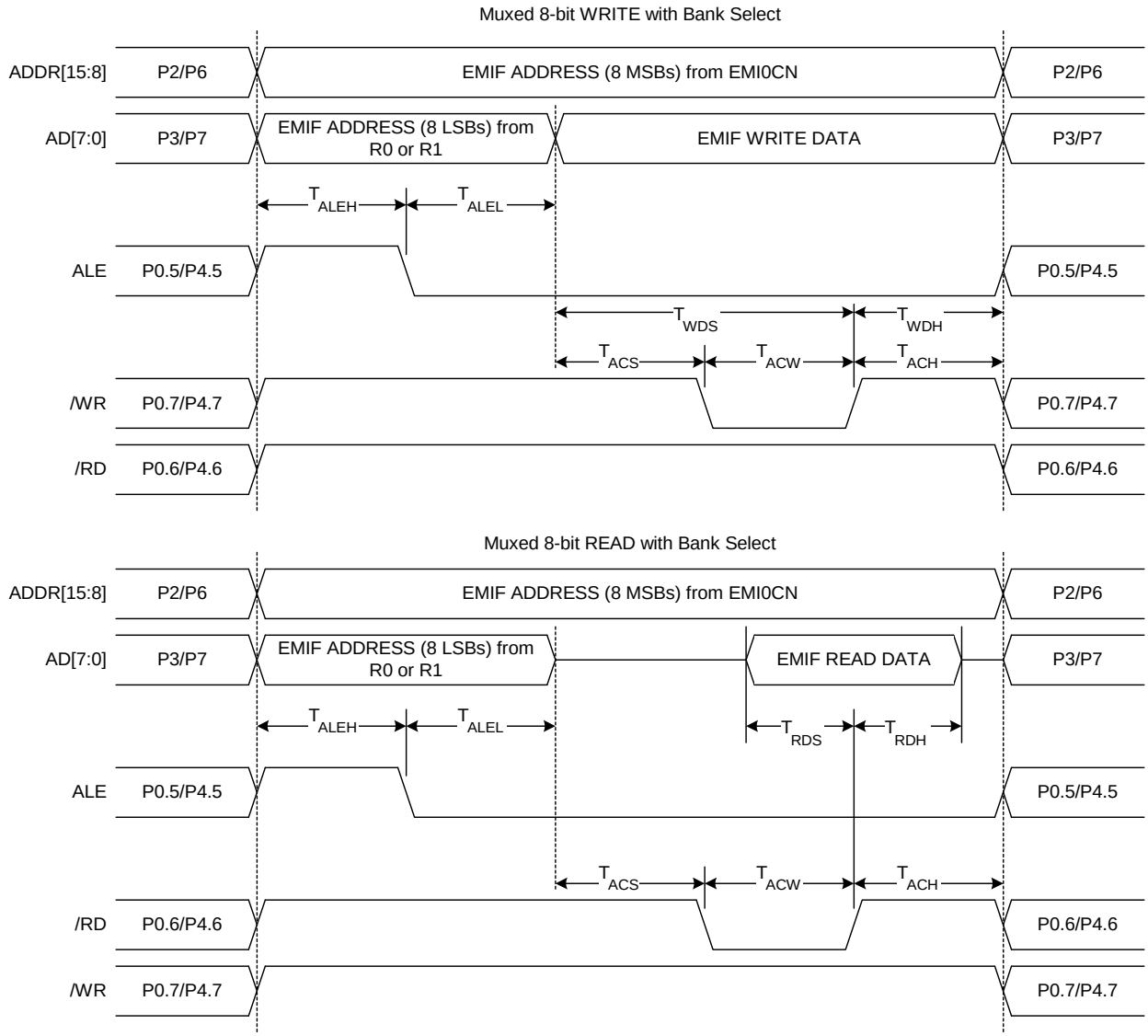

Figure 17.9. Multiplexed 8-bit MOVX with Bank Select Timing

SFR Definition 18.12. P3MDOUT: Port3 Output Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xA7
SFR Page: F

Bits7–0: P3MDOUT.[7:0]: Port3 Output Mode Bits.
0: Port Pin output mode is configured as Open-Drain.
1: Port Pin output mode is configured as Push-Pull.

18.2. Ports 4 through 7 (100-pin TQFP devices only)

All Port pins on Ports 4 through 7 can be accessed as General-Purpose I/O (GPIO) pins by reading and writing the associated Port Data registers (See SFR Definition 18.13, SFR Definition 18.15, SFR Definition 18.17, and SFR Definition 18.19), a set of SFR's which are both bit and byte-addressable. Note also that the Port 4, 5, 6, and 7 registers are located on SFR Page F. The SFRPAGE register must be set to 0x0F to access these Port registers.

A Read of a Port Data register (or Port bit) will always return the logic state present at the pin itself, regardless of whether the Crossbar has allocated the pin for peripheral use or not. An exception to this occurs during the execution of a *read-modify-write* instruction (ANL, ORL, XRL, CPL, INC, DEC, DJNZ, JBC, CLR, SETB, and the bitwise MOV write operation). During the *read* cycle of the *read-modify-write* instruction, it is the contents of the Port Data register, not the state of the Port pins themselves, which is read. Note that at clock rates above 50 MHz, when a pin is written and then immediately read (i.e. a write instruction followed immediately by a read instruction), the propagation delay of the port drivers may cause the read instruction to return the previous logic level of the pin.

18.2.1. Configuring Ports which are not Pinned Out

Although P4, P5, P6, and P7 are not brought out to pins on the 64-pin TQFP devices, the Port Data registers are still present and can be used by software. Because the digital input paths also remain active, it is recommended that these pins not be left in a 'floating' state in order to avoid unnecessary power dissipation arising from the inputs floating to non-valid logic levels. This condition can be prevented by any of the following:

1. Leave the weak pullup devices enabled by setting WEAKPUD (XBR2.7) to a logic 0.
2. Configure the output modes of P4, P5, P6, and P7 to "Push-Pull" by writing PnMDOUT = 0xFF.
3. Force the output states of P4, P5, P6, and P7 to logic 0 by writing zeros to the Port Data registers: P4 = 0x00, P5 = 0x00, P6= 0x00, and P7 = 0x00.

18.2.2. Configuring the Output Modes of the Port Pins

The output mode of each port pin can be configured to be either Open-Drain or Push-Pull. In the Push-Pull configuration, a logic 0 in the associated bit in the Port Data register will cause the Port pin to be driven to GND, and a logic 1 will cause the Port pin to be driven to V_{DD}. In the Open-Drain configuration, a logic 0 in the associated bit in the Port Data register will cause the Port pin to be driven to GND, and a logic 1 will cause the Port pin to assume a high-impedance state. The Open-Drain configuration is useful to prevent contention between devices in systems where the Port pin participates in a shared interconnection in which multiple outputs are connected to the same physical wire.

SFR Definition 18.13. P4: Port4 Data

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
P4.7	P4.6	P4.5	P4.4	P4.3	P4.2	P4.1	P4.0	11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0xC8
SFR Page: F

Bits7–0: P4.[7:0]: Port4 Output Latch Bits.
Write - Output appears on I/O pins.
0: Logic Low Output.
1: Logic High Output (Open-Drain if corresponding P4MDOUT.n bit = 0). See SFR Definition 18.14.
Read - Returns states of I/O pins.
0: P4.n pin is logic low.
1: P4.n pin is logic high.

Note: P4.7 (/WR), P4.6 (/RD), and P4.5 (ALE) can be driven by the External Data Memory Interface. See **Section “17. External Data Memory Interface and On-Chip XRAM” on page 219** for more information.

SFR Definition 18.14. P4MDOUT: Port4 Output Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x9C
SFR Page: F

Bits7–0: P4MDOUT.[7:0]: Port4 Output Mode Bits.
0: Port Pin output mode is configured as Open-Drain.
1: Port Pin output mode is configured as Push-Pull.

SFR Definition 22.2. SBUF1: Serial (UART1) Port Data Buffer

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x99
SFR Page: 1

Bits7–0: SBUF1[7:0]: Serial Data Buffer Bits 7-0 (MSB-LSB)
This SFR accesses two registers; a transmit shift register and a receive latch register. When data is written to SBUF1, it goes to the transmit shift register and is held for serial transmission. Writing a byte to SBUF1 is what initiates the transmission. A read of SBUF1 returns the contents of the receive latch.

Table 22.1. Timer Settings for Standard Baud Rates Using The Internal 24.5 MHz Oscillator

	Frequency: 24.5 MHz						
	Target Baud Rate (bps)	**Baud Rate % Error**	**Oscillator Divide Factor**	**Timer Clock Source**	**SCA1-SCA0 (pre-scale select)***	**T1M***	**Timer 1 Reload Value (hex)**
SYSCLK from Internal Osc.	230400	-0.32%	106	SYSCLK	XX	1	0xCB
	115200	-0.32%	212	SYSCLK	XX	1	0x96
	57600	0.15%	426	SYSCLK	XX	1	0x2B
	28800	-0.32%	848	SYSCLK / 4	01	0	0x96
	14400	0.15%	1704	SYSCLK / 12	00	0	0xB9
	9600	-0.32%	2544	SYSCLK / 12	00	0	0x96
	2400	-0.32%	10176	SYSCLK / 48	10	0	0x96
	1200	0.15%	20448	SYSCLK / 48	10	0	0x2B

X = Don't care

***Note:** SCA1-SCA0 and T1M bit definitions can be found in **Section 23.1**.