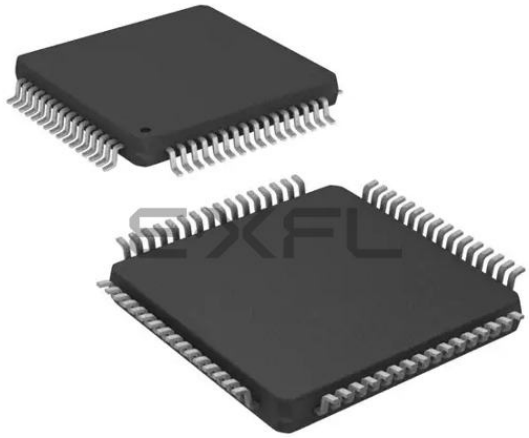

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	100MHz
Connectivity	EBI/EMI, SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	32
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8.25K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x8b, 8x10b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f123

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Table 1.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	Flash Memory	RAM	2-cycle 16 by 16 MAC	External Memory Interface	SMBus/I2C	SPI	UARTS	Timers (16-bit)	Programmable Counter Array	Digital Port I/O's	12-bit 100ksps ADC Inputs	10-bit 100ksps ADC Inputs	8-bit 500ksps ADC Inputs	Voltage Reference	Temperature Sensor	DAC Resolution (bits)	DAC Outputs	Analog Comparators	Lead-Free (RoHS Compliant)	Package
C8051F120	100	128 k	8448	✓	✓	✓	✓	2	5	✓	64	8	-	8	✓	✓	12	2	2	-	100TQFP
C8051F120-GQ	100	128 k	8448	✓	✓	✓	✓	2	5	✓	64	8	-	8	✓	✓	12	2	2	✓	100TQFP
C8051F121	100	128 k	8448	✓	✓	✓	✓	2	5	✓	32	8	-	8	✓	✓	12	2	2	-	64TQFP
C8051F121-GQ	100	128 k	8448	✓	✓	✓	✓	2	5	✓	32	8	-	8	✓	✓	12	2	2	✓	64TQFP
C8051F122	100	128 k	8448	✓	✓	✓	✓	2	5	✓	64	-	8	8	✓	✓	12	2	2	-	100TQFP
C8051F122-GQ	100	128 k	8448	✓	✓	✓	✓	2	5	✓	64	-	8	8	✓	✓	12	2	2	✓	100TQFP
C8051F123	100	128 k	8448	✓	✓	✓	✓	2	5	✓	32	-	8	8	✓	✓	12	2	2	-	64TQFP
C8051F123-GQ	100	128 k	8448	✓	✓	✓	✓	2	5	✓	32	-	8	8	✓	✓	12	2	2	✓	64TQFP
C8051F124	50	128 k	8448	-	✓	✓	✓	2	5	✓	64	8	-	8	✓	✓	12	2	2	-	100TQFP
C8051F124-GQ	50	128 k	8448	-	✓	✓	✓	2	5	✓	64	8	-	8	✓	✓	12	2	2	✓	100TQFP
C8051F125	50	128 k	8448	-	✓	✓	✓	2	5	✓	32	8	-	8	✓	✓	12	2	2	-	64TQFP
C8051F125-GQ	50	128 k	8448	-	✓	✓	✓	2	5	✓	32	8	-	8	✓	✓	12	2	2	✓	64TQFP
C8051F126	50	128 k	8448	-	✓	✓	✓	2	5	✓	64	-	8	8	✓	✓	12	2	2	-	100TQFP
C8051F126-GQ	50	128 k	8448	-	✓	✓	✓	2	5	✓	64	-	8	8	✓	✓	12	2	2	✓	100TQFP
C8051F127	50	128 k	8448	-	✓	✓	✓	2	5	✓	32	-	8	8	✓	✓	12	2	2	-	64TQFP
C8051F127-GQ	50	128 k	8448	-	✓	✓	✓	2	5	✓	32	-	8	8	✓	✓	12	2	2	✓	64TQFP
C8051F130	100	128 k	8448	✓	✓	✓	✓	2	5	✓	64	-	8	-	✓	✓	-	-	2	-	100TQFP
C8051F130-GQ	100	128 k	8448	✓	✓	✓	✓	2	5	✓	64	-	8	-	✓	✓	-	-	2	✓	100TQFP
C8051F131	100	128 k	8448	✓	✓	✓	✓	2	5	✓	32	-	8	-	✓	✓	-	-	2	-	64TQFP
C8051F131-GQ	100	128 k	8448	✓	✓	✓	✓	2	5	✓	32	-	8	-	✓	✓	-	-	2	✓	64TQFP
C8051F132	100	64 k	8448	✓	✓	✓	✓	2	5	✓	64	-	8	-	✓	✓	-	-	2	-	100TQFP
C8051F132-GQ	100	64 k	8448	✓	✓	✓	✓	2	5	✓	64	-	8	-	✓	✓	-	-	2	✓	100TQFP
C8051F133	100	64 k	8448	✓	✓	✓	✓	2	5	✓	32	-	8	-	✓	✓	-	-	2	-	64TQFP
C8051F133-GQ	100	64 k	8448	✓	✓	✓	✓	2	5	✓	32	-	8	-	✓	✓	-	-	2	✓	64TQFP

Table 4.1. Pin Definitions (Continued)

Name	Pin Numbers				Type	Description
	‘F120 ‘F122 ‘F124 ‘F126	‘F121 ‘F123 ‘F125 ‘F127	‘F130 ‘F132	‘F131 ‘F133		
VREF	12	7	12	7	A I/O	Bandgap Voltage Reference Output (all devices). DAC Voltage Reference Input (C8051F121/3/5/7 only).
VREFA		8			A In	ADC0 and ADC2 Voltage Reference Input.
VREF0	16		16	8	A In	ADC0 Voltage Reference Input.
VREF2	17		17		A In	ADC2 Voltage Reference Input.
VREFD	15		15		A In	DAC Voltage Reference Input.
AIN0.0	18	9	18	9	A In	ADC0 Input Channel 0 (See ADC0 Specification for complete description).
AIN0.1	19	10	19	10	A In	ADC0 Input Channel 1 (See ADC0 Specification for complete description).
AIN0.2	20	11	20	11	A In	ADC0 Input Channel 2 (See ADC0 Specification for complete description).
AIN0.3	21	12	21	12	A In	ADC0 Input Channel 3 (See ADC0 Specification for complete description).
AIN0.4	22	13	22	13	A In	ADC0 Input Channel 4 (See ADC0 Specification for complete description).
AIN0.5	23	14	23	14	A In	ADC0 Input Channel 5 (See ADC0 Specification for complete description).
AIN0.6	24	15	24	15	A In	ADC0 Input Channel 6 (See ADC0 Specification for complete description).
AIN0.7	25	16	25	16	A In	ADC0 Input Channel 7 (See ADC0 Specification for complete description).
CP0+	9	4	9	4	A In	Comparator 0 Non-Inverting Input.
CP0-	8	3	8	3	A In	Comparator 0 Inverting Input.
CP1+	7	2	7	2	A In	Comparator 1 Non-Inverting Input.
CP1–	6	1	6	1	A In	Comparator 1 Inverting Input.
DAC0	100	64			A Out	Digital to Analog Converter 0 Voltage Output. (See DAC Specification for complete description).

SFR Definition 5.1. AMX0CF: AMUX0 Configuration

SFR Page: 0
SFR Address: 0xBA

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	AIN67IC	AIN45IC	AIN23IC	AIN01IC	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits7–4: UNUSED. Read = 0000b; Write = don't care.
Bit3: AIN67IC: AIN0.6, AIN0.7 Input Pair Configuration Bit.
0: AIN0.6 and AIN0.7 are independent single-ended inputs.
1: AIN0.6, AIN0.7 are (respectively) +, – differential input pair.
Bit2: AIN45IC: AIN0.4, AIN0.5 Input Pair Configuration Bit.
0: AIN0.4 and AIN0.5 are independent single-ended inputs.
1: AIN0.4, AIN0.5 are (respectively) +, – differential input pair.
Bit1: AIN23IC: AIN0.2, AIN0.3 Input Pair Configuration Bit.
0: AIN0.2 and AIN0.3 are independent single-ended inputs.
1: AIN0.2, AIN0.3 are (respectively) +, – differential input pair.
Bit0: AIN01IC: AIN0.0, AIN0.1 Input Pair Configuration Bit.
0: AIN0.0 and AIN0.1 are independent single-ended inputs.
1: AIN0.0, AIN0.1 are (respectively) +, – differential input pair.

Note: The ADC0 Data Word is in 2's complement format for channels configured as differential.

6.2. ADC Modes of Operation

ADC0 has a maximum conversion speed of 100 ksps. The ADC0 conversion clock is derived from the system clock divided by the value held in the ADCSC bits of register ADC0CF.

6.2.1. Starting a Conversion

A conversion can be initiated in one of four ways, depending on the programmed states of the ADC0 Start of Conversion Mode bits (AD0CM1, AD0CM0) in ADC0CN. Conversions may be initiated by:

1. Writing a ‘1’ to the AD0BUSY bit of ADC0CN;
2. A Timer 3 overflow (i.e. timed continuous conversions);
3. A rising edge detected on the external ADC convert start signal, CNVSTR0;
4. A Timer 2 overflow (i.e. timed continuous conversions).

The AD0BUSY bit is set to logic 1 during conversion and restored to logic 0 when conversion is complete. The falling edge of AD0BUSY triggers an interrupt (when enabled) and sets the AD0INT interrupt flag (ADC0CN.5). Converted data is available in the ADC0 data word MSB and LSB registers, ADC0H, ADC0L. Converted data can be either left or right justified in the ADC0H:ADC0L register pair (see example in Figure 6.5) depending on the programmed state of the AD0LJST bit in the ADC0CN register.

When initiating conversions by writing a ‘1’ to AD0BUSY, the AD0INT bit should be polled to determine when a conversion has completed (ADC0 interrupts may also be used). The recommended polling procedure is shown below.

Step 1. Write a ‘0’ to AD0INT;
Step 2. Write a ‘1’ to AD0BUSY;
Step 3. Poll AD0INT for ‘1’;
Step 4. Process ADC0 data.

When CNVSTR0 is used as a conversion start source, it must be enabled in the crossbar, and the corresponding pin must be set to open-drain, high-impedance mode (see **Section “18. Port Input/Output” on page 235** for more details on Port I/O configuration).

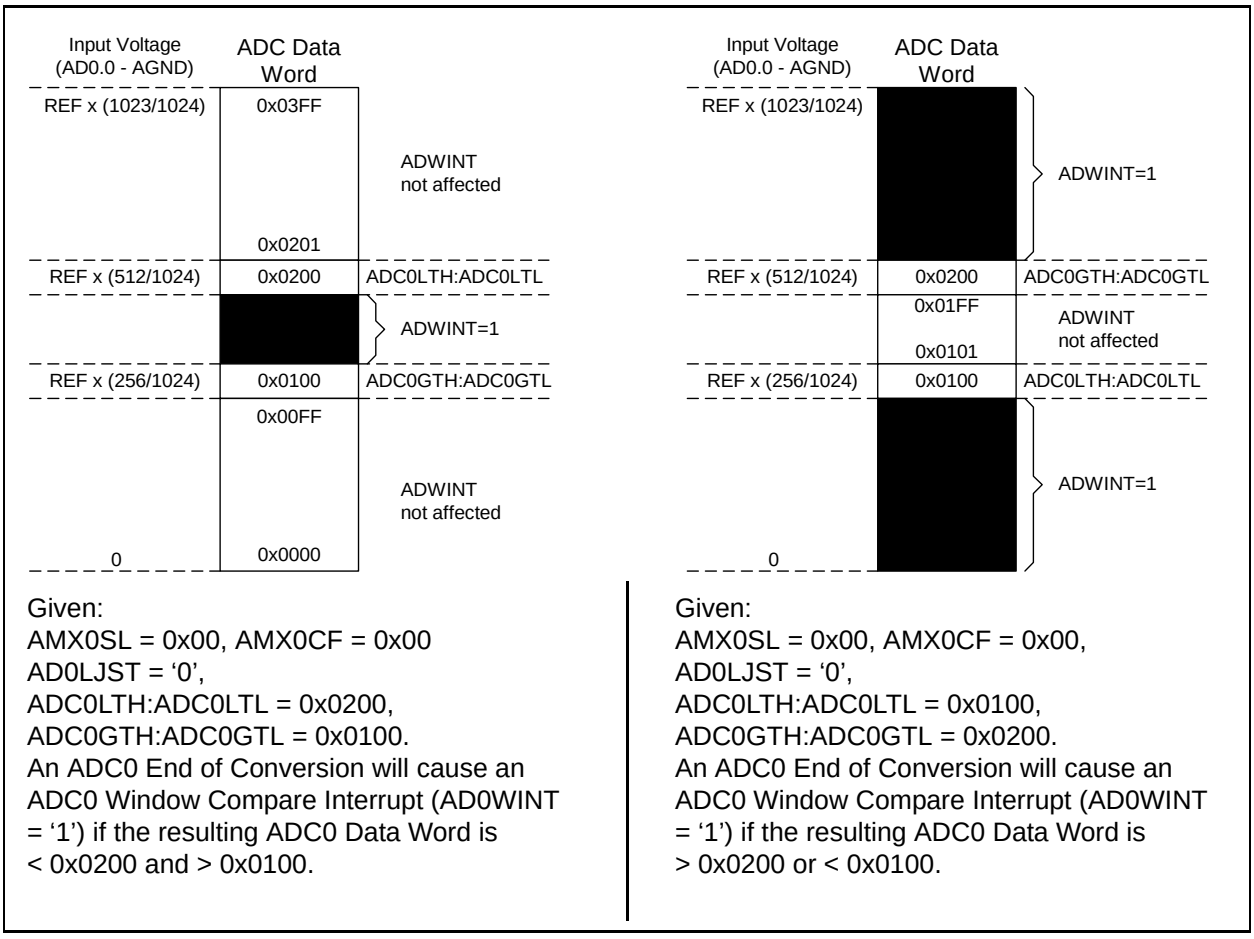


Figure 6.6. 10-Bit ADC0 Window Interrupt Example: Right Justified Single-Ended Data

11.2.6.3.SFR Page Stack Example

The following is an example that shows the operation of the SFR Page Stack during interrupts.

In this example, the SFR Page Control is left in the default enabled state (i.e., SFRPGEN = 1), and the CIP-51 is executing in-line code that is writing values to Port 5 (SFR “P5”, located at address 0xD8 on SFR Page 0x0F). The device is also using the Programmable Counter Array (PCA) and the 10-bit ADC (ADC2) window comparator to monitor a voltage. The PCA is timing a critical control function in its interrupt service routine (ISR), so its interrupt is enabled and is set to *high* priority. The ADC2 is monitoring a voltage that is less important, but to minimize the software overhead its window comparator is being used with an associated ISR that is set to *low* priority. At this point, the SFR page is set to access the Port 5 SFR (SFRPAGE = 0x0F). See Figure 11.5 below.

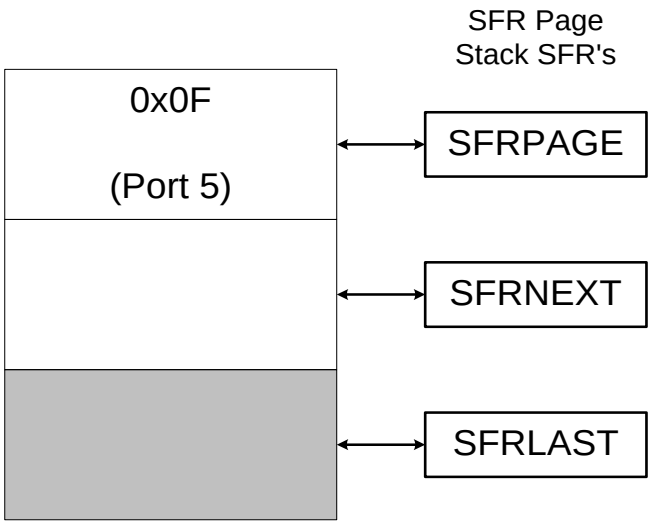


Figure 11.5. SFR Page Stack While Using SFR Page 0x0F To Access Port 5

While CIP-51 executes in-line code (writing values to Port 5 in this example), ADC2 Window Comparator Interrupt occurs. The CIP-51 vectors to the ADC2 Window Comparator ISR and pushes the current SFR Page value (SFR Page 0x0F) into SFRNEXT in the SFR Page Stack. The SFR page needed to access ADC2’s SFR’s is then automatically placed in the SFRPAGE register (SFR Page 0x02). SFRPAGE is considered the “top” of the SFR Page Stack. Software can now access the ADC2 SFR’s. Software may switch to any SFR Page by writing a new value to the SFRPAGE register at any time during the ADC2 ISR to access SFR’s that are not on SFR Page 0x02. See Figure 11.6 below.

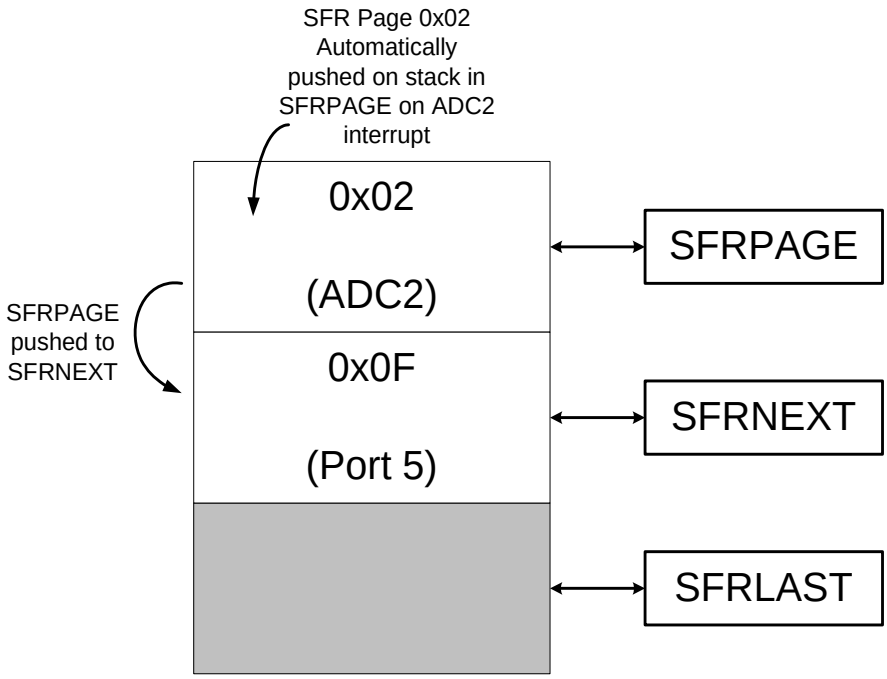


Figure 11.6. SFR Page Stack After ADC2 Window Comparator Interrupt Occurs

While in the ADC2 ISR, a PCA interrupt occurs. Recall the PCA interrupt is configured as a *high* priority interrupt, while the ADC2 interrupt is configured as a *low* priority interrupt. Thus, the CIP-51 will now vector to the high priority PCA ISR. Upon doing so, the CIP-51 will automatically place the SFR page needed to access the PCA's special function registers into the SFRPAGE register, SFR Page 0x00. The value that was in the SFRPAGE register before the PCA interrupt (SFR Page 2 for ADC2) is pushed down the stack into SFRNEXT. Likewise, the value that was in the SFRNEXT register before the PCA interrupt (in this case SFR Page 0x0F for Port 5) is pushed down to the SFRLAST register, the "bottom" of the stack. Note that a value stored in SFRLAST (via a previous software write to the SFRLAST register) will be overwritten. See Figure 11.7 below.

Table 11.3. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved.

Register	Address	SFR Page	Description	Page No.
REF0CN	0xD1	0	Voltage Reference Control	page 114[5], page 116[6], page 117[7]
RSTSRC	0xEF	0	Reset Source	page 182
SADDR0	0xA9	0	UART 0 Slave Address	page 298
SADEN0	0xB9	0	UART 0 Slave Address Mask	page 298
SBUF0	0x99	0	UART 0 Data Buffer	page 298
SBUF1	0x99	1	UART 1 Data Buffer	page 305
SCON0	0x98	0	UART 0 Control	page 296
SCON1	0x98	1	UART 1 Control	page 304
SFRLAST	0x86	All Pages	SFR Stack Last Page	page 143
SFRNEXT	0x85	All Pages	SFR Stack Next Page	page 143
SFRPAGE	0x84	All Pages	SFR Page Select	page 142
SFRPGCN	0x96	F	SFR Page Control	page 142
SMB0ADR	0xC3	0	SMBus Slave Address	page 269
SMB0CN	0xC0	0	SMBus Control	page 266
SMB0CR	0xCF	0	SMBus Clock Rate	page 267
SMB0DAT	0xC2	0	SMBus Data	page 268
SMB0STA	0xC1	0	SMBus Status	page 269
SP	0x81	All Pages	Stack Pointer	page 151
SPI0CFG	0x9A	0	SPI Configuration	page 280
SPI0CKR	0x9D	0	SPI Clock Rate Control	page 282
SPI0CN	0xF8	0	SPI Control	page 281
SPI0DAT	0x9B	0	SPI Data	page 282
SSTA0	0x91	0	UART 0 Status	page 297
TCON	0x88	0	Timer/Counter Control	page 313
TH0	0x8C	0	Timer/Counter 0 High Byte	page 316
TH1	0x8D	0	Timer/Counter 1 High Byte	page 316
TL0	0x8A	0	Timer/Counter 0 Low Byte	page 315
TL1	0x8B	0	Timer/Counter 1 Low Byte	page 316
TMOD	0x89	0	Timer/Counter Mode	page 314
TMR2CF	0xC9	0	Timer/Counter 2 Configuration	page 324
TMR2CN	0xC8	0	Timer/Counter 2 Control	page 324
TMR2H	0xCD	0	Timer/Counter 2 High Byte	page 324
TMR2L	0xCC	0	Timer/Counter 2 Low Byte	page 323
TMR3CF	0xC9	1	Timer 3 Configuration	page 324
TMR3CN	0xC8	1	Timer 3 Control	page 324
TMR3H	0xCD	1	Timer 3 High Byte	page 324
TMR3L	0xCC	1	Timer 3 Low Byte	page 323
TMR4CF	0xC9	2	Timer/Counter 4 Configuration	page 324
TMR4CN	0xC8	2	Timer/Counter 4 Control	page 324
TMR4H	0xCD	2	Timer/Counter 4 High Byte	page 324

SFR Definition 12.2. MAC0STA: MAC0 Status

R	R	R	R	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	MAC0HO	MAC0Z	MAC0SO	MAC0N	00000100
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0xC0
SFR Page: 3

Bits 7–4: UNUSED: Read = 0000b, Write = don't care.

Bit 3: MAC0HO: Hard Overflow Flag.
This bit is set to '1' whenever an overflow out of the MAC0OVR register occurs during a MAC operation (i.e. when MAC0OVR changes from 0x7F to 0x80 or from 0x80 to 0x7F). The hard overflow flag must be cleared in software by directly writing it to '0', or by resetting the MAC logic using the MAC0CA bit in register MAC0CF.

Bit 2: MAC0Z: Zero Flag.
This bit is set to '1' if a MAC0 operation results in an Accumulator value of zero. If the result is non-zero, this bit will be cleared to '0'.

Bit 1: MAC0SO: Soft Overflow Flag.
This bit is set to '1' when a MAC operation causes an overflow into the sign bit (bit 31) of the MAC0 Accumulator. If the overflow condition is corrected after a subsequent MAC operation, this bit is cleared to '0'.

Bit 0: MAC0N: Negative Flag.
If the MAC Accumulator result is negative, this bit will be set to '1'. If the result is positive or zero, this flag will be cleared to '0'.

***Note:** The contents of this register should not be changed by software during the first two MAC0 pipeline stages.

SFR Definition 12.3. MAC0AH: MAC0 A High Byte

R	R	R	R	R	R	R	R	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xC2
SFR Page: 3

Bits 7–0: High Byte (bits 15–8) of MAC0 A Register.

SFR Definition 14.4. OSCXCN: External Oscillator Control

R	R/W	R/W	R/W	R	R/W	R/W	R/W	Reset Value
XTLVLD	XOSCMD2	XOSCMD1	XOSCMD0	-	XFCN2	XFCN1	XFCN0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x8C
SFR Page: F

Bit7: XTLVLD: Crystal Oscillator Valid Flag.
(**Valid only when XOSCMD = 11x.**)
0: Crystal Oscillator is unused or not yet stable.
1: Crystal Oscillator is running and stable.

Bits6–4: XOSCMD2–0: External Oscillator Mode Bits.
00x: External Oscillator circuit off.
010: External CMOS Clock Mode (External CMOS Clock input on XTAL1 pin).
011: External CMOS Clock Mode with divide by 2 stage (External CMOS Clock input on XTAL1 pin).
10x: RC/C Oscillator Mode with divide by 2 stage.
110: Crystal Oscillator Mode.
111: Crystal Oscillator Mode with divide by 2 stage.

Bit3: RESERVED. Read = 0, Write = don't care.

Bits2–0: XFCN2–0: External Oscillator Frequency Control Bits.
000-111: see table below:

XFCN	Crystal (XOSCMD = 11x)	RC (XOSCMD = 10x)	C (XOSCMD = 10x)
000	f ≤ 32 kHz	f ≤ 25 kHz	K Factor = 0.87
001	32 kHz < f ≤ 84 kHz	25 kHz < f ≤ 50 kHz	K Factor = 2.6
010	84 kHz < f ≤ 225 kHz	50 kHz < f ≤ 100 kHz	K Factor = 7.7
011	225 kHz < f ≤ 590 kHz	100 kHz < f ≤ 200 kHz	K Factor = 22
100	590 kHz < f ≤ 1.5 MHz	200 kHz < f ≤ 400 kHz	K Factor = 65
101	1.5 MHz < f ≤ 4 MHz	400 kHz < f ≤ 800 kHz	K Factor = 180
110	4 MHz < f ≤ 10 MHz	800 kHz < f ≤ 1.6 MHz	K Factor = 664
111	10 MHz < f ≤ 30 MHz	1.6 MHz < f ≤ 3.2 MHz	K Factor = 1590

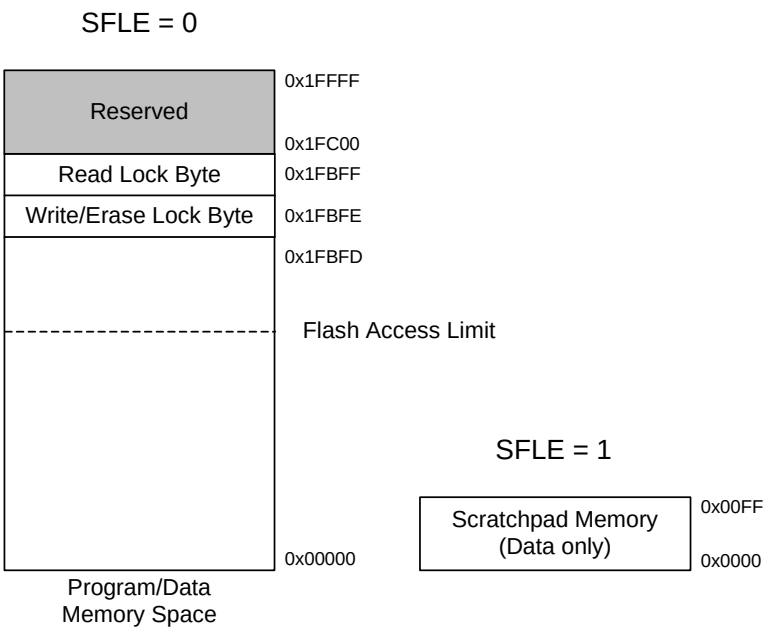
CRYSTAL MODE (Circuit from Figure 14.1, Option 1; XOSCMD = 11x)
Choose XFCN value to match crystal frequency.

RC MODE (Circuit from Figure 14.1, Option 2; XOSCMD = 10x)
Choose XFCN value to match frequency range:
f = **1.23(10^3) / (R * C)**, where
f = frequency of oscillation in MHz
C = capacitor value in pF
R = Pullup resistor value in kΩ

C MODE (Circuit from Figure 14.1, Option 3; XOSCMD = 10x)
Choose K Factor (KF) for the oscillation frequency desired:
f = **KF / (C *** V_{DD}**)**, where
f = frequency of oscillation in MHz
C = capacitor value on XTAL1, XTAL2 pins in pF
V_{DD} = Power Supply on MCU in Volts

Read and Write/Erase Security Bits.
(Bit 7 is MSB.)

Bit	Memory Block
7	0x1C000 - 0x1FBFD
6	0x18000 - 0x1BFFF
5	0x14000 - 0x17FFF
4	0x10000 - 0x13FFF
3	0x0C000 - 0x0FFFF
2	0x08000 - 0x0BFFF
1	0x04000 - 0x07FFF
0	0x00000 - 0x03FFF



Flash Read Lock Byte

Bits7–0: Each bit locks a corresponding block of memory. (Bit7 is MSB).

0: Read operations are locked (disabled) for corresponding block across the JTAG interface.

1: Read operations are unlocked (enabled) for corresponding block across the JTAG interface.

Flash Write/Erase Lock Byte

Bits7–0: Each bit locks a corresponding block of memory.

0: Write/Erase operations are locked (disabled) for corresponding block across the JTAG interface.

1: Write/Erase operations are unlocked (enabled) for corresponding block across the JTAG interface.

NOTE: When the highest block is locked, the security bytes may be written but not erased.

Flash access Limit Register (FLACL)

The Flash Access Limit is defined by the setting of the FLACL register, as described in SFR Definition 15.1. Firmware running at or above this address is prohibited from using the MOVX and MOVC instructions to read, write, or erase Flash locations below this address.

Figure 15.2. 128 kB Flash Memory Map and Security Bytes

Table 18.1. Port I/O DC Electrical Characteristics

V_{DD} = 2.7 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Output High Voltage (V_{OH})	I_{OH} = -3 mA, Port I/O Push-Pull I_{OH} = -10 µA, Port I/O Push-Pull I_{OH} = -10 mA, Port I/O Push-Pull	V_{DD} – 0.7 V_{DD} – 0.1	 V_{DD} – 0.8		V
Output Low Voltage (V_{OL})	I_{OL} = 8.5 mA I_{OL} = 10 µA I_{OL} = 25 mA		 1.0	0.6 0.1	V
Input High Voltage (VIH)		0.7 x V_{DD}			
Input Low Voltage (VIL)				0.3 x V_{DD}	
Input Leakage Current	DGND < Port Pin < V_{DD}, Pin Tri-state Weak Pullup Off Weak Pullup On		 10	± 1	µA
Input Capacitance			5		pF

SFR Definition 18.12. P3MDOUT: Port3 Output Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xA7
SFR Page: F

Bits7–0: P3MDOUT.[7:0]: Port3 Output Mode Bits.
0: Port Pin output mode is configured as Open-Drain.
1: Port Pin output mode is configured as Push-Pull.

18.2. Ports 4 through 7 (100-pin TQFP devices only)

All Port pins on Ports 4 through 7 can be accessed as General-Purpose I/O (GPIO) pins by reading and writing the associated Port Data registers (See SFR Definition 18.13, SFR Definition 18.15, SFR Definition 18.17, and SFR Definition 18.19), a set of SFR's which are both bit and byte-addressable. Note also that the Port 4, 5, 6, and 7 registers are located on SFR Page F. The SFRPAGE register must be set to 0x0F to access these Port registers.

A Read of a Port Data register (or Port bit) will always return the logic state present at the pin itself, regardless of whether the Crossbar has allocated the pin for peripheral use or not. An exception to this occurs during the execution of a *read-modify-write* instruction (ANL, ORL, XRL, CPL, INC, DEC, DJNZ, JBC, CLR, SETB, and the bitwise MOV write operation). During the *read* cycle of the *read-modify-write* instruction, it is the contents of the Port Data register, not the state of the Port pins themselves, which is read. Note that at clock rates above 50 MHz, when a pin is written and then immediately read (i.e. a write instruction followed immediately by a read instruction), the propagation delay of the port drivers may cause the read instruction to return the previous logic level of the pin.

18.2.1. Configuring Ports which are not Pinned Out

Although P4, P5, P6, and P7 are not brought out to pins on the 64-pin TQFP devices, the Port Data registers are still present and can be used by software. Because the digital input paths also remain active, it is recommended that these pins not be left in a 'floating' state in order to avoid unnecessary power dissipation arising from the inputs floating to non-valid logic levels. This condition can be prevented by any of the following:

1. Leave the weak pullup devices enabled by setting WEAKPUD (XBR2.7) to a logic 0.
2. Configure the output modes of P4, P5, P6, and P7 to "Push-Pull" by writing PnMDOUT = 0xFF.
3. Force the output states of P4, P5, P6, and P7 to logic 0 by writing zeros to the Port Data registers: P4 = 0x00, P5 = 0x00, P6= 0x00, and P7 = 0x00.

18.2.2. Configuring the Output Modes of the Port Pins

The output mode of each port pin can be configured to be either Open-Drain or Push-Pull. In the Push-Pull configuration, a logic 0 in the associated bit in the Port Data register will cause the Port pin to be driven to GND, and a logic 1 will cause the Port pin to be driven to V_{DD}. In the Open-Drain configuration, a logic 0 in the associated bit in the Port Data register will cause the Port pin to be driven to GND, and a logic 1 will cause the Port pin to assume a high-impedance state. The Open-Drain configuration is useful to prevent contention between devices in systems where the Port pin participates in a shared interconnection in which multiple outputs are connected to the same physical wire.

SFR Definition 19.4. SMB0ADR: SMBus0 Address

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
SLV6	SLV5	SLV4	SLV3	SLV2	SLV1	SLV0	GC	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xC3
SFR Page: 0

Bits7–1: SLV6–SLV0: SMBus0 Slave Address.
These bits are loaded with the 7-bit slave address to which SMBus0 will respond when operating as a slave transmitter or slave receiver. SLV6 is the most significant bit of the address and corresponds to the first bit of the address byte received.

Bit0: GC: General Call Address Enable.
This bit is used to enable general call address (0x00) recognition.
0: General call address is ignored.
1: General call address is recognized.

19.4.5. Status Register

The SMB0STA Status register holds an 8-bit status code indicating the current state of the SMBus0 interface. There are 28 possible SMBus0 states, each with a corresponding unique status code. The five most significant bits of the status code vary while the three least-significant bits of a valid status code are fixed at zero when SI = '1'. Therefore, all possible status codes are multiples of eight. This facilitates the use of status codes in software as an index used to branch to appropriate service routines (allowing 8 bytes of code to service the state or jump to a more extensive service routine).

For the purposes of user software, the contents of the SMB0STA register is only defined when the SI flag is logic 1. Software should never write to the SMB0STA register; doing so will yield indeterminate results. The 28 SMBus0 states, along with their corresponding status codes, are given in Table 1.1.

SFR Definition 19.5. SMB0STA: SMBus0 Status

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
STA7	STA6	STA5	STA4	STA3	STA2	STA1	STA0	11111000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xC1
SFR Page: 0

Bits7–3: STA7–STA3: SMBus0 Status Code.
These bits contain the SMBus0 Status Code. There are 28 possible status codes; each status code corresponds to a single SMBus state. A valid status code is present in SMB0STA when the SI flag (SMB0CN.3) is set to logic 1. The content of SMB0STA is not defined when the SI flag is logic 0. Writing to the SMB0STA register at any time will yield indeterminate results.

Bits2–0: STA2–STA0: The three least significant bits of SMB0STA are always read as logic 0 when the SI flag is logic 1.

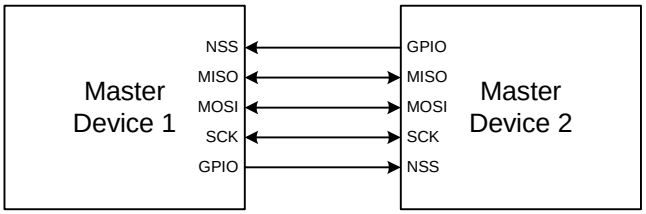


Figure 20.2. Multiple-Master Mode Connection Diagram

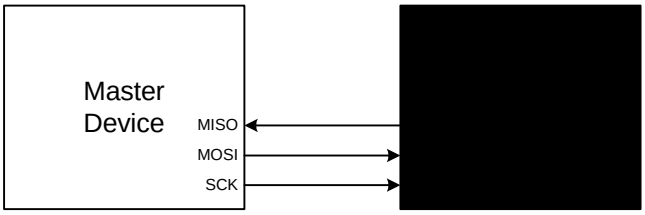


Figure 20.3. 3-Wire Single Master and Slave Mode Connection Diagram

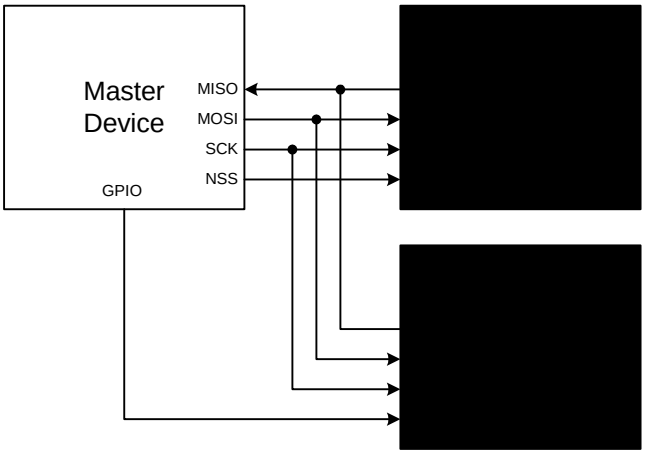


Figure 20.4. 4-Wire Single Master and Slave Mode Connection Diagram

24.2.6. 16-Bit Pulse Width Modulator Mode

Each PCA0 module may also be operated in 16-Bit PWM mode. In this mode, the 16-bit capture/compare module defines the number of PCA0 clocks for the low time of the PWM signal. When the PCA0 counter matches the module contents, the output on CEXn is asserted high; when the counter overflows, CEXn is asserted low. To output a varying duty cycle, new value writes should be synchronized with PCA0 CCFn match interrupts. 16-Bit PWM Mode is enabled by setting the ECOMn, PWMn, and PWM16n bits in the PCA0CPMn register. For a varying duty cycle, CCFn should also be set to logic 1 to enable match interrupts. The duty cycle for 16-Bit PWM Mode is given by Equation 24.3.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to ‘0’; writing to PCA0CPHn sets ECOMn to ‘1’.

Equation 24.3. 16-Bit PWM Duty Cycle

$$DutyCycle = \frac{(65536 - PCA0CPn)}{65536}$$

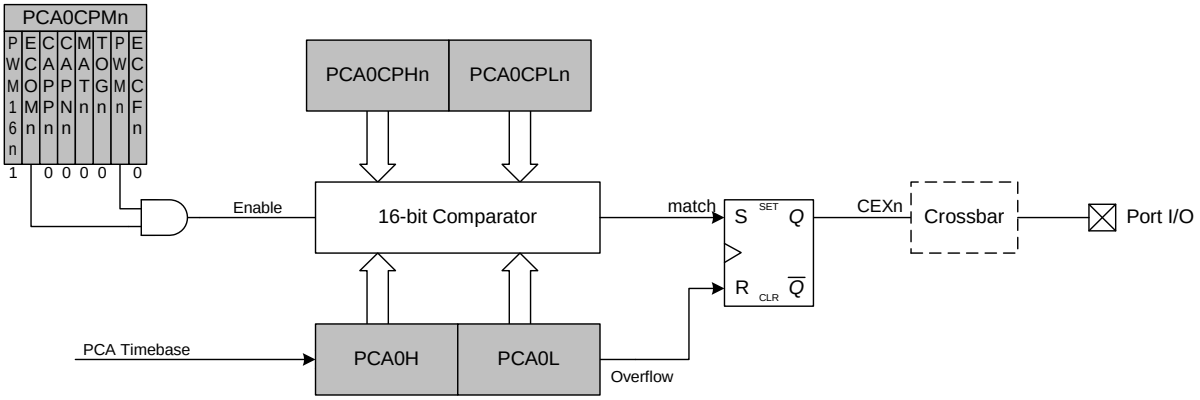


Figure 24.9. PCA 16-Bit PWM Mode

24.3. Register Descriptions for PCA0

Following are detailed descriptions of the special function registers related to the operation of PCA0.

SFR Definition 24.1. PCA0CN: PCA Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
CF	CR	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xD8
SFR Page: 0

Bit7: CF: PCA Counter/Timer Overflow Flag.
Set by hardware when the PCA0 Counter/Timer overflows from 0xFFFF to 0x0000. When the Counter/Timer Overflow (CF) interrupt is enabled, setting this bit causes the CPU to vector to the CF interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.

Bit6: CR: PCA0 Counter/Timer Run Control.
This bit enables/disables the PCA0 Counter/Timer.
0: PCA0 Counter/Timer disabled.
1: PCA0 Counter/Timer enabled.

Bit5: CCF5: PCA0 Module 5 Capture/Compare Flag.
This bit is set by hardware when a match or capture occurs. When the CCF interrupt is enabled, setting this bit causes the CPU to vector to the CCF interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.

Bit4: CCF4: PCA0 Module 4 Capture/Compare Flag.
This bit is set by hardware when a match or capture occurs. When the CCF interrupt is enabled, setting this bit causes the CPU to vector to the CCF interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.

Bit3: CCF3: PCA0 Module 3 Capture/Compare Flag.
This bit is set by hardware when a match or capture occurs. When the CCF interrupt is enabled, setting this bit causes the CPU to vector to the CCF interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.

Bit2: CCF2: PCA0 Module 2 Capture/Compare Flag.
This bit is set by hardware when a match or capture occurs. When the CCF interrupt is enabled, setting this bit causes the CPU to vector to the CCF interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.

Bit1: CCF1: PCA0 Module 1 Capture/Compare Flag.
This bit is set by hardware when a match or capture occurs. When the CCF interrupt is enabled, setting this bit causes the CPU to vector to the CCF interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.

Bit0: CCF0: PCA0 Module 0 Capture/Compare Flag.
This bit is set by hardware when a match or capture occurs. When the CCF interrupt is enabled, setting this bit causes the CPU to vector to the CCF interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.