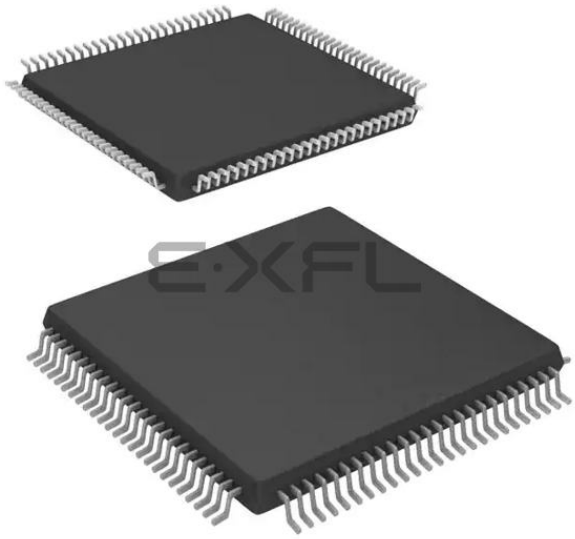

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	64
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x8b, 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f124

Table of Contents

List of Registers

2. Absolute Maximum Ratings

Table 2.1. Absolute Maximum Ratings*

Parameter	Conditions	Min	Typ	Max	Units
Ambient temperature under bias		–55	—	125	°C
Storage Temperature		–65	—	150	°C
Voltage on any Pin (except V_{DD} and Port I/O) with Respect to DGND		–0.3	—	V_{DD} + 0.3	V
Voltage on any Port I/O Pin or $\overline{RST}$ with Respect to DGND		–0.3	—	5.8	V
Voltage on V_{DD} with Respect to DGND		–0.3	—	4.2	V
Maximum Total Current through V_{DD}, AV+, DGND, and AGND		—	—	800	mA
Maximum Output Current Sunk by any Port pin		—	—	100	mA
Maximum Output Current Sunk by any other I/O pin		—	—	50	mA
Maximum Output Current Sourced by any Port pin		—	—	100	mA
Maximum Output Current Sourced by any other I/O Pin		—	—	50	mA

***Note:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

The Temperature Sensor transfer function is shown in Figure 5.2. The output voltage (V_{TEMP}) is the PGA input when the Temperature Sensor is selected by bits AMX0AD3-0 in register AMX0SL; this voltage will be amplified by the PGA according to the user-programmed PGA settings. Typical values for the Slope and Offset parameters can be found in Table 5.1.

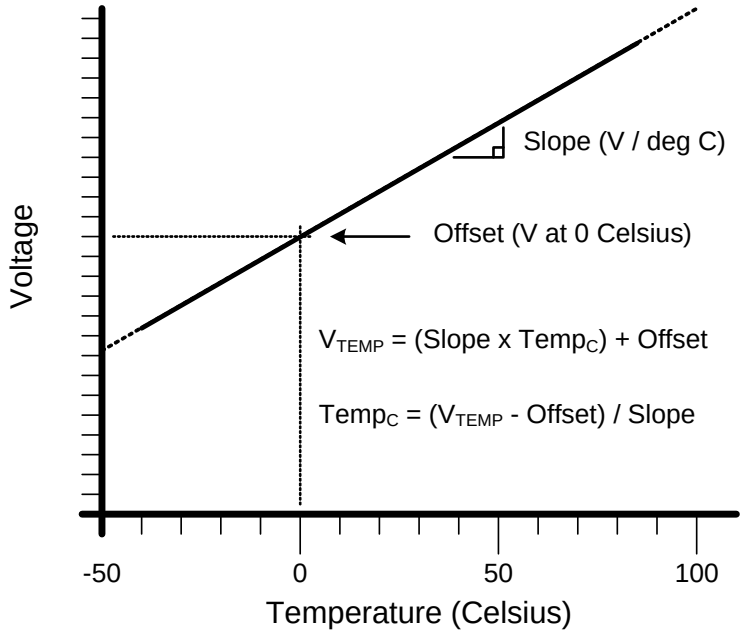

Figure 5.2. Typical Temperature Sensor Transfer Function

SFR Definition 5.4. ADC0CN: ADC0 Control

SFR Page: 0
SFR Address: 0xE8 (bit addressable)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
AD0EN	AD0TM	AD0INT	AD0BUSY	AD0CM1	AD0CM0	AD0WINT	AD0LJST	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bit7: AD0EN: ADC0 Enable Bit.
0: ADC0 Disabled. ADC0 is in low-power shutdown.
1: ADC0 Enabled. ADC0 is active and ready for data conversions.

Bit6: AD0TM: ADC Track Mode Bit.
0: When the ADC is enabled, tracking is continuous unless a conversion is in process.
1: Tracking Defined by ADCM1-0 bits.

Bit5: AD0INT: ADC0 Conversion Complete Interrupt Flag.
This flag must be cleared by software.
0: ADC0 has not completed a data conversion since the last time this flag was cleared.
1: ADC0 has completed a data conversion.

Bit4: AD0BUSY: ADC0 Busy Bit.
Read:
0: ADC0 Conversion is complete or a conversion is not currently in progress. AD0INT is set to logic 1 on the falling edge of AD0BUSY.
1: ADC0 Conversion is in progress.
Write:
0: No Effect.
1: Initiates ADC0 Conversion if AD0CM1-0 = 00b.

Bits3–2: AD0CM1–0: ADC0 Start of Conversion Mode Select.
If AD0TM = 0:
00: ADC0 conversion initiated on every write of ‘1’ to AD0BUSY.
01: ADC0 conversion initiated on overflow of Timer 3.
10: ADC0 conversion initiated on rising edge of external CNVSTR0.
11: ADC0 conversion initiated on overflow of Timer 2.
If AD0TM = 1:
00: Tracking starts with the write of ‘1’ to AD0BUSY and lasts for 3 SAR clocks, followed by conversion.
01: Tracking started by the overflow of Timer 3 and lasts for 3 SAR clocks, followed by conversion.
10: ADC0 tracks only when CNVSTR0 input is logic low; conversion starts on rising CNVSTR0 edge.
11: Tracking started by the overflow of Timer 2 and lasts for 3 SAR clocks, followed by conversion.

Bit1: AD0WINT: ADC0 Window Compare Interrupt Flag.
This bit must be cleared by software.
0: ADC0 Window Comparison Data match has not occurred since this flag was last cleared.
1: ADC0 Window Comparison Data match has occurred.

Bit0: AD0LJST: ADC0 Left Justify Select.
0: Data in ADC0H:ADC0L registers are right-justified.
1: Data in ADC0H:ADC0L registers are left-justified.

SFR Definition 7.6. ADC2GT: ADC2 Greater-Than Data Byte

SFR Page: 2
SFR Address: 0xC4

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits7–0: ADC2 Greater-Than Data Word.

SFR Definition 7.7. ADC2LT: ADC2 Less-Than Data Byte

SFR Page: 2
SFR Address: 0xC6

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits7–0: ADC2 Less-Than Data Word.

SFR Definition 11.4. SFRNEXT: SFR Next Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x85
SFR Page: All Pages

Bits7–0: SFR Page Stack Bits: SFR page context is retained upon interrupts/return from interrupts in a 3 byte SFR Page Stack: SFRPAGE is the first entry, SFRNEXT is the second, and SFRLAST is the third entry. The SFR stack bytes may be used alter the context in the SFR Page Stack, and will not cause the stack to 'push' or 'pop'. Only interrupts and return from interrupts cause pushes and pops of the SFR Page Stack.

Write: Sets the SFR Page contained in the second byte of the SFR Stack. This will cause the SFRPAGE SFR to have this SFR page value upon a return from interrupt.

Read: Returns the value of the SFR page contained in the second byte of the SFR stack. This is the value that will go to the SFR Page register upon a return from interrupt.

SFR Definition 11.5. SFRLAST: SFR Last Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x86
SFR Page: All Pages

Bits7–0: SFR Page Stack Bits: SFR page context is retained upon interrupts/return from interrupts in a 3 byte SFR Page Stack: SFRPAGE is the first entry, SFRNEXT is the second, and SFRLAST is the third entry. The SFR stack bytes may be used alter the context in the SFR Page Stack, and will not cause the stack to 'push' or 'pop'. Only interrupts and return from interrupts cause pushes and pops of the SFR Page Stack.

Write: Sets the SFR Page in the last entry of the SFR Stack. This will cause the SFRNEXT SFR to have this SFR page value upon a return from interrupt.

Read: Returns the value of the SFR page contained in the last entry of the SFR stack.

Table 11.3. Special Function Registers

SFRs are listed in alphabetical order. All undefined SFR locations are reserved.

Register	Address	SFR Page	Description	Page No.
ACC	0xE0	All Pages	Accumulator	page 153
ADC0CF	0xBC	0	ADC0 Configuration	page 62[1], page 80[2]
ADC0CN	0xE8	0	ADC0 Control	page 63[1], page 81[2]
ADC0GTH	0xC5	0	ADC0 Greater-Than High Byte	page 66[1], page 84[2]
ADC0GTL	0xC4	0	ADC0 Greater-Than Low Byte	page 66[1], page 84[2]
ADC0H	0xBF	0	ADC0 Data Word High Byte	page 64[1], page 82[2]
ADC0L	0xBE	0	ADC0 Data Word Low Byte	page 64[1], page 82[2]
ADC0LTH	0xC7	0	ADC0 Less-Than High Byte	page 67[1], page 85[2]
ADC0LTL	0xC6	0	ADC0 Less-Than Low Byte	page 67[1], page 85[2]
ADC2	0xBE	2	ADC2 Data Word	page 99[3]
ADC2CF	0xBC	2	ADC2 Configuration	page 97[3]
ADC2CN	0xE8	2	ADC2 Control	page 98[3]
ADC2GT	0xC4	2	ADC2 Greater-Than	page 102[3]
ADC2LT	0xC6	2	ADC2 Less-Than	page 102[3]
AMX0CF	0xBA	0	ADC0 Multiplexer Configuration	page 60[1], page 78[2]
AMX0SL	0xBB	0	ADC0 Multiplexer Channel Select	page 61[1], page 79[2]
AMX2CF	0xBA	2	ADC2 Multiplexer Configuration	page 95[3]
AMX2SL	0xBB	2	ADC2 Multiplexer Channel Select	page 96[3]
B	0xF0	All Pages	B Register	page 153
CCH0CN	0xA1	F	Cache Control	page 215
CCH0LC	0xA3	F	Cache Lock	page 216
CCH0MA	0x9A	F	Cache Miss Accumulator	page 217
CCH0TN	0xA2	F	Cache Tuning	page 216
CKCON	0x8E	0	Clock Control	page 315
CLKSEL	0x97	F	System Clock Select	page 188
CPT0CN	0x88	1	Comparator 0 Control	page 123
CPT0MD	0x89	1	Comparator 0 Configuration	page 123
CPT1CN	0x88	2	Comparator 1 Control	page 124
CPT1MD	0x89	2	Comparator 1 Configuration	page 125
DAC0CN	0xD4	0	DAC0 Control	page 108[3]
DAC0H	0xD3	0	DAC0 High Byte	page 107[3]
DAC0L	0xD2	0	DAC0 Low Byte	page 107[3]
DAC1CN	0xD4	1	DAC1 Control	page 110[3]
DAC1H	0xD3	1	DAC1 High Byte	page 109[3]
DAC1L	0xD2	1	DAC1 Low Byte	page 109[3]
DPH	0x83	All Pages	Data Pointer High Byte	page 151
DPL	0x82	All Pages	Data Pointer Low Byte	page 151

SFR Definition 11.15. EIE2: Extended Interrupt Enable 2

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	ES1	-	EADC2	EWADC2	ET4	EADC0	ET3	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xE7
SFR Page: All Pages

Bit7: UNUSED. Read = 0b, Write = don't care.
Bit6: ES1: Enable UART1 Interrupt.
This bit sets the masking of the UART1 interrupt.
0: Disable UART1 interrupts.
1: Enable UART1 interrupts.
Bit5: UNUSED. Read = 0b, Write = don't care.
Bit4: EADC2: Enable ADC2 End Of Conversion Interrupt.
This bit sets the masking of the ADC2 End of Conversion interrupt.
0: Disable ADC2 End of Conversion interrupts.
1: Enable ADC2 End of Conversion Interrupts.
Bit3: EWADC2: Enable Window Comparison ADC2 Interrupt.
This bit sets the masking of ADC2 Window Comparison interrupt.
0: Disable ADC2 Window Comparison Interrupts.
1: Enable ADC2 Window Comparison Interrupts.
Bit2: ET4: Enable Timer 4 Interrupt
This bit sets the masking of the Timer 4 interrupt.
0: Disable Timer 4 interrupts.
1: Enable Timer 4 interrupts.
Bit1: EADC0: Enable ADC0 End of Conversion Interrupt.
This bit sets the masking of the ADC0 End of Conversion Interrupt.
0: Disable ADC0 End of Conversion Interrupts.
1: Enable ADC0 End of Conversion Interrupts.
Bit0: ET3: Enable Timer 3 Interrupt.
This bit sets the masking of the Timer 3 interrupt.
0: Disable Timer 3 interrupts.
1: Enable Timer 3 interrupts.

12.6. Rounding and Saturation

A Rounding Engine is included, which can be used to provide a rounded result when operating on fractional numbers. MAC0 uses an unbiased rounding algorithm to round the data stored in bits 31–16 of the accumulator, as shown in Table 12.1. Rounding occurs during the third stage of the MAC0 pipeline, after any shift operation, or on a write to the LSB of the accumulator. The rounded results are stored in the rounding registers: MAC0RNDH (SFR Definition 12.12) and MAC0RNDL (SFR Definition 12.13). The accumulator registers are not affected by the rounding engine. Although rounding is primarily used for fractional data, the data in the rounding registers is updated in the same way when operating in integer mode.

Table 12.1. MAC0 Rounding (MAC0SAT = 0)

Accumulator Bits 15–0 (MAC0ACC1:MAC0ACC0)	Accumulator Bits 31–16 (MAC0ACC3:MAC0ACC2)	Rounding Direction	Rounded Results (MAC0RNDH:MAC0RNDL)
Greater Than 0x8000	Anything	Up	(MAC0ACC3:MAC0ACC2) + 1
Less Than 0x8000	Anything	Down	(MAC0ACC3:MAC0ACC2)
Equal To 0x8000	Odd (LSB = 1)	Up	(MAC0ACC3:MAC0ACC2) + 1
Equal To 0x8000	Even (LSB = 0)	Down	(MAC0ACC3:MAC0ACC2)

The rounding engine can also be used to saturate the results stored in the rounding registers. If the MAC0SAT bit is set to '1' and the rounding register overflows, the rounding registers will saturate. When a positive overflow occurs, the rounding registers will show a value of 0x7FFF when saturated. For a negative overflow, the rounding registers will show a value of 0x8000 when saturated. If the MAC0SAT bit is cleared to '0', the rounding registers will not saturate.

12.7. Usage Examples

This section details some software examples for using MAC0. **Section 12.7.1** shows a series of two MAC operations using fractional numbers. **Section 12.7.2** shows a single operation in Multiply Only mode with integer numbers. The last example, shown in **Section 12.7.3**, demonstrates how the left-shift and right-shift operations can be used to modify the accumulator. All of the examples assume that all of the flags in the MAC0STA register are initially set to '0'.

12.7.1. Multiply and Accumulate Example

The example below implements the equation:

$$(0.5 \times 0.25) + (0.5 \times -0.25) = 0.125 - 0.125 = 0.0$$

```
MOV   MAC0CF, #0Ah    ; Set to Clear Accumulator, Use fractional numbers
MOV   MAC0AH, #40h    ; Load MAC0A register with 4000 hex = 0.5 decimal
MOV   MAC0AL, #00h
MOV   MAC0BH, #20h    ; Load MAC0B register with 2000 hex = 0.25 decimal
MOV   MAC0BL, #00h    ; This line initiates the first MAC operation
MOV   MAC0BH, #E0h    ; Load MAC0B register with E000 hex = -0.25 decimal
MOV   MAC0BL, #00h    ; This line initiates the second MAC operation
NOP
NOP                   ; After this instruction, the Accumulator should be equal to 0,
                      ; and the MAC0STA register should be 0x04, indicating a zero
NOP                   ; After this instruction, the Rounding register is updated
```

13.3. External Reset

The external RST pin provides a means for external circuitry to force the MCU into a reset state. Asserting the RST pin low will cause the MCU to enter the reset state. It may be desirable to provide an external pull-up and/or decoupling of the RST pin to avoid erroneous noise-induced resets. The MCU will remain in reset until at least 12 clock cycles after the active-low RST signal is removed. The PINRSF flag (RSTSRC.0) is set on exit from an external reset.

13.4. Missing Clock Detector Reset

The Missing Clock Detector is essentially a one-shot circuit that is triggered by the MCU system clock. If the system clock goes away for more than 100 µs, the one-shot will time out and generate a reset. After a Missing Clock Detector reset, the MCDRSF flag (RSTSRC.2) will be set, signifying the MSD as the reset source; otherwise, this bit reads '0'. The state of the RST pin is unaffected by this reset. Setting the MCDRSF bit, RSTSRC.2 (see Section "**14. Oscillators**" on page **185**) enables the Missing Clock Detector.

13.5. Comparator0 Reset

Comparator0 can be configured as a reset input by writing a '1' to the C0RSEF flag (RSTSRC.5). Comparator0 should be enabled using CPT0CN.7 (see Section "**10. Comparators**" on page **119**) prior to writing to C0RSEF to prevent any turn-on chatter on the output from generating an unwanted reset. The Comparator0 reset is active-low: if the non-inverting input voltage (CP0+ pin) is less than the inverting input voltage (CP0- pin), the MCU is put into the reset state. After a Comparator0 Reset, the C0RSEF flag (RSTSRC.5) will read '1' signifying Comparator0 as the reset source; otherwise, this bit reads '0'. The state of the RST pin is unaffected by this reset.

13.6. External CNVSTR0 Pin Reset

The external CNVSTR0 signal can be configured as a reset input by writing a '1' to the CNVRSEF flag (RSTSRC.6). The CNVSTR0 signal can appear on any of the P0, P1, P2 or P3 I/O pins as described in Section "**18.1. Ports 0 through 3 and the Priority Crossbar Decoder**" on page **238**. Note that the Crossbar must be configured for the CNVSTR0 signal to be routed to the appropriate Port I/O. The Crossbar should be configured and enabled before the CNVRSEF is set. When configured as a reset, CNVSTR0 is active-low and level sensitive. CNVSTR0 cannot be used to start ADC0 conversions when it is configured as a reset source. After a CNVSTR0 reset, the CNVRSEF flag (RSTSRC.6) will read '1' signifying CNVSTR0 as the reset source; otherwise, this bit reads '0'. The state of the /RST pin is unaffected by this reset.

13.7. Watchdog Timer Reset

The MCU includes a programmable Watchdog Timer (WDT) running off the system clock. A WDT overflow will force the MCU into the reset state. To prevent the reset, the WDT must be restarted by application software before overflow. If the system experiences a software or hardware malfunction preventing the software from restarting the WDT, the WDT will overflow and cause a reset. This should prevent the system from running out of control.

Following a reset the WDT is automatically enabled and running with the default maximum time interval. If desired the WDT can be disabled by system software or locked on to prevent accidental disabling. Once locked, the WDT cannot be disabled until the next system reset. The state of the RST pin is unaffected by this reset.

The WDT consists of a 21-bit timer running from the programmed system clock. The timer measures the period between specific writes to its control register. If this period exceeds the programmed limit, a WDT

page 199). **Important Note: Cache reads, cache writes, and the prefetch engine should be disabled whenever the FLRT bits are changed to a lower setting.**

To shut down the PLL, the system clock should be switched to the internal oscillator or a stable external clock source, using the CLKSEL register. Next, disable the PLL by setting PLLEN (PLL0CN.1) to '0'. Finally, the PLL can be powered off, by setting PLLPWR (PLL0CN.0) to '0'. Note that the PLLEN and PLLPWR bits can be cleared at the same time.

SFR Definition 14.5. PLL0CN: PLL Control

R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	Reset Value
-	-	-	PLLLCK	0	PLLSRC	PLLEN	PLLPWR	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x89
SFR Page: F

Bits 7–5: UNUSED: Read = 000b; Write = don't care.
Bit 4: PLLCK: PLL Lock Flag.
0: PLL Frequency is not locked.
1: PLL Frequency is locked.
Bit 3: RESERVED. Must write to '0'.
Bit 2: PLLSRC: PLL Reference Clock Source Select Bit.
0: PLL Reference Clock Source is Internal Oscillator.
1: PLL Reference Clock Source is External Oscillator.
Bit 1: PLLEN: PLL Enable Bit.
0: PLL is held in reset.
1: PLL is enabled. PLLPWR must be '1'.
Bit 0: PLLPWR: PLL Power Enable.
0: PLL bias generator is de-activated. No static power is consumed.
1: PLL bias generator is active. Must be set for PLL to operate.

Table 15.1. Flash Electrical Characteristics

V_{DD} = 2.7 to 3.6 V; –40 to +85 °C

Parameter	Conditions	Min	Typ	Max	Units
Flash Size[1]	C8051F12x and C8051F130/1		131328[2]		Bytes
Flash Size[1]	C8051F132/3		65792		Bytes
Endurance		20k	100k		Erase/Write
Erase Cycle Time		10	12	14	ms
Write Cycle Time		40	50	60	µs

Notes:
1. Includes 256-byte Scratch Pad Area
2. 1024 Bytes at location 0x1FC00 to 0x1FFFF are reserved.

15.1.1. Non-volatile Data Storage

The Flash memory can be used for non-volatile data storage as well as program code. This allows data such as calibration coefficients to be calculated and stored at run time. Data is written and erased using the MOVX write instruction (as described in **Section 15.1.2** and **Section 15.1.3**) and read using the MOVC instruction. The COBANK bits in register PSBANK (SFR Definition 11.1) control which portion of the Flash memory is targeted by writes and erases of addresses above 0x07FFF. For devices with 64 kB of Flash. the COBANK bits should always remain set to '01' to ensure that Flash write, erase, and read operations are valid.

Two additional 128-byte sectors (256 bytes total) of Flash memory are included for non-volatile data storage. The smaller sector size makes them particularly well suited as general purpose, non-volatile scratch-pad memory. Even though Flash memory can be written a single byte at a time, an entire sector must be erased first. In order to change a single byte of a multi-byte data set, the data must be moved to temporary storage. The 128-byte sector-size facilitates updating data without wasting program memory or RAM space. The 128-byte sectors are double-mapped over the normal Flash memory for MOVC reads and MOVX writes only; their addresses range from 0x00 to 0x7F and from 0x80 to 0xFF (see Figure 15.2). To access the 128-byte sectors, the SFLE bit in PSCTL must be set to logic 1. Code execution from the 128-byte Scratchpad areas is not permitted. The 128-byte sectors can be erased individually, or both at the same time. To erase both sectors simultaneously, the address 0x0400 should be targeted during the erase operation with SFLE set to '1'. See Figure 15.1 for the memory map under different COBANK and SFLE settings.

17.6.2. Multiplexed Mode

17.6.2.1.16-bit MOVX: EMI0CF[4:2] = ‘001’, ‘010’, or ‘011’

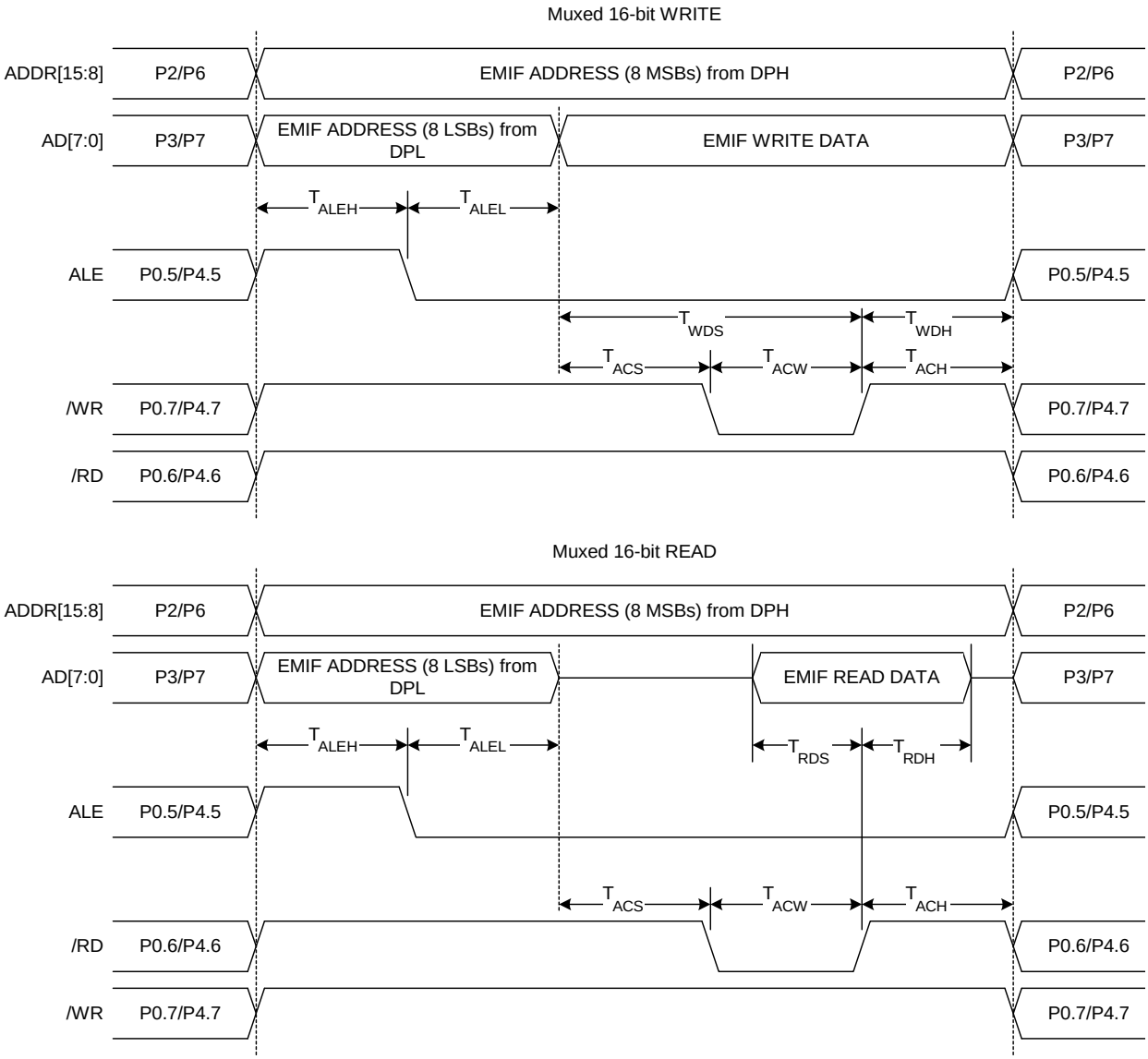

Figure 17.7. Multiplexed 16-bit MOVX Timing

SFR Definition 18.17. P6: Port6 Data

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
P6.7	P6.6	P6.5	P6.4	P6.3	P6.2	P6.1	P6.0	11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0xE8
SFR Page: F

Bits7–0: P6.[7:0]: Port6 Output Latch Bits.
Write - Output appears on I/O pins.
0: Logic Low Output.
1: Logic High Output (Open-Drain if corresponding P6MDOUT bit = 0). See SFR Definition 18.18.
Read - Returns states of I/O pins.
0: P6.n pin is logic low.
1: P6.n pin is logic high.

Note: P6.[7:0] can be driven by the External Data Memory Interface (as Address[15:8] in Multiplexed mode, or as Address[7:0] in Non-multiplexed mode). See **Section “17. External Data Memory Interface and On-Chip XRAM” on page 219** for more information about the External Memory Interface.

SFR Definition 18.18. P6MDOUT: Port6 Output Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x9E
SFR Page: F

Bits7–0: P6MDOUT.[7:0]: Port6 Output Mode Bits.
0: Port Pin output mode is configured as Open-Drain.
1: Port Pin output mode is configured as Push-Pull.

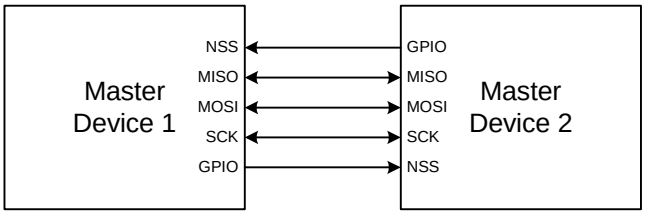

Figure 20.2. Multiple-Master Mode Connection Diagram

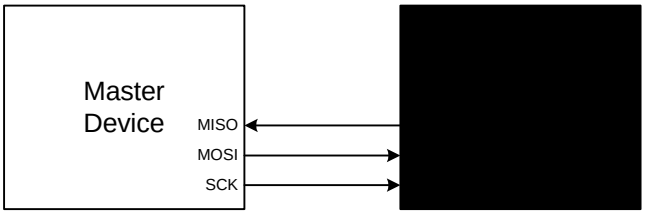

Figure 20.3. 3-Wire Single Master and Slave Mode Connection Diagram

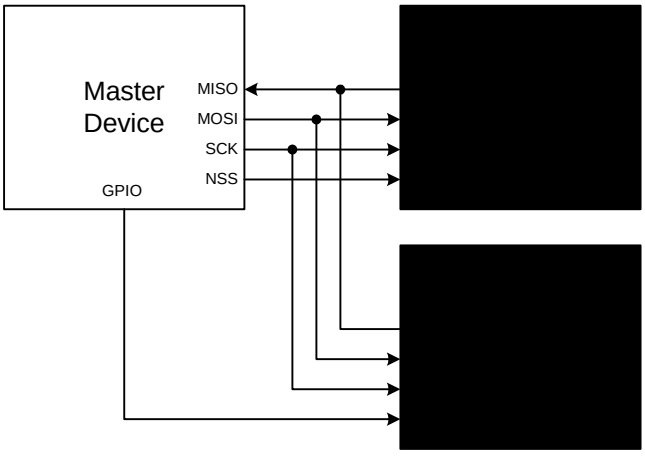

Figure 20.4. 4-Wire Single Master and Slave Mode Connection Diagram

Table 20.1. SPI Slave Timing Parameters

Parameter	Description	Min	Max	Units
Master Mode Timing* (See Figure 20.8 and Figure 20.9)				
T_{MCKH}	SCK High Time	1 x T_{SYSCLK}		ns
T_{MCKL}	SCK Low Time	1 x T_{SYSCLK}		ns
T_{MIS}	MISO Valid to SCK Shift Edge	1 x T_{SYSCLK} + 20		ns
T_{MIH}	SCK Shift Edge to MISO Change	0		ns
Slave Mode Timing* (See Figure 20.10 and Figure 20.11)				
T_{SE}	NSS Falling to First SCK Edge	2 x T_{SYSCLK}		ns
T_{SD}	Last SCK Edge to NSS Rising	2 x T_{SYSCLK}		ns
T_{SEZ}	NSS Falling to MISO Valid		4 x T_{SYSCLK}	ns
T_{SDZ}	NSS Rising to MISO High-Z		4 x T_{SYSCLK}	ns
T_{CKH}	SCK High Time	5 x T_{SYSCLK}		ns
T_{CKL}	SCK Low Time	5 x T_{SYSCLK}		ns
T_{SIS}	MOSI Valid to SCK Sample Edge	2 x T_{SYSCLK}		ns
T_{SIH}	SCK Sample Edge to MOSI Change	2 x T_{SYSCLK}		ns
T_{SOH}	SCK Shift Edge to MISO Change		4 x T_{SYSCLK}	ns
T_{SLH}	Last SCK Edge to MISO Change (CKPHA = 1 ONLY)	6 x T_{SYSCLK}	8 x T_{SYSCLK}	ns

***Note:** T_{SYSCLK} is equal to one period of the device system clock (SYSCLK).

21.1.2. Mode 1: 8-Bit UART, Variable Baud Rate

Mode 1 provides standard asynchronous, full duplex communication using a total of 10 bits per data byte: one start bit, eight data bits (LSB first), and one stop bit. Data are transmitted from the TX0 pin and received at the RX0 pin. On receive, the eight data bits are stored in SBUF0 and the stop bit goes into RB80 (SCON0.2).

Data transmission begins when an instruction writes a data byte to the SBUF0 register. The TI0 Transmit Interrupt Flag (SCON0.1) is set at the end of the transmission (the beginning of the stop-bit time). Data reception can begin any time after the REN0 Receive Enable bit (SCON0.4) is set to logic 1. After the stop bit is received, the data byte will be loaded into the SBUF0 receive register if the following conditions are met: RI0 must be logic 0, and if SM20 is logic 1, the stop bit must be logic 1.

If these conditions are met, the eight bits of data is stored in SBUF0, the stop bit is stored in RB80 and the RI0 flag is set. If these conditions are not met, SBUF0 and RB80 will not be loaded and the RI0 flag will not be set. An interrupt will occur if enabled when either TI0 or RI0 are set.

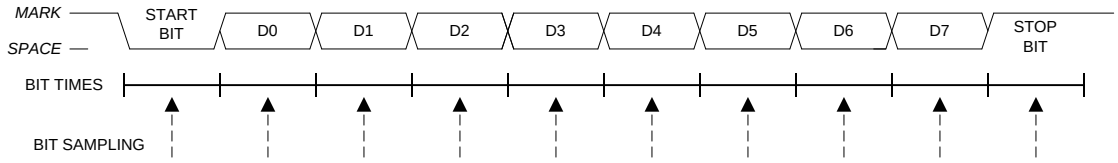

Figure 21.4. UART0 Mode 1 Timing Diagram

The baud rate generated in Mode 1 is a function of timer overflow. UART0 can use Timer 1 operating in *8-Bit Auto-Reload Mode*, or Timer 2, 3, or 4 operating in *Auto-reload Mode* to generate the baud rate (note that the TX and RX clocks are selected separately). On each timer overflow event (a rollover from all ones - (0xFF for Timer 1, 0xFFFF for Timer 2, 3, or 4) - to zero) a clock is sent to the baud rate logic.

Timers 1, 2, 3, or 4 are selected as the baud rate source with bits in the SSTA0 register (see SFR Definition 21.2). The transmit baud rate clock is selected using the S0TCLK1 and S0TCLK0 bits, and the receive baud rate clock is selected using the S0RCLK1 and S0RCLK0 bits.

When Timer 1 is selected as a baud rate source, the SMOD0 bit (SSTA0.4) selects whether or not to divide the Timer 1 overflow rate by two. On reset, the SMOD0 bit is logic 0, thus selecting the lower speed baud rate by default. The SMOD0 bit affects the baud rate generated by Timer 1 as shown in Equation 21.1.

The Mode 1 baud rate equations are shown below, where T1M is bit4 of register CKCON, TH1 is the 8-bit reload register for Timer 1, and [RCAPnH , RCAPnL] is the 16-bit reload register for Timer 2, 3, or 4.

Equation 21.1. Mode 1 Baud Rate using Timer 1

When SMOD0 = 0:

$$\text{Mode1\_BaudRate} = 1/32 \cdot \text{Timer1\_OverflowRate}$$

When SMOD0 = 1:

$$\text{Mode1\_BaudRate} = 1/16 \cdot \text{Timer1\_OverflowRate}$$

24.3. Register Descriptions for PCA0

Following are detailed descriptions of the special function registers related to the operation of PCA0.

SFR Definition 24.1. PCA0CN: PCA Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
CF	CR	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xD8
SFR Page: 0

Bit7: CF: PCA Counter/Timer Overflow Flag.
Set by hardware when the PCA0 Counter/Timer overflows from 0xFFFF to 0x0000. When the Counter/Timer Overflow (CF) interrupt is enabled, setting this bit causes the CPU to vector to the CF interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.

Bit6: CR: PCA0 Counter/Timer Run Control.
This bit enables/disables the PCA0 Counter/Timer.
0: PCA0 Counter/Timer disabled.
1: PCA0 Counter/Timer enabled.

Bit5: CCF5: PCA0 Module 5 Capture/Compare Flag.
This bit is set by hardware when a match or capture occurs. When the CCF interrupt is enabled, setting this bit causes the CPU to vector to the CCF interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.

Bit4: CCF4: PCA0 Module 4 Capture/Compare Flag.
This bit is set by hardware when a match or capture occurs. When the CCF interrupt is enabled, setting this bit causes the CPU to vector to the CCF interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.

Bit3: CCF3: PCA0 Module 3 Capture/Compare Flag.
This bit is set by hardware when a match or capture occurs. When the CCF interrupt is enabled, setting this bit causes the CPU to vector to the CCF interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.

Bit2: CCF2: PCA0 Module 2 Capture/Compare Flag.
This bit is set by hardware when a match or capture occurs. When the CCF interrupt is enabled, setting this bit causes the CPU to vector to the CCF interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.

Bit1: CCF1: PCA0 Module 1 Capture/Compare Flag.
This bit is set by hardware when a match or capture occurs. When the CCF interrupt is enabled, setting this bit causes the CPU to vector to the CCF interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.

Bit0: CCF0: PCA0 Module 0 Capture/Compare Flag.
This bit is set by hardware when a match or capture occurs. When the CCF interrupt is enabled, setting this bit causes the CPU to vector to the CCF interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.

DOCUMENT CHANGE LIST

Revision 1.3 to Revision 1.4

- Added new paragraph tags: SFR Definition and JTAG Register Definition.
- Product Selection Guide Table 1.1: Added RoHS-compliant ordering information.
- Overview Chapter, Figure 1.8, “On-Chip Memory Map”: Corrected on-chip XRAM size to “8192 Bytes”.
- SAR8 Chapter: Table 7.1, “ADC2 Electrical Characteristics”: Track/Hold minimum spec corrected to “300 ns”.
- SAR8 Chapter: Table 7.1, “ADC2 Electrical Characteristics”: Total Harmonic Distortion typical spec corrected to “-51 dB”.
- Oscillators Chapter, Figure 14.1, “Oscillator Diagram”: Corrected location of IOSCEN arrow.
- CIP51 Chapter, **Section 11.3**: Added note describing EA change behavior when followed by single-cycle instruction.
- CIP51 Chapter, Interrupt Summary Table: Added “SFRPAGE” column and SFRPAGE value for each interrupt source.
- CIP-51 Chapter, Figure 11.2, “Memory Map”: Corrected on-chip XRAM size to “8192 Bytes”.
- Port I/O Chapter, Crossbar Priority Figures: Character formatting problem corrected.
- Port I/O Chapter, P7MDOUT Register Description: Removed references to UART and SMBus peripherals.
- Port I/O Chapter, P3MDOUT Register Description: Corrected text to read “P3MDOUT.[7:0]”.
- Timers Chapter: References to “TnCON” corrected to read “TMRnCN”.
- PCA0 Chapter, Section 24.1: Added note about PCA0CN Register and effects of read-modify-write instructions on the CF bit.