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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, SMBus (2-Wire/I ² C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	64
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x8b, 8x10b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f126-gq

C8051F120/1/2/3/4/5/6/7 C8051F130/1/2/3

1. System Overview

The C8051F12x and C8051F13x device families are fully integrated mixed-signal System-on-a-Chip MCUs with 64 digital I/O pins (100-pin TQFP) or 32 digital I/O pins (64-pin TQFP).

Highlighted features are listed below. Refer to Table 1.1 for specific product feature selection.

- High-Speed pipelined 8051-compatible CIP-51 microcontroller core (100 MIPS or 50 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- True 12 or 10-bit 100 ksps ADC with PGA and 8-channel analog multiplexer
- True 8-bit 500 ksps ADC with PGA and 8-channel analog multiplexer (C8051F12x Family)
- Two 12-bit DACs with programmable update scheduling (C8051F12x Family)
- 2-cycle 16 by 16 Multiply and Accumulate Engine (C8051F120/1/2/3 and C8051F130/1/2/3)
- 128 or 64 kB of in-system programmable Flash memory
- 8448 (8 k + 256) bytes of on-chip RAM
- External Data Memory Interface with 64 kB address space
- SPI, SMBus/I2C, and (2) UART serial interfaces implemented in hardware
- Five general purpose 16-bit Timers
- Programmable Counter/Timer Array with 6 capture/compare modules
- On-chip Watchdog Timer, V_{DD} Monitor, and Temperature Sensor

With on-chip V_{DD} monitor, Watchdog Timer, and clock oscillator, the C8051F12x and C8051F13x devices are truly stand-alone System-on-a-Chip solutions. All analog and digital peripherals are enabled/disabled and configured by user firmware. The Flash memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware.

On-board JTAG debug circuitry allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug system supports inspection and modification of memory and registers, setting breakpoints, watchpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using JTAG.

Each MCU is specified for operation over the industrial temperature range (-45 to $+85$ °C). The Port I/O, RST, and JTAG pins are tolerant for input signals up to 5 V. The devices are available in 100-pin TQFP or 64-pin TQFP packaging. Table 1.1 lists the specific device features and package offerings for each part number. Figure 1.1 through Figure 1.6 show functional block diagrams for each device.

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1.1.3. Additional Features

Several key enhancements are implemented in the CIP-51 core and peripherals to improve overall performance and ease of use in end applications.

The extended interrupt handler provides 20 interrupt sources into the CIP-51 (as opposed to 7 for the standard 8051), allowing the numerous analog and digital peripherals to interrupt the controller. An interrupt driven system requires less intervention by the MCU, giving it more effective throughput. The extra interrupt sources are very useful when building multi-tasking, real-time systems.

There are up to seven reset sources for the MCU: an on-board V_{DD} monitor, a Watchdog Timer, a missing clock detector, a voltage level detection from Comparator0, a forced software reset, the CNVSTR0 input pin, and the RST pin. The RST pin is bi-directional, accommodating an external reset, or allowing the internally generated POR to be output on the RST pin. Each reset source except for the V_{DD} monitor and Reset Input pin may be disabled by the user in software; the V_{DD} monitor is enabled/disabled via the MONEN pin. The Watchdog Timer may be permanently enabled in software after a power-on reset during MCU initialization.

The MCU has an internal, stand alone clock generator which is used by default as the system clock after any reset. If desired, the clock source may be switched on the fly to the external oscillator, which can use a crystal, ceramic resonator, capacitor, RC, or external clock source to generate the system clock. This can be extremely useful in low power applications, allowing the MCU to run from a slow (power saving) external crystal source, while periodically switching to the 24.5 MHz internal oscillator as needed. Additionally, an on-chip PLL is provided to achieve higher system clock speeds for increased throughput.

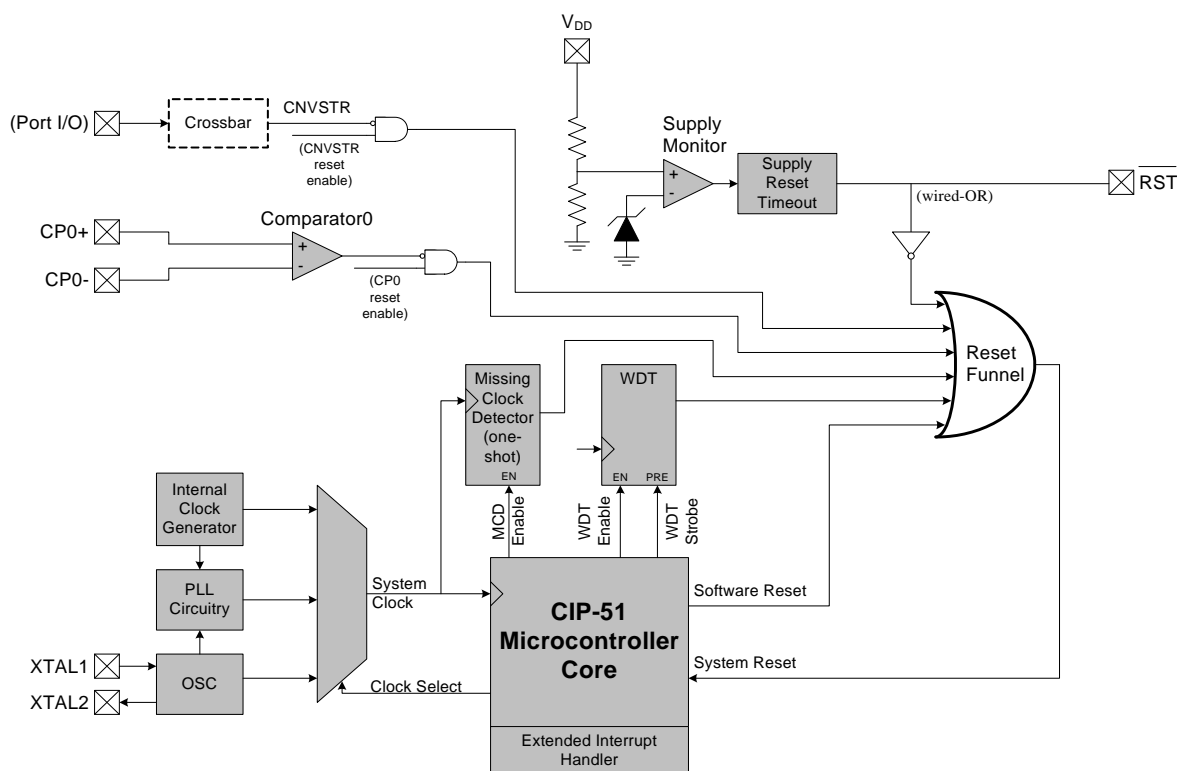


Figure 1.7. On-Board Clock and Reset

1.6. Programmable Counter Array

An on-board Programmable Counter/Timer Array (PCA) is included in addition to the five 16-bit general purpose counter/timers. The PCA consists of a dedicated 16-bit counter/timer time base with 6 programmable capture/compare modules. The timebase is clocked from one of six sources: the system clock divided by 12, the system clock divided by 4, Timer 0 overflow, an External Clock Input (ECI pin), the system clock, or the external oscillator source divided by 8.

Each capture/compare module can be configured to operate in one of six modes: Edge-Triggered Capture, Software Timer, High Speed Output, Frequency Output, 8-Bit Pulse Width Modulator, or 16-Bit Pulse Width Modulator. The PCA Capture/Compare Module I/O and External Clock Input are routed to the MCU Port I/O via the Digital Crossbar.

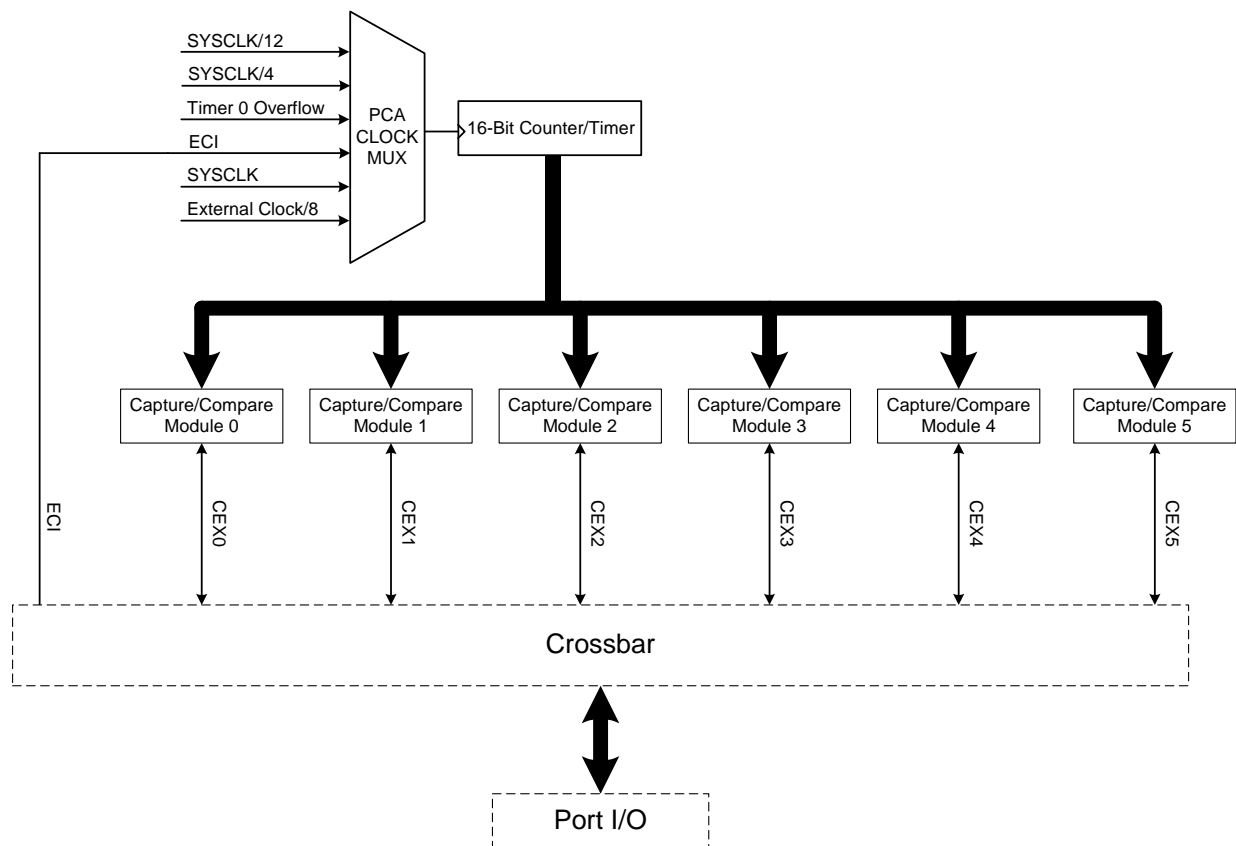


Figure 1.12. PCA Block Diagram

1.7. Serial Ports

Serial peripherals included on the devices are two Enhanced Full-Duplex UARTs, SPI Bus, and SMBus/I2C. Each of the serial buses is fully implemented in hardware and makes extensive use of the CIP-51's interrupts, thus requiring very little intervention by the CPU. The serial buses do not "share" resources such as timers, interrupts, or Port I/O, so any or all of the serial buses may be used together with any other.

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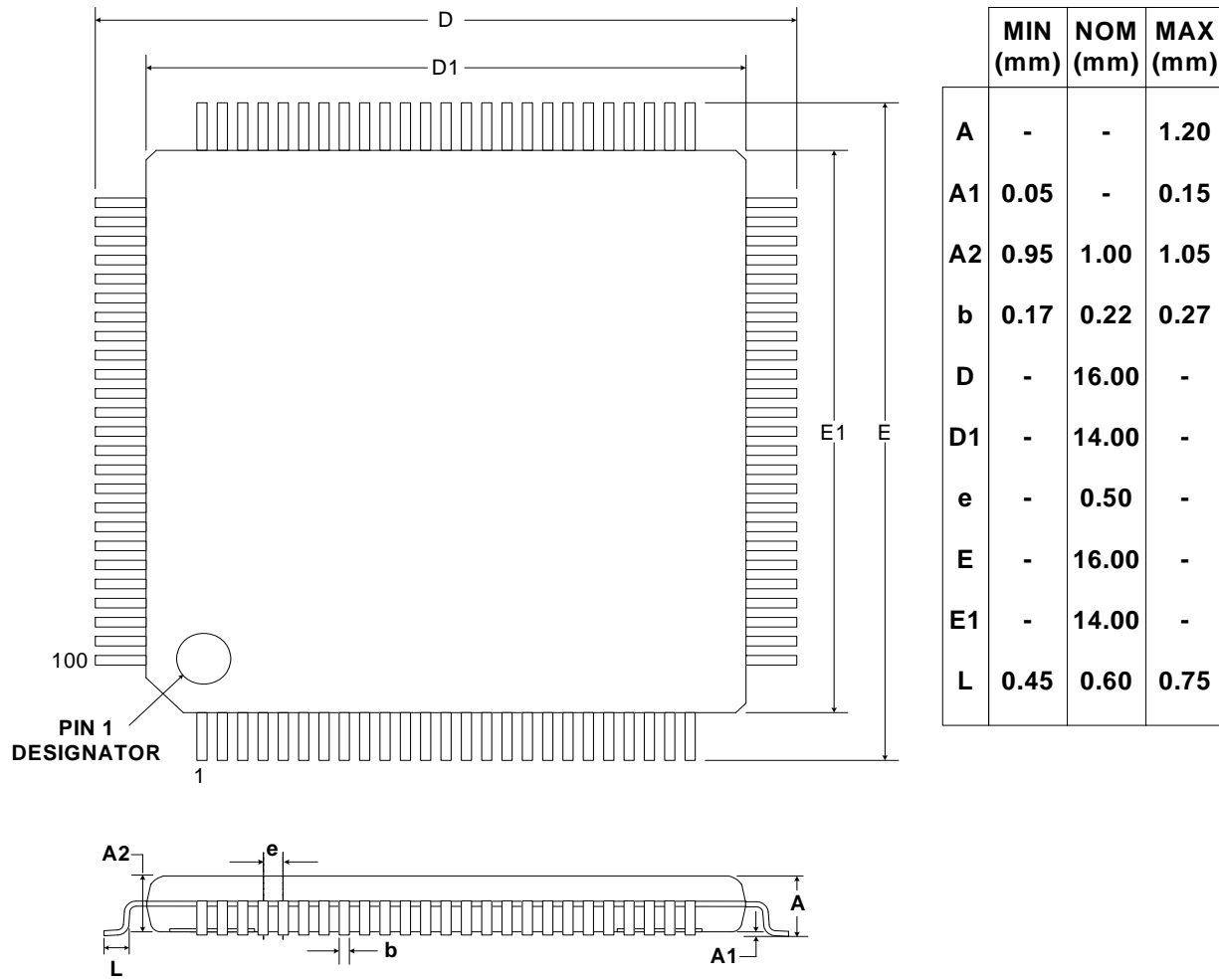


Figure 4.3. TQFP-100 Package Drawing

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SFR Definition 5.3. ADC0CF: ADC0 Configuration

SFR Page: 0
SFR Address: 0xBC

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
AD0SC4	AD0SC3	AD0SC2	AD0SC1	AD0SC0	AMP0GN2	AMP0GN1	AMP0GN0	11111000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits7–3: AD0SC4–0: ADC0 SAR Conversion Clock Period Bits.
The SAR Conversion clock is derived from system clock by the following equation, where *AD0SC* refers to the 5-bit value held in AD0SC4-0, and CLK_{SAR0} refers to the desired ADC0 SAR clock (Note: the ADC0 SAR Conversion Clock should be less than or equal to 2.5 MHz).

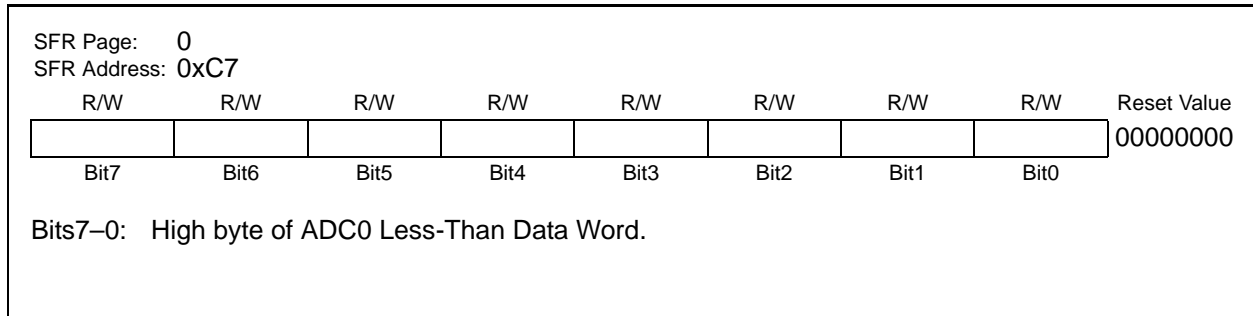
$$AD0SC = \frac{SYSCLK}{2 \times CLK_{SAR0}} - 1 \quad (AD0SC > 00000b)$$

When the AD0SC bits are equal to 00000b, the SAR Conversion clock is equal to SYSCLK to facilitate faster ADC conversions at slower SYSCLK speeds.

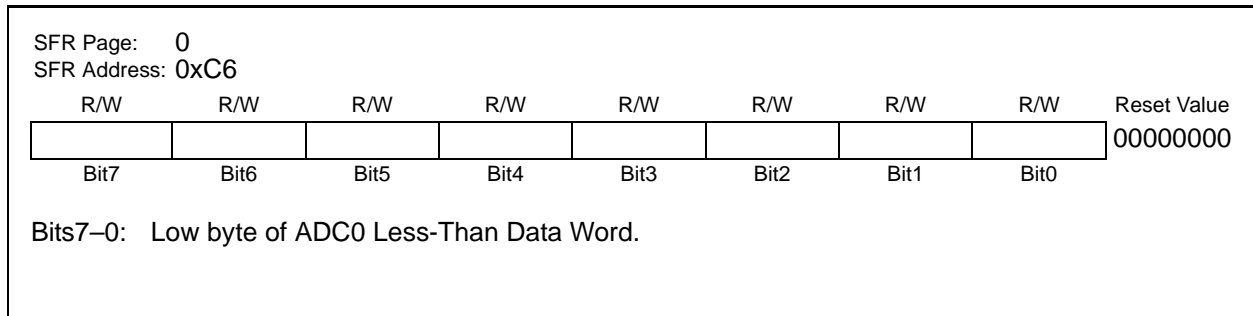
Bits2–0: AMP0GN2–0: ADC0 Internal Amplifier Gain (PGA).
000: Gain = 1
001: Gain = 2
010: Gain = 4
011: Gain = 8
10x: Gain = 16
11x: Gain = 0.5

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SFR Definition 5.9. ADC0LTH: ADC0 Less-Than Data High Byte



SFR Definition 5.10. ADC0LTL: ADC0 Less-Than Data Low Byte



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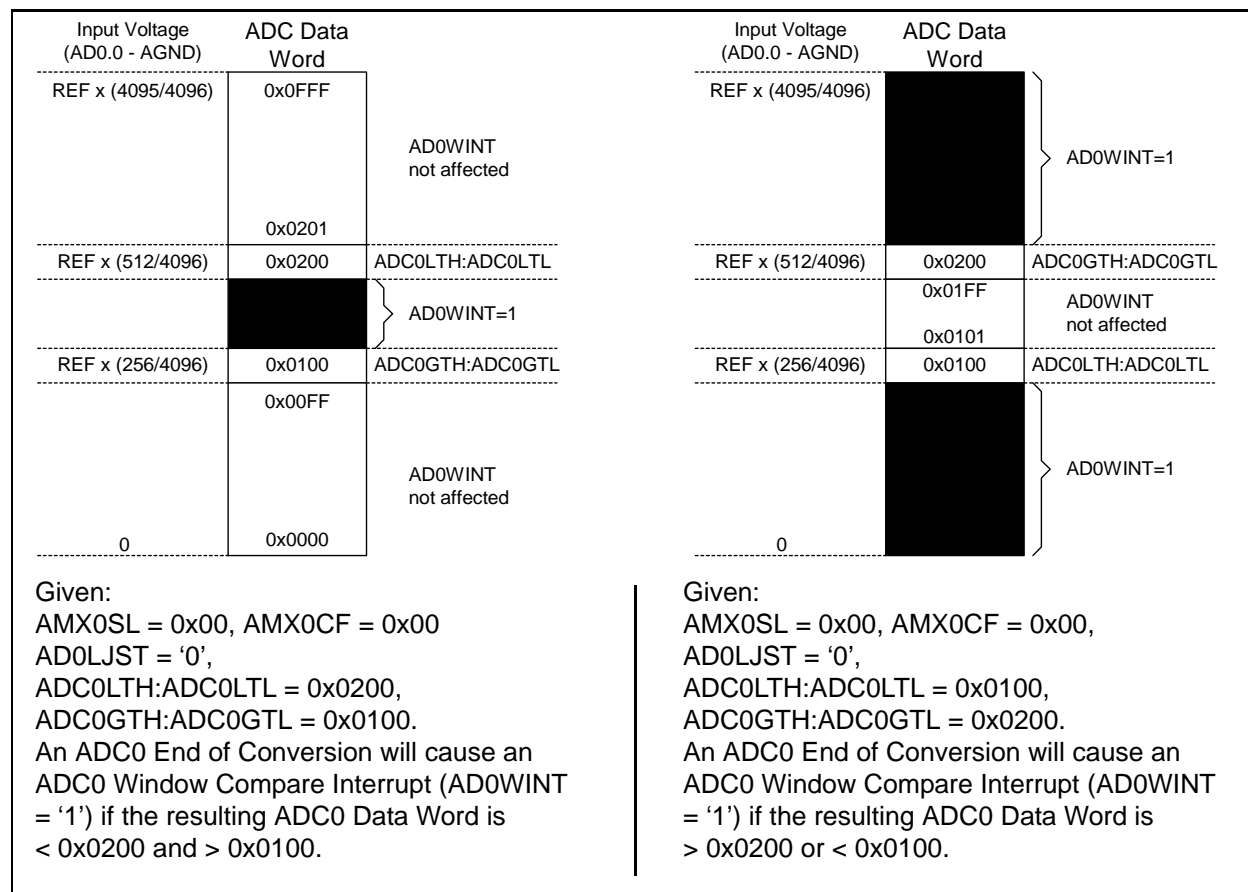


Figure 5.6. 12-Bit ADC0 Window Interrupt Example: Right Justified Single-Ended Data

9. Voltage Reference

The voltage reference options available on the C8051F12x and C8051F13x device families vary according to the device capabilities.

All devices include an internal voltage reference circuit, consisting of a 1.2 V, 15 ppm/°C (typical) bandgap voltage reference generator and a gain-of-two output buffer amplifier. The internal reference may be routed via the VREF pin to external system components or to the voltage reference input pins. The maximum load seen by the VREF pin must be less than 200 μ A to AGND. Bypass capacitors of 0.1 μ F and 4.7 μ F are recommended from the VREF pin to AGND.

The Reference Control Register, REF0CN enables/disables the internal reference generator and the internal temperature sensor on all devices. The BIASE bit in REF0CN enables the on-board reference generator while the REFBE bit enables the gain-of-two buffer amplifier which drives the VREF pin. When disabled, the supply current drawn by the bandgap and buffer amplifier falls to less than 1 μ A (typical) and the output of the buffer amplifier enters a high impedance state. If the internal bandgap is used as the reference voltage generator, BIASE and REFBE must both be set to logic 1. If the internal reference is not used, REFBE may be set to logic 0. Note that the BIASE bit must be set to logic 1 if any DACs or ADCs are used, regardless of whether the voltage reference is derived from the on-chip reference or supplied by an off-chip source. If no ADCs or DACs are being used, both of these bits can be set to logic 0 to conserve power.

When enabled, the temperature sensor connects to the highest order input of the ADC0 input multiplexer. The TEMPE bit within REF0CN enables and disables the temperature sensor. While disabled, the temperature sensor defaults to a high impedance state. Any ADC measurements performed on the sensor while disabled will result in undefined data.

The electrical specifications for the internal voltage reference are given in Table 9.1.

9.1. Reference Configuration on the C8051F120/2/4/6

On the C8051F120/2/4/6 devices, the REF0CN register also allows selection of the voltage reference source for ADC0 and ADC2, as shown in SFR Definition 9.1. Bits AD0VRS and AD2VRS in the REF0CN register select the ADC0 and ADC2 voltage reference sources, respectively. Three voltage reference input pins allow each ADC and the two DACs to reference an external voltage reference or the on-chip voltage reference output (with an external connection). ADC0 may also reference the DAC0 output internally, and ADC2 may reference the analog power supply voltage, via the VREF multiplexers shown in Figure 9.1.

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SFR Definition 9.2. REF0CN: Reference Control (C8051F121/3/5/7)

SFR Page: 0
SFR Address: 0xD1

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	AD0VRS	AD2VRS	TEMPE	BIASE	REFBE	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits7–5: UNUSED. Read = 000b; Write = don't care.

Bit4: AD0VRS: ADC0 Voltage Reference Select.
0: ADC0 voltage reference from VREFA pin.
1: ADC0 voltage reference from DAC0 output.

Bit3: AD2VRS: ADC2 Voltage Reference Select.
0: ADC2 voltage reference from VREFA pin.
1: ADC2 voltage reference from AV+.

Bit2: TEMPE: Temperature Sensor Enable Bit.
0: Internal Temperature Sensor Off.
1: Internal Temperature Sensor On.

Bit1: BIASE: ADC/DAC Bias Generator Enable Bit. (Must be '1' if using ADC, DAC, or VREF).
0: Internal Bias Generator Off.
1: Internal Bias Generator On.

Bit0: REFBE: Internal Reference Buffer Enable Bit.
0: Internal Reference Buffer Off.
1: Internal Reference Buffer On. Internal voltage reference is driven on the VREF pin.

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Table 11.1. CIP-51 Instruction Set Summary (Continued)

Mnemonic	Description	Bytes	Clock Cycles
DEC A	Decrement A	1	1
DEC Rn	Decrement register	1	1
DEC direct	Decrement direct byte	2	2
DEC @Ri	Decrement indirect RAM	1	2
INC DPTR	Increment Data Pointer	1	1
MUL AB	Multiply A and B	1	4
DIV AB	Divide A by B	1	8
DA A	Decimal adjust A	1	1
Logical Operations			
ANL A, Rn	AND Register to A	1	1
ANL A, direct	AND direct byte to A	2	2
ANL A, @Ri	AND indirect RAM to A	1	2
ANL A, #data	AND immediate to A	2	2
ANL direct, A	AND A to direct byte	2	2
ANL direct, #data	AND immediate to direct byte	3	3
ORL A, Rn	OR Register to A	1	1
ORL A, direct	OR direct byte to A	2	2
ORL A, @Ri	OR indirect RAM to A	1	2
ORL A, #data	OR immediate to A	2	2
ORL direct, A	OR A to direct byte	2	2
ORL direct, #data	OR immediate to direct byte	3	3
XRL A, Rn	Exclusive-OR Register to A	1	1
XRL A, direct	Exclusive-OR direct byte to A	2	2
XRL A, @Ri	Exclusive-OR indirect RAM to A	1	2
XRL A, #data	Exclusive-OR immediate to A	2	2
XRL direct, A	Exclusive-OR A to direct byte	2	2
XRL direct, #data	Exclusive-OR immediate to direct byte	3	3
CLR A	Clear A	1	1
CPL A	Complement A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through Carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through Carry	1	1
SWAP A	Swap nibbles of A	1	1
Data Transfer			
MOV A, Rn	Move Register to A	1	1
MOV A, direct	Move direct byte to A	2	2
MOV A, @Ri	Move indirect RAM to A	1	2
MOV A, #data	Move immediate to A	2	2
MOV Rn, A	Move A to Register	1	1
MOV Rn, direct	Move direct byte to Register	2	2
MOV Rn, #data	Move immediate to Register	2	2
MOV direct, A	Move A to direct byte	2	2
MOV direct, Rn	Move Register to direct byte	2	2
MOV direct, direct	Move direct byte to direct byte	3	3

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SFR Definition 17.2. EMI0CF: External Memory Configuration

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	PRTSEL	EMD2	EMD1	EMD0	EALE1	EALE0	00000011
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xA3
SFR Page: 0

- Bits7–6: Unused. Read = 00b. Write = don't care.
- Bit5: PRTSEL: EMIF Port Select.
0: EMIF active on P0–P3.
1: EMIF active on P4–P7.
- Bit4: EMD2: EMIF Multiplex Mode Select.
0: EMIF operates in multiplexed address/data mode.
1: EMIF operates in non-multiplexed mode (separate address and data pins).
- Bits3–2: EMD1-0: EMIF Operating Mode Select.
These bits control the operating mode of the External Memory Interface.
00: Internal Only: MOVX accesses on-chip XRAM only. All effective addresses alias to on-chip memory space.
01: Split Mode without Bank Select: Accesses below the 8 k boundary are directed on-chip. Accesses above the 8 k boundary are directed off-chip. 8-bit off-chip MOVX operations use the current contents of the Address High port latches to resolve upper address byte. Note that in order to access off-chip space, EMI0CN must be set to a page that is not contained in the on-chip address space.
10: Split Mode with Bank Select: Accesses below the 8 k boundary are directed on-chip. Accesses above the 8k boundary are directed off-chip. 8-bit off-chip MOVX operations use the contents of EMI0CN to determine the high-byte of the address.
11: External Only: MOVX accesses off-chip XRAM only. On-chip XRAM is not visible to the CPU.
- Bits1–0: EALE1–0: ALE Pulse-Width Select Bits (only has effect when EMD2 = 0).
00: ALE high and ALE low pulse width = 1 SYSCLK cycle.
01: ALE high and ALE low pulse width = 2 SYSCLK cycles.
10: ALE high and ALE low pulse width = 3 SYSCLK cycles.
11: ALE high and ALE low pulse width = 4 SYSCLK cycles.

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Table 21.2. Oscillator Frequencies for Standard Baud Rates

System Clock Frequency (MHz)	Divide Factor	Timer 1 Reload Value ¹	Timer 2, 3, or 4 Reload Value	Resulting Baud Rate (Hz) ²
100.0	864	0xCA	0xFFCA	115200 (115741)
99.5328	864	0xCA	0xFFCA	115200
50.0	432	0xE5	0xFFE5	115200 (115741)
49.7664	432	0xE5	0xFFE5	115200
24.0	208	0xF3	0xFFF3	115200 (115384)
22.1184	192	0xF4	0xFFF4	115200
18.432	160	0xF6	0xFFF6	115200
11.0592	96	0xFA	0xFFFA	115200
3.6864	32	0xFE	0xFFFFE	115200
1.8432	16	0xFF	0xFFFFF	115200
100.0	3472	0x27	0xFF27	28800 (28802)
99.5328	3456	0x28	0xFF28	28800
50.0	1744	0x93	0xFF93	28800 (28670)
49.7664	1728	0x94	0xFF94	28800
24.0	832	0xCC	0xFFCC	28800 (28846)
22.1184	768	0xD0	0xFFD0	28800
18.432	640	0xD8	0xFFD8	28800
11.0592	348	0xE8	0xFFE8	28800
3.6864	128	0xF8	0xFFFF8	28800
1.8432	64	0xFC	0xFFFFC	28800
100.0	10416	-	0xFD75	9600 (9601)
99.5328	10368	-	0xFD78	9600
50.0	5216	-	0xFEBA	9600 (9586)
49.7664	5184	-	0xFEBC	9600
24.0	2496	0x64	0xFF64	9600 (9615)
22.1184	2304	0x70	0xFF70	9600
18.432	1920	0x88	0xFF88	9600
11.0592	1152	0xB8	0xFFB8	9600
3.6864	384	0xE8	0xFFE8	9600
1.8432	192	0xF4	0xFFFF4	9600

Notes:

1. Assumes SMOD0 = 1 and T1M = 1.
2. Numbers in parenthesis show the actual baud rate.

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22.2.2. 9-Bit UART

9-bit UART mode uses a total of eleven bits per data byte: a start bit, 8 data bits (LSB first), a programmable ninth data bit, and a stop bit. The state of the ninth transmit data bit is determined by the value in TB81 (SCON1.3), which is assigned by user software. It can be assigned the value of the parity flag (bit P in register PSW) for error detection, or used in multiprocessor communications. On receive, the ninth data bit goes into RB81 (SCON1.2) and the stop bit is ignored.

Data transmission begins when an instruction writes a data byte to the SBUF1 register. The TI1 Transmit Interrupt Flag (SCON1.1) is set at the end of the transmission (the beginning of the stop-bit time). Data reception can begin any time after the REN1 Receive Enable bit (SCON1.4) is set to '1'. After the stop bit is received, the data byte will be loaded into the SBUF1 receive register if the following conditions are met: (1) RI1 must be logic 0, and (2) if MCE1 is logic 1, the 9th bit must be logic 1 (when MCE1 is logic 0, the state of the ninth data bit is unimportant). If these conditions are met, the eight bits of data are stored in SBUF1, the ninth bit is stored in RB81, and the RI1 flag is set to '1'. If the above conditions are not met, SBUF1 and RB81 will not be loaded and the RI1 flag will not be set to '1'. A UART1 interrupt will occur if enabled when either TI1 or RI1 is set to '1'.

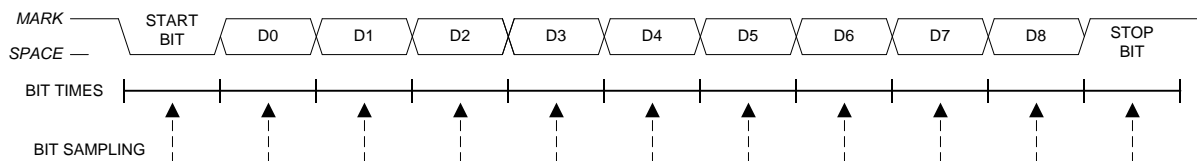


Figure 22.5. 9-Bit UART Timing Diagram

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23.1.2. Mode 1: 16-bit Counter/Timer

Mode 1 operation is the same as Mode 0, except that the counter/timer registers use all 16 bits. The counter/timers are enabled and configured in Mode 1 in the same manner as for Mode 0.

23.1.3. Mode 2: 8-bit Counter/Timer with Auto-Reload

Mode 2 configures Timer 0 or Timer 1 to operate as 8-bit counter/timers with automatic reload of the start value. TL0 holds the count and TH0 holds the reload value. When the counter in TL0 overflows from 0xFF to 0x00, the timer overflow flag TF0 (TCON.5) is set and the counter in TL0 is reloaded from TH0. If Timer 0 interrupts are enabled, an interrupt will occur when the TF0 flag is set. The reload value in TH0 is not changed. TL0 must be initialized to the desired value before enabling the timer for the first count to be correct. When in Mode 2, Timer 1 operates identically to Timer 0.

Both counter/timers are enabled and configured in Mode 2 in the same manner as Mode 0. Setting the TR0 bit (TCON.4) enables the timer when either GATE0 (TMOD.3) is logic 0 or when the input signal /INT0 is low

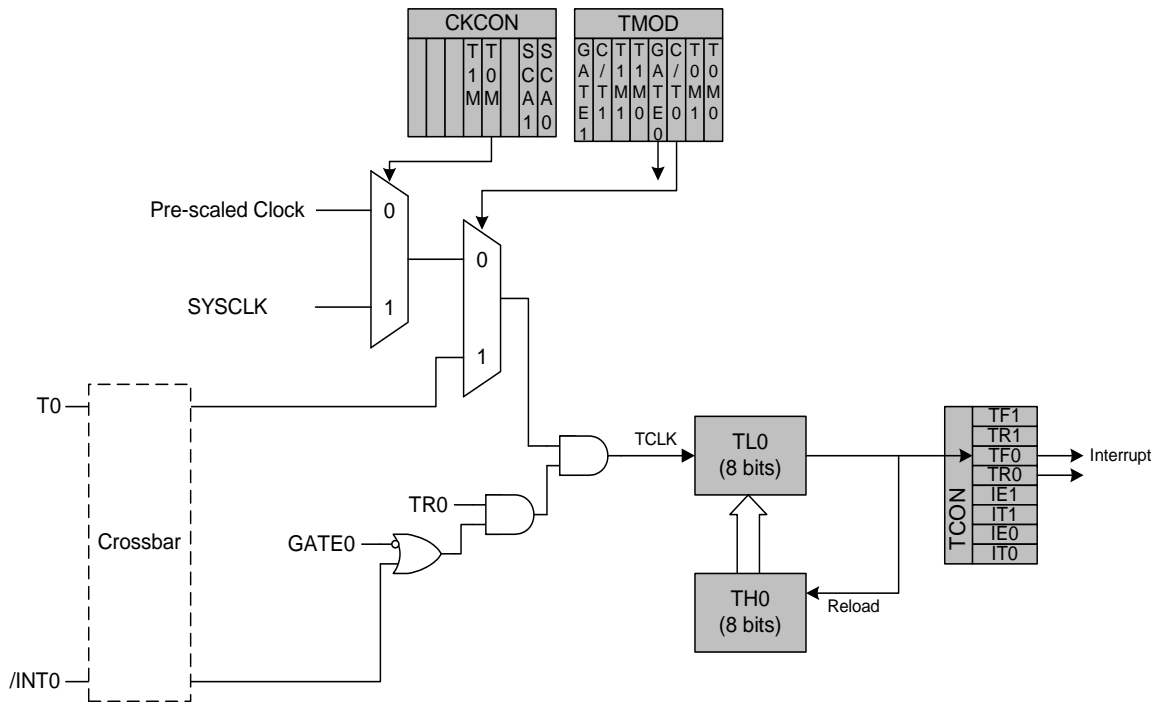


Figure 23.2. T0 Mode 2 Block Diagram

23.2. Timer 2, Timer 3, and Timer 4

Timers 2, 3, and 4 are 16-bit counter/timers, each formed by two 8-bit SFR's: TMRnL (low byte) and TMRnH (high byte) where $n = 2, 3,$ and 4 for timers 2, 3, and 4 respectively. Timers 2 and 4 feature auto-reload, capture, and toggle output modes with the ability to count up or down. Timer 3 features auto-reload and capture modes, with the ability to count up or down. Capture Mode and Auto-reload mode are selected using bits in the Timer 2, 3, and 4 Control registers (TMRnCN). Toggle output mode is selected using the Timer 2 or 4 Configuration registers (TMRnCF). These timers may also be used to generate a square-wave at an external pin. As with Timers 0 and 1, Timers 2, 3, and 4 can use either the system clock (divided by one, two, or twelve), external clock (divided by eight) or transitions on an external input pin as its clock source. Timer 2 and 3 can be used to start an ADC Data Conversion and Timers 2, 3, and 4 can schedule DAC outputs. Timers 1, 2, 3, or 4 may be used to generate baud rates for UART 0. Only Timer 1 can be used to generate baud rates for UART 1.

The Counter/Timer Select bit C/Tn bit (TMRnCN.1) configures the peripheral as a counter or timer. Clearing C/Tn configures the Timer to be in a timer mode (i.e., the system clock or transitions on an external pin as the input for the timer). When C/Tn is set to 1, the timer is configured as a counter (i.e., high-to-low transitions at the Tn input pin increment (or decrement) the counter/timer register. Timer 3 and Timer 2 share the T2 input pin. Refer to **Section “18.1. Ports 0 through 3 and the Priority Crossbar Decoder” on page 238** for information on selecting and configuring external I/O pins for digital peripherals, such as the Tn pin.

Timer 2, 3, and 4 can use either SYSCLK, SYSCLK divided by 2, SYSCLK divided by 12, an external clock divided by 8, or high-to-low transitions on the Tn input pin as its clock source when operating in Counter/Timer with Capture mode. Clearing the C/Tn bit (TMRnCN.1) selects the system clock/external clock as the input for the timer. The Timer Clock Select bits TnM0 and TnM1 in TMRnCF can be used to select the system clock undivided, system clock divided by two, system clock divided by 12, or an external clock provided at the XTAL1/XTAL2 pins divided by 8 (see SFR Definition 23.13). When C/Tn is set to logic 1, a high-to-low transition at the Tn input pin increments the counter/timer register (i.e., configured as a counter).

23.2.1. Configuring Timer 2, 3, and 4 to Count Down

Timers 2, 3, and 4 have the ability to count down. When the timer's Decrement Enable Bit (DCENn) in the Timer Configuration Register (See SFR Definition 23.13) is set to '1', the timer can then count *up* or *down*. When DCENn = 1, the direction of the timer's count is controlled by the TnEX pin's logic level (Timer 3 shares the T2EX pin with Timer 2). When TnEX = 1, the counter/timer will count up; when TnEX = 0, the counter/timer will count down. To use this feature, TnEX must be enabled in the digital crossbar and configured as a digital input.

Note: When DCENn = 1, other functions of the TnEX input (i.e., capture and auto-reload) are not available. TnEX will only control the direction of the timer when DCENn = 1.

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SFR Definition 23.9. TMRnCF: Timer 2, 3, and 4 Configuration

			R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	TnM1	TnM0	TOGn	TnOE	DCENn	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: TMR2CF:0xC9;TMR3CF:0xC9;TMR4CF:0xC9

SFR Page TMR2CF: page 0;TMR3CF: page 1;TMR4CF: Page 2

Bit7–5: Reserved.

Bit4–3: TnM1 and TnM0: Timer Clock Mode Select Bits.

Bits used to select the Timer clock source. The sources can be the System Clock (SYSCLK), SYSCLK divided by 2 or 12, or the external clock divided by 8. Clock source is selected as follows:

00: SYSCLK/12

01: SYSCLK

10: EXTERNAL CLOCK/8 (Synchronized to the System Clock)

11: SYSCLK/2

Bit2: TOGn: Toggle output state bit.

When timer is used to toggle a port pin, this bit can be used to read the state of the output, or can be written to in order to force the state of the output (Timer 2 and Timer 4 Only).

Bit1: TnOE: Timer output enable bit.

This bit enables the timer to output a 50% duty cycle output to the timer's assigned external port pin.

NOTE: A timer is configured for Square Wave Output as follows:

CP/RLn = 0

C/Tn = 0

TnOE = 1

Load RCAPnH:RCAPnL (See "Square Wave Frequency (Timer 2 and Timer 4 Only)" on page 320.)

Configure Port Pin to output squarewave (See Section "18. Port Input/Output" on page 235)

0: Output of toggle mode not available at Timers's assigned port pin.

1: Output of toggle mode available at Timers's assigned port pin.

Bit0: DCENn: Decrement Enable Bit.

This bit enables the timer to count up or down as determined by the state of TnEX.

0: Timer will count up, regardless of the state of TnEX.

1: Timer will count up or down depending on the state of TnEX as follows:

if TnEX = 0, the timer counts DOWN.

if TnEX = 1, the timer counts UP.

Note: Timer 3 and Timer 2 share the T2 and T2EX pins.

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Table 24.2. PCA0CPM Register Settings for PCA Capture/Compare Modules

PWM16	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	Operation Mode
X	X	1	0	0	0	0	X	Capture triggered by positive edge on CEXn
X	X	0	1	0	0	0	X	Capture triggered by negative edge on CEXn
X	X	1	1	0	0	0	X	Capture triggered by transition on CEXn
X	1	0	0	1	0	0	X	Software Timer
X	1	0	0	1	1	0	X	High Speed Output
X	1	0	0	0	1	1	X	Frequency Output
0	1	0	0	0	0	1	0	8-Bit Pulse Width Modulator
1	1	0	0	0	0	1	0	16-Bit Pulse Width Modulator

X = Don't Care

24.2.1. Edge-triggered Capture Mode

In this mode, a valid transition on the CEXn pin causes PCA0 to capture the value of the PCA0 counter/timer and load it into the corresponding module's 16-bit capture/compare register (PCA0CPLn and PCA0CPHn). The CAPPn and CAPNn bits in the PCA0CPMn register are used to select the type of transition that triggers the capture: low-to-high transition (positive edge), high-to-low transition (negative edge), or either transition (positive or negative edge). When a capture occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1 and an interrupt request is generated if CCF interrupts are enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software.

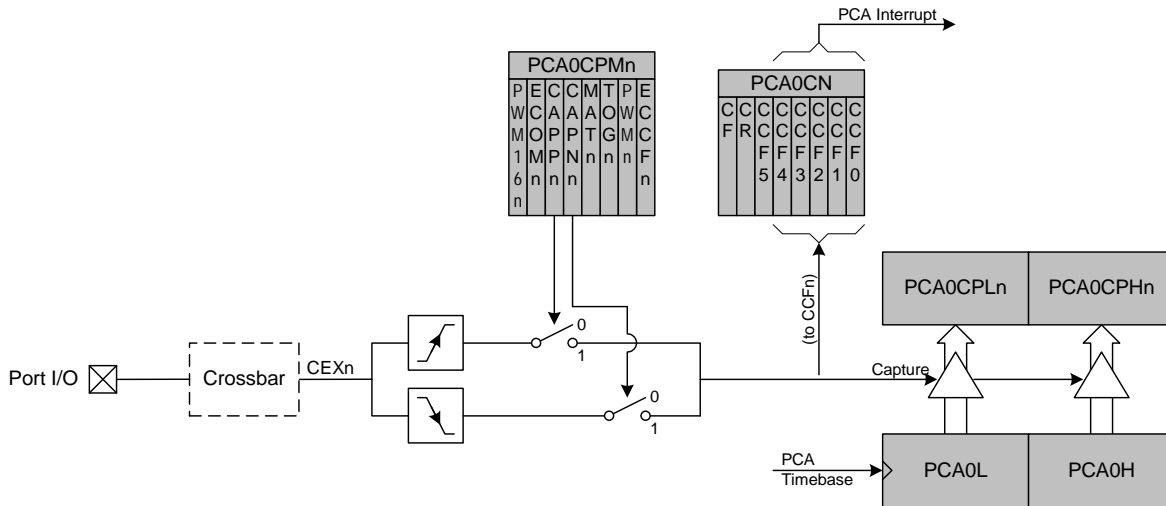


Figure 24.4. PCA Capture Mode Diagram

Note: The signal at CEXn must be high or low for at least 2 system clock cycles in order to be valid.

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24.2.4. Frequency Output Mode

Frequency Output Mode produces a programmable-frequency square wave on the module's associated CEXn pin. The capture/compare module high byte holds the number of PCA clocks to count before the output is toggled. The frequency of the square wave is then defined by Equation 24.1.

Equation 24.1. Square Wave Frequency Output

$$F_{sqr} = \frac{F_{PCA}}{2 \times PCA0CPHn}$$

Note: A value of 0x00 in the PCA0CPHn register is equal to 256 for this equation.

Where F_{PCA} is the frequency of the clock selected by the CPS2–0 bits in the PCA mode register, PCA0MD. The lower byte of the capture/compare module is compared to the PCA0 counter low byte; on a match, CEXn is toggled and the offset held in the high byte is added to the matched value in PCA0CPLn. Frequency Output Mode is enabled by setting the ECOMn, TOGn, and PWMn bits in the PCA0CPMn register.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to '0'; writing to PCA0CPHn sets ECOMn to '1'.

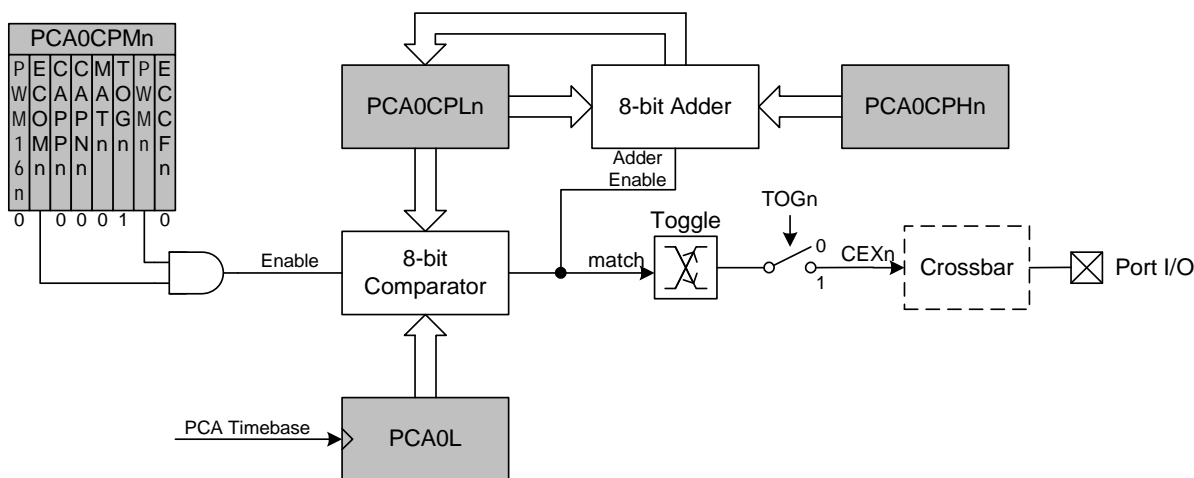


Figure 24.7. PCA Frequency Output Mode

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SFR Definition 24.3. PCA0CPMn: PCA0 Capture/Compare Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
PWM16n	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR PCA0CPM0: 0xDA, PCA0CPM1: 0xDB, PCA0CPM2: 0xDC, PCA0CPM3: 0xDD, PCA0CPM4: 0xDE, Address: PCA0CPM5: 0xDF

SFR Page: PCA0CPM0: page 0, PCA0CPM1: page 0, PCA0CPM2: page 0, PCA0CPM3: 0, PCA0CPM4: page 0, PCA0CPM5: page 0

Bit7: PWM16n: 16-bit Pulse Width Modulation Enable
This bit selects 16-bit mode when Pulse Width Modulation mode is enabled (PWMn = 1).
0: 8-bit PWM selected.
1: 16-bit PWM selected.

Bit6: ECOMn: Comparator Function Enable.
This bit enables/disables the comparator function for PCA0 module n.
0: Disabled.
1: Enabled.

Bit5: CAPPn: Capture Positive Function Enable.
This bit enables/disables the positive edge capture for PCA0 module n.
0: Disabled.
1: Enabled.

Bit4: CAPNn: Capture Negative Function Enable.
This bit enables/disables the negative edge capture for PCA0 module n.
0: Disabled.
1: Enabled.

Bit3: MATn: Match Function Enable.
This bit enables/disables the match function for PCA0 module n. When enabled, matches of the PCA0 counter with a module's capture/compare register cause the CCFn bit in PCA0MD register to be set to logic 1.
0: Disabled.
1: Enabled.

Bit2: TOGn: Toggle Function Enable.
This bit enables/disables the toggle function for PCA0 module n. When enabled, matches of the PCA0 counter with a module's capture/compare register cause the logic level on the CEXn pin to toggle. If the PWMn bit is also set to logic 1, the module operates in Frequency Output Mode.
0: Disabled.
1: Enabled.

Bit1: PWMn: Pulse Width Modulation Mode Enable.
This bit enables/disables the PWM function for PCA0 module n. When enabled, a pulse width modulated signal is output on the CEXn pin. 8-bit PWM is used if PWM16n is logic 0; 16-bit mode is used if PWM16n logic 1. If the TOGn bit is also set, the module operates in Frequency Output Mode.
0: Disabled.
1: Enabled.

Bit0: ECCFn: Capture/Compare Flag Interrupt Enable.
This bit sets the masking of the Capture/Compare Flag (CCFn) interrupt.
0: Disable CCFn interrupts.
1: Enable a Capture/Compare Flag interrupt request when CCFn is set.

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SFR Definition 24.7. PCA0CPHn: PCA0 Capture Module High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SFR Address: PCA0CPH0: 0xFC, PCA0CPH1: 0xFD, PCA0CPH2: 0xEA, PCA0CPH3: 0xEC, PCA0CPH4: 0xEE, PCA0CPH5: 0xE2								
SFR Page: PCA0CPH0: page 0, PCA0CPH1: page 0, PCA0CPH2: page 0, PCA0CPH3: page 0, PCA0CPH4: page 0, PCA0CPH5: page 0								
Bits7–0: PCA0CPHn: PCA0 Capture Module High Byte. The PCA0CPHn register holds the high byte (MSB) of the 16-bit capture module n.								