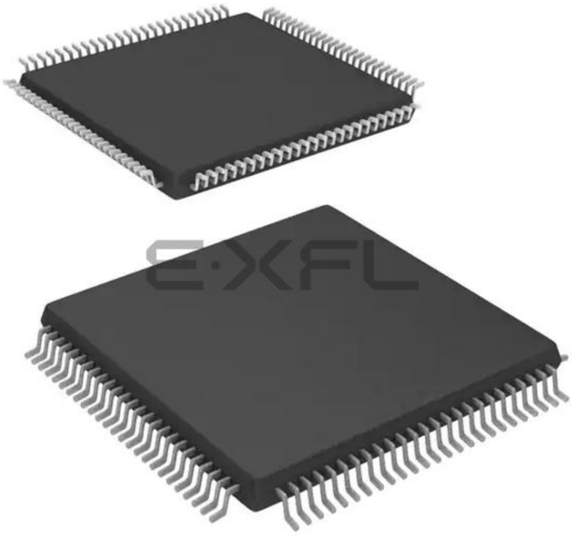

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	64
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x8b, 8x10b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f126-gqr

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1.9. 8-Bit Analog to Digital Converter

The C8051F12x devices have an on-board 8-bit SAR ADC (ADC2) with an 8-channel input multiplexer and programmable gain amplifier. This ADC features a 500 ksps maximum throughput and true 8-bit linearity with an INL of ±1LSB. Eight input pins are available for measurement. The ADC is under full control of the CIP-51 microcontroller via the Special Function Registers. The ADC2 voltage reference is selected between the analog power supply (AV+) and an external VREF pin. On the 100-pin TQFP devices, ADC2 has its own dedicated Voltage Reference input pin; on the 64-pin TQFP devices, ADC2 shares a Voltage Reference input pin with ADC0. User software may put ADC2 into shutdown mode to save power.

A programmable gain amplifier follows the analog multiplexer. The gain stage can be especially useful when different ADC input channels have widely varied input voltage signals, or when it is necessary to "zoom in" on a signal with a large DC offset (in differential mode, a DAC could be used to provide the DC offset). The PGA gain can be set in software to 0.5, 1, 2, or 4.

A flexible conversion scheduling system allows ADC2 conversions to be initiated by software commands, timer overflows, or an external input signal. ADC2 conversions may also be synchronized with ADC0 software-commanded conversions. Conversion completions are indicated by a status bit and an interrupt (if enabled), and the resulting 8-bit data word is latched into an SFR upon completion.

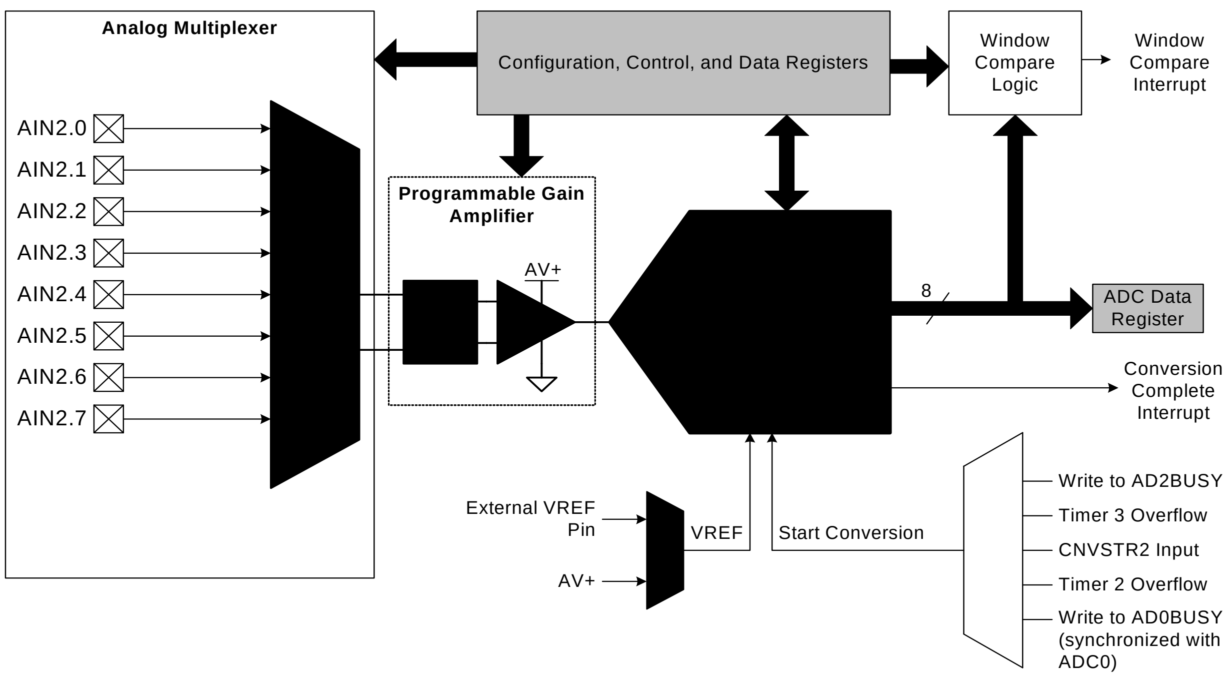


Figure 1.14. 8-Bit ADC Diagram

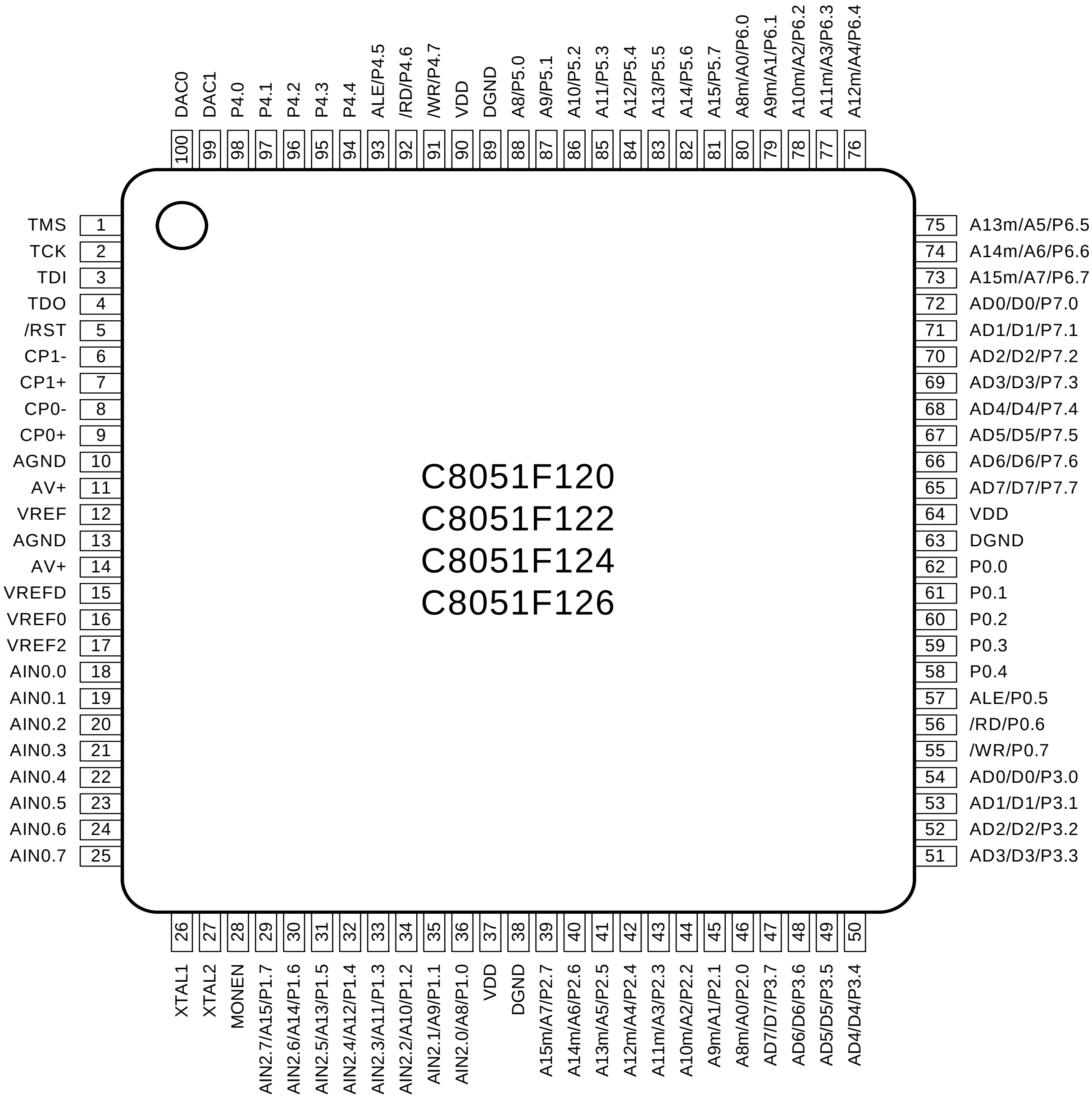


Figure 4.1. C8051F120/2/4/6 Pinout Diagram (TQFP-100)

SFR Definition 5.4. ADC0CN: ADC0 Control

SFR Page: 0
SFR Address: 0xE8 (bit addressable)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
AD0EN	AD0TM	AD0INT	AD0BUSY	AD0CM1	AD0CM0	AD0WINT	AD0LJST	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bit7: AD0EN: ADC0 Enable Bit.
0: ADC0 Disabled. ADC0 is in low-power shutdown.
1: ADC0 Enabled. ADC0 is active and ready for data conversions.

Bit6: AD0TM: ADC Track Mode Bit.
0: When the ADC is enabled, tracking is continuous unless a conversion is in process.
1: Tracking Defined by ADCM1-0 bits.

Bit5: AD0INT: ADC0 Conversion Complete Interrupt Flag.
This flag must be cleared by software.
0: ADC0 has not completed a data conversion since the last time this flag was cleared.
1: ADC0 has completed a data conversion.

Bit4: AD0BUSY: ADC0 Busy Bit.
Read:
0: ADC0 Conversion is complete or a conversion is not currently in progress. AD0INT is set to logic 1 on the falling edge of AD0BUSY.
1: ADC0 Conversion is in progress.
Write:
0: No Effect.
1: Initiates ADC0 Conversion if AD0CM1-0 = 00b.

Bits3–2: AD0CM1–0: ADC0 Start of Conversion Mode Select.
If AD0TM = 0:
00: ADC0 conversion initiated on every write of ‘1’ to AD0BUSY.
01: ADC0 conversion initiated on overflow of Timer 3.
10: ADC0 conversion initiated on rising edge of external CNVSTR0.
11: ADC0 conversion initiated on overflow of Timer 2.
If AD0TM = 1:
00: Tracking starts with the write of ‘1’ to AD0BUSY and lasts for 3 SAR clocks, followed by conversion.
01: Tracking started by the overflow of Timer 3 and lasts for 3 SAR clocks, followed by conversion.
10: ADC0 tracks only when CNVSTR0 input is logic low; conversion starts on rising CNVSTR0 edge.
11: Tracking started by the overflow of Timer 2 and lasts for 3 SAR clocks, followed by conversion.

Bit1: AD0WINT: ADC0 Window Compare Interrupt Flag.
This bit must be cleared by software.
0: ADC0 Window Comparison Data match has not occurred since this flag was last cleared.
1: ADC0 Window Comparison Data match has occurred.

Bit0: AD0LJST: ADC0 Left Justify Select.
0: Data in ADC0H:ADC0L registers are right-justified.
1: Data in ADC0H:ADC0L registers are left-justified.

6.2.3. Settling Time Requirements

A minimum tracking time is required before an accurate conversion can be performed. This tracking time is determined by the ADC0 MUX resistance, the ADC0 sampling capacitance, any external source resistance, and the accuracy required for the conversion. Figure 6.4 shows the equivalent ADC0 input circuits for both Differential and Single-ended modes. Notice that the equivalent time constant for both input circuits is the same. The required settling time for a given settling accuracy (*SA*) may be approximated by Equation 6.1. When measuring the Temperature Sensor output, R_{TOTAL} reduces to R_{MUX}. An absolute minimum settling time of 1.5 µs is required after any MUX or PGA selection. Note that in low-power tracking mode, three SAR clocks are used for tracking at the start of every conversion. For most applications, these three SAR clocks will meet the tracking requirements.

$$t = \ln\left(\frac{2^n}{SA}\right) \times R_{TOTAL}C_{SAMPLE}$$

Equation 6.1. ADC0 Settling Time Requirements

Where:
SA is the settling accuracy, given as a fraction of an LSB (for example, 0.25 to settle within 1/4 LSB)
t is the required settling time in seconds
R_{TOTAL} is the sum of the ADC0 MUX resistance and any external source resistance.
n is the ADC resolution in bits (10).

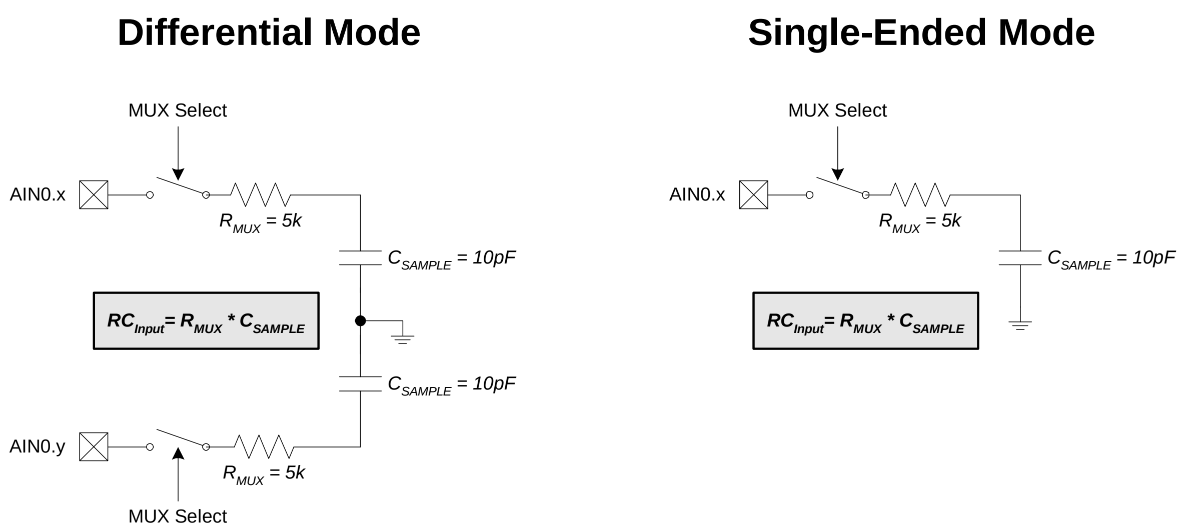
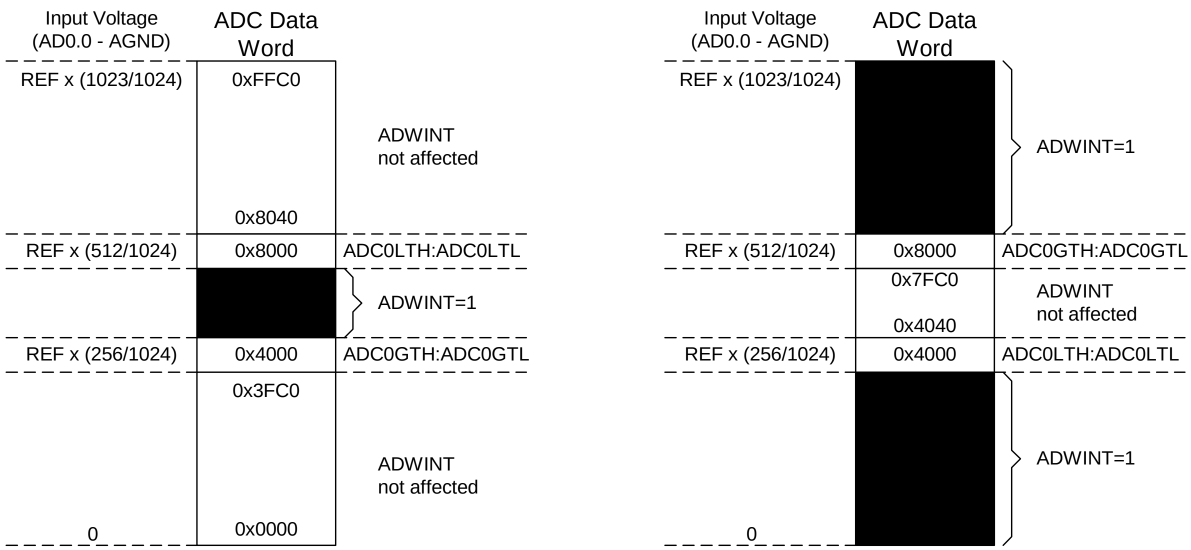


Figure 6.4. ADC0 Equivalent Input Circuits



Given:
AMX0SL = 0x00, AMX0CF = 0x00,
AD0LJST = ‘1’,
ADC0LTH:ADC0LTL = 0x2000,
ADC0GTH:ADC0GTL = 0x1000.
An ADC0 End of Conversion will cause an ADC0 Window Compare Interrupt (AD0WINT = ‘1’) if the resulting ADC0 Data Word is < 0x2000 and > 0x1000.

Given:
AMX0SL = 0x00, AMX0CF = 0x00,
AD0LJST = ‘1’
ADC0LTH:ADC0LTL = 0x1000,
ADC0GTH:ADC0GTL = 0x2000.
An ADC0 End of Conversion will cause an ADC0 Window Compare Interrupt (AD0WINT = ‘1’) if the resulting ADC0 Data Word is < 0x1000 or > 0x2000.

Figure 6.8. 10-Bit ADC0 Window Interrupt Example: Left Justified Single-Ended Data

7.2. ADC2 Modes of Operation

ADC2 has a maximum conversion speed of 500 ksps. The ADC2 conversion clock (SAR2 clock) is a divided version of the system clock, determined by the AD2SC bits in the ADC2CF register. The maximum ADC2 conversion clock is 6 MHz.

7.2.1. Starting a Conversion

A conversion can be initiated in one of five ways, depending on the programmed states of the ADC2 Start of Conversion Mode bits (AD2CM2-0) in ADC2CN. Conversions may be initiated by:

1. Writing a ‘1’ to the AD2BUSY bit of ADC2CN;
2. A Timer 3 overflow (i.e. timed continuous conversions);
3. A rising edge detected on the external ADC convert start signal, CNVSTR2;
4. A Timer 2 overflow (i.e. timed continuous conversions);
5. Writing a ‘1’ to the AD0BUSY of register ADC0CN (initiate conversion of ADC2 and ADC0 with a single software command).

During conversion, the AD2BUSY bit is set to logic 1 and restored to 0 when conversion is complete. The falling edge of AD2BUSY triggers an interrupt (when enabled) and sets the interrupt flag in ADC2CN. Converted data is available in the ADC2 data word, ADC2.

When a conversion is initiated by writing a ‘1’ to AD2BUSY, it is recommended to poll AD2INT to determine when the conversion is complete. The recommended procedure is:

Step 1. Write a ‘0’ to AD2INT;
Step 2. Write a ‘1’ to AD2BUSY;
Step 3. Poll AD2INT for ‘1’;
Step 4. Process ADC2 data.

When CNVSTR2 is used as a conversion start source, it must be enabled in the crossbar, and the corresponding pin must be set to open-drain, high-impedance mode (see **Section “18. Port Input/Output” on page 235** for more details on Port I/O configuration).

7.2.2. Tracking Modes

The AD2TM bit in register ADC2CN controls the ADC2 track-and-hold mode. In its default state, the ADC2 input is continuously tracked, except when a conversion is in progress. When the AD2TM bit is logic 1, ADC2 operates in low-power track-and-hold mode. In this mode, each conversion is preceded by a tracking period of 3 SAR clocks (after the start-of-conversion signal). When the CNVSTR2 signal is used to initiate conversions in low-power tracking mode, ADC2 tracks only when CNVSTR2 is low; conversion begins on the rising edge of CNVSTR2 (see Figure 7.2). Tracking can also be disabled (shutdown) when the entire chip is in low power standby or sleep modes. Low-power Track-and-Hold mode is also useful when AMUX or PGA settings are frequently changed, due to the settling time requirements described in **Section “7.2.3. Settling Time Requirements” on page 94**.

SFR Definition 10.4. CPT1MD: Comparator1 Mode Selection

SFR Page: 2
SFR Address: 0x89

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	CP1RIE	CP1FIE	-	-	CP1MD1	CP1MD0	00000010
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits7–6: UNUSED. Read = 00b, Write = don't care.
Bit 5: CP1RIE: Comparator 1 Rising-Edge Interrupt Enable Bit.
0: Comparator 1 rising-edge interrupt disabled.
1: Comparator 1 rising-edge interrupt enabled.
Bit 4: CP1FIE: Comparator 0 Falling-Edge Interrupt Enable Bit.
0: Comparator 1 falling-edge interrupt disabled.
1: Comparator 1 falling-edge interrupt enabled.
Bits3–2: UNUSED. Read = 00b, Write = don't care.
Bits1–0: CP1MD1–CP1MD0: Comparator1 Mode Select
These bits select the response time for Comparator1.

Mode	CP0MD1	CP0MD0	Notes
0	0	0	Fastest Response Time
1	0	1	—
2	1	0	—
3	1	1	Lowest Power Consumption

Table 11.1. CIP-51 Instruction Set Summary (Continued)

Mnemonic	Description	Bytes	Clock Cycles
MOV direct, @Ri	Move indirect RAM to direct byte	2	2
MOV direct, #data	Move immediate to direct byte	3	3
MOV @Ri, A	Move A to indirect RAM	1	2
MOV @Ri, direct	Move direct byte to indirect RAM	2	2
MOV @Ri, #data	Move immediate to indirect RAM	2	2
MOV DPTR, #data16	Load DPTR with 16-bit constant	3	3
MOVC A, @A+DPTR	Move code byte relative DPTR to A	1	3
MOVC A, @A+PC	Move code byte relative PC to A	1	3
MOVX A, @Ri	Move external data (8-bit address) to A	1	3
MOVX @Ri, A	Move A to external data (8-bit address)	1	3
MOVX A, @DPTR	Move external data (16-bit address) to A	1	3
MOVX @DPTR, A	Move A to external data (16-bit address)	1	3
PUSH direct	Push direct byte onto stack	2	2
POP direct	Pop direct byte from stack	2	2
XCH A, Rn	Exchange Register with A	1	1
XCH A, direct	Exchange direct byte with A	2	2
XCH A, @Ri	Exchange indirect RAM with A	1	2
XCHD A, @Ri	Exchange low nibble of indirect RAM with A	1	2
Boolean Manipulation			
CLR C	Clear Carry	1	1
CLR bit	Clear direct bit	2	2
SETB C	Set Carry	1	1
SETB bit	Set direct bit	2	2
CPL C	Complement Carry	1	1
CPL bit	Complement direct bit	2	2
ANL C, bit	AND direct bit to Carry	2	2
ANL C, /bit	AND complement of direct bit to Carry	2	2
ORL C, bit	OR direct bit to carry	2	2
ORL C, /bit	OR complement of direct bit to Carry	2	2
MOV C, bit	Move direct bit to Carry	2	2
MOV bit, C	Move Carry to direct bit	2	2
JC rel	Jump if Carry is set	2	2/3*
JNC rel	Jump if Carry is not set	2	2/3*
JB bit, rel	Jump if direct bit is set	3	3/4*
JNB bit, rel	Jump if direct bit is not set	3	3/4*
JBC bit, rel	Jump if direct bit is set and clear bit	3	3/4*
Program Branching			
ACALL addr11	Absolute subroutine call	2	3*
LCALL addr16	Long subroutine call	3	4*
RET	Return from subroutine	1	5*
RETI	Return from interrupt	1	5*
AJMP addr11	Absolute jump	2	3*
LJMP addr16	Long jump	3	4*
SJMP rel	Short jump (relative address)	2	3*
JMP @A+DPTR	Jump indirect relative to DPTR	1	3*

14. Oscillators

The devices include a programmable internal oscillator and an external oscillator drive circuit. The internal oscillator can be enabled, disabled, and calibrated using the OSCICN and OSCICL registers, as shown in Figure 14.1. The system clock can be sourced by the external oscillator circuit, the internal oscillator, or the on-chip phase-locked loop (PLL). The internal oscillator's electrical specifications are given in Table 14.1 on page 185.

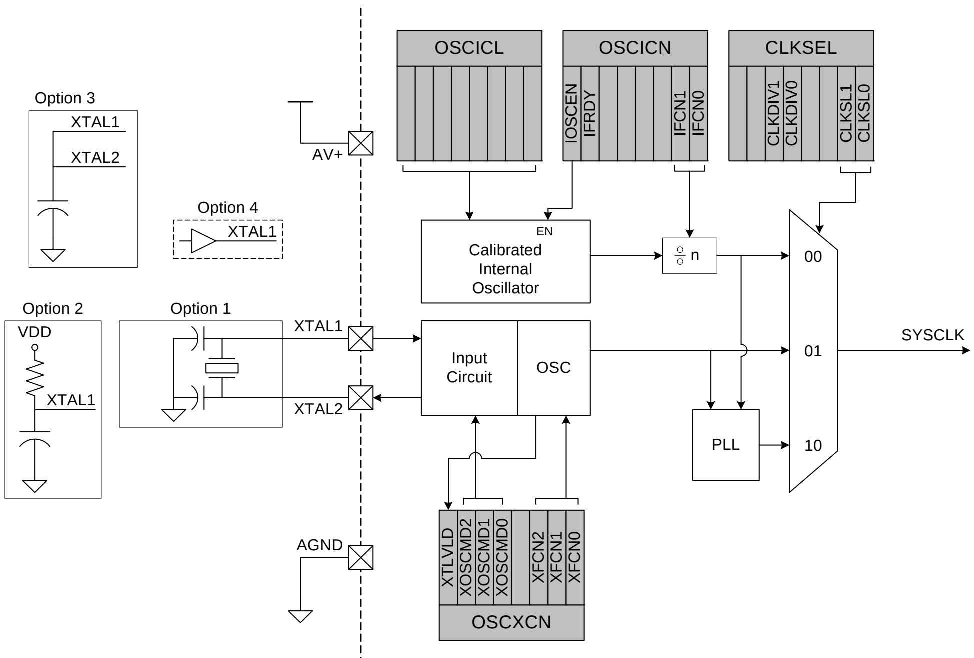


Figure 14.1. Oscillator Diagram

Table 14.1. Oscillator Electrical Characteristics

–40°C to +85°C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Calibrated Internal Oscillator Frequency		24	24.5	25	MHz
Internal Oscillator Supply Current (from V_{DD})	OSCICN.7 = 1	—	400	—	µA
External Clock Frequency		0	—	30	MHz
T_{XCH} (External Clock High Time)		15	—	—	ns
T_{XCL} (External Clock Low Time)		15	—	—	ns

14.1. Internal Calibrated Oscillator

All devices include a calibrated internal oscillator that defaults as the system clock after a system reset. The internal oscillator period can be adjusted via the OSCICL register as defined by SFR Definition 14.1. OSCICL is factory calibrated to obtain a 24.5 MHz frequency.

SFR Definition 15.2. FLSCL: Flash Memory Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	FLRT		Reserved	Reserved	Reserved	FLWE	10000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:

SFR Address: 0xB7
SFR Page: 0

Bits 7–6: Unused.

Bits 5–4: FLRT: Flash Read Time.
These bits should be programmed to the smallest allowed value, according to the system clock speed.
00: SYSCLK $\leq$ 25 MHz.
01: SYSCLK $\leq$ 50 MHz.
10: SYSCLK $\leq$ 75 MHz.
11: SYSCLK $\leq$ 100 MHz.

Bits 3–1: RESERVED. Read = 000b. Must Write 000b.

Bit 0: FLWE: Flash Write/Erase Enable.
This bit must be set to allow Flash writes/erasures from user software.
0: Flash writes/erases disabled.
1: Flash writes/erases enabled.

Important Note: When changing the FLRT bits to a lower setting (e.g. when changing from a value of 11b to 00b), cache reads, cache writes, and the prefetch engine should be disabled using the CCH0CN register (see SFR Definition 16.1).

Table 17.1. AC Parameters for External Memory Interface

Parameter	Description	Min	Max	Units
T_{ACS}	Address/Control Setup Time	0	3 x T_{SYSCLK}	ns
T_{ACW}	Address/Control Pulse Width	1 x T_{SYSCLK}	16 x T_{SYSCLK}	ns
T_{ACH}	Address/Control Hold Time	0	3 x T_{SYSCLK}	ns
T_{ALEH}	Address Latch Enable High Time	1 x T_{SYSCLK}	4 x T_{SYSCLK}	ns
T_{ALEL}	Address Latch Enable Low Time	1 x T_{SYSCLK}	4 x T_{SYSCLK}	ns
T_{WDS}	Write Data Setup Time	1 x T_{SYSCLK}	19 x T_{SYSCLK}	ns
T_{WDH}	Write Data Hold Time	0	3 x T_{SYSCLK}	ns
T_{RDS}	Read Data Setup Time	20	—	ns
T_{RDH}	Read Data Hold Time	0	—	ns

Note: T_{SYSCLK} is equal to one period of the device system clock (SYSCLK).

19.3. SMBus Transfer Modes

The SMBus0 interface may be configured to operate as a master and/or a slave. At any particular time, the interface will be operating in one of the following modes: Master Transmitter, Master Receiver, Slave Transmitter, or Slave Receiver. See Table 19.1 for transfer mode status decoding using the SMB0STA status register. The following mode descriptions illustrate an interrupt-driven SMBus0 application; SMBus0 may alternatively be operated in polled mode.

19.3.1. Master Transmitter Mode

Serial data is transmitted on SDA while the serial clock is output on SCL. SMBus0 generates a START condition and then transmits the first byte containing the address of the target slave device and the data direction bit. In this case the data direction bit (R/W) will be logic 0 to indicate a "WRITE" operation. The SMBus0 interface transmits one or more bytes of serial data, waiting for an acknowledge (ACK) from the slave after each byte. To indicate the end of the serial transfer, SMBus0 generates a STOP condition.

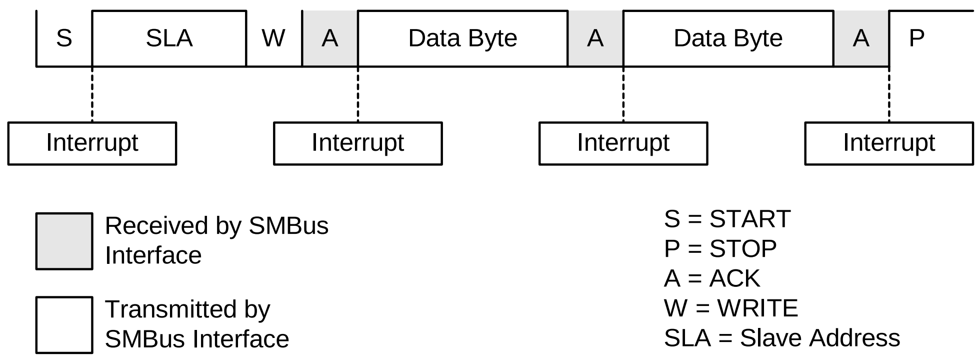


Figure 19.4. Typical Master Transmitter Sequence

19.3.2. Master Receiver Mode

Serial data is received on SDA while the serial clock is output on SCL. The SMBus0 interface generates a START followed by the first data byte containing the address of the target slave and the data direction bit. In this case the data direction bit (R/W) will be logic 1 to indicate a "READ" operation. The SMBus0 interface receives serial data from the slave and generates the clock on SCL. After each byte is received, SMBus0 generates an ACK or NACK depending on the state of the AA bit in register SMB0CN. SMBus0 generates a STOP condition to indicate the end of the serial transfer.

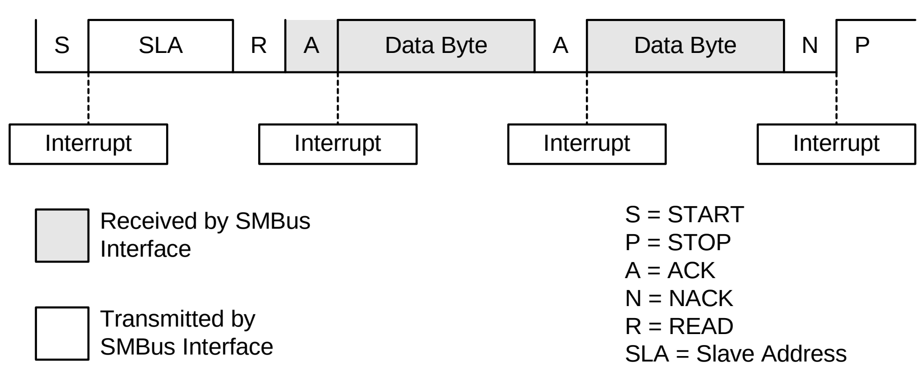


Figure 19.5. Typical Master Receiver Sequence

19.3.3. Slave Transmitter Mode

Serial data is transmitted on SDA while the serial clock is received on SCL. The SMBus0 interface receives a START followed by data byte containing the slave address and direction bit. If the received slave address matches the address held in register SMB0ADR, the SMBus0 interface generates an ACK. SMBus0 will also ACK if the general call address (0x00) is received and the General Call Address Enable bit (SMB0ADR.0) is set to logic 1. In this case the data direction bit (R/W) will be logic 1 to indicate a "READ" operation. The SMBus0 interface receives the clock on SCL and transmits one or more bytes of serial data, waiting for an ACK from the master after each byte. SMBus0 exits slave mode after receiving a STOP condition from the master.

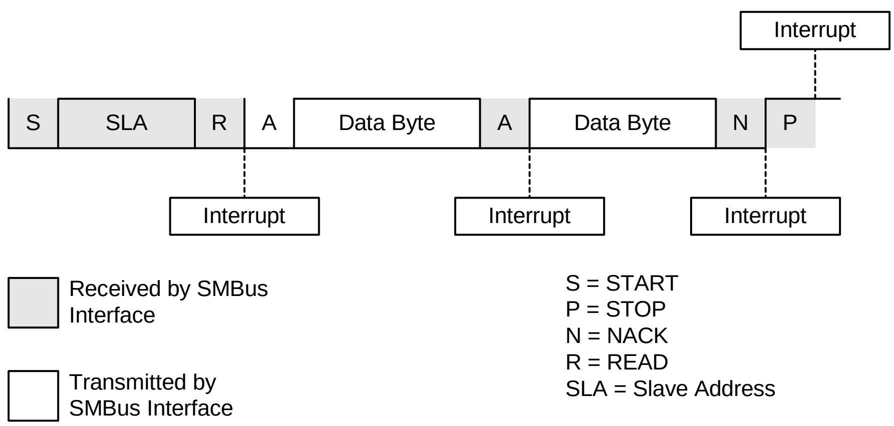


Figure 19.6. Typical Slave Transmitter Sequence

19.3.4. Slave Receiver Mode

Serial data is received on SDA while the serial clock is received on SCL. The SMBus0 interface receives a START followed by data byte containing the slave address and direction bit. If the received slave address matches the address held in register SMB0ADR, the interface generates an ACK. SMBus0 will also ACK if the general call address (0x00) is received and the General Call Address Enable bit (SMB0ADR.0) is set to logic 1. In this case the data direction bit (R/W) will be logic 0 to indicate a "WRITE" operation. The SMBus0 interface receives one or more bytes of serial data; after each byte is received, the interface transmits an ACK or NACK depending on the state of the AA bit in SMB0CN. SMBus0 exits Slave Receiver Mode after receiving a STOP condition from the master.

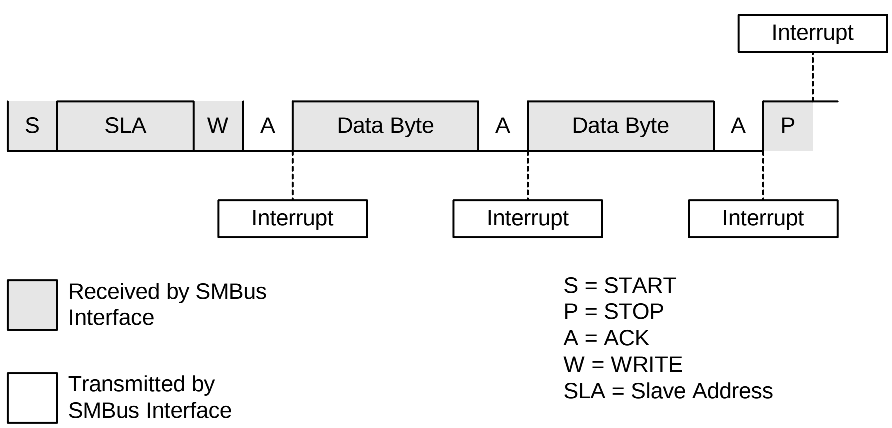


Figure 19.7. Typical Slave Receiver Sequence

21.1. UART0 Operational Modes

UART0 provides four operating modes (one synchronous and three asynchronous) selected by setting configuration bits in the SCON0 register. These four modes offer different baud rates and communication protocols. The four modes are summarized in Table 21.1.

Table 21.1. UART0 Modes

Mode	Synchronization	Baud Clock	Data Bits	Start/Stop Bits
0	Synchronous	SYSCLK / 12	8	None
1	Asynchronous	Timer 1, 2, 3, or 4 Overflow	8	1 Start, 1 Stop
2	Asynchronous	SYSCLK / 32 or SYSCLK / 64	9	1 Start, 1 Stop
3	Asynchronous	Timer 1, 2, 3, or 4 Overflow	9	1 Start, 1 Stop

21.1.1. Mode 0: Synchronous Mode

Mode 0 provides synchronous, half-duplex communication. Serial data is transmitted and received on the RX0 pin. The TX0 pin provides the shift clock for both transmit and receive. The MCU must be the master since it generates the shift clock for transmission in both directions (see the interconnect diagram in Figure 21.3).

Data transmission begins when an instruction writes a data byte to the SBUF0 register. Eight data bits are transferred LSB first (see the timing diagram in Figure 21.2), and the TI0 Transmit Interrupt Flag (SCON0.1) is set at the end of the eighth bit time. Data reception begins when the REN0 Receive Enable bit (SCON0.4) is set to logic 1 and the RI0 Receive Interrupt Flag (SCON0.0) is cleared. One cycle after the eighth bit is shifted in, the RI0 flag is set and reception stops until software clears the RI0 bit. An interrupt will occur if enabled when either TI0 or RI0 are set.

The Mode 0 baud rate is SYSCLK / 12. RX0 is forced to open-drain in Mode 0, and an external pullup will typically be required.

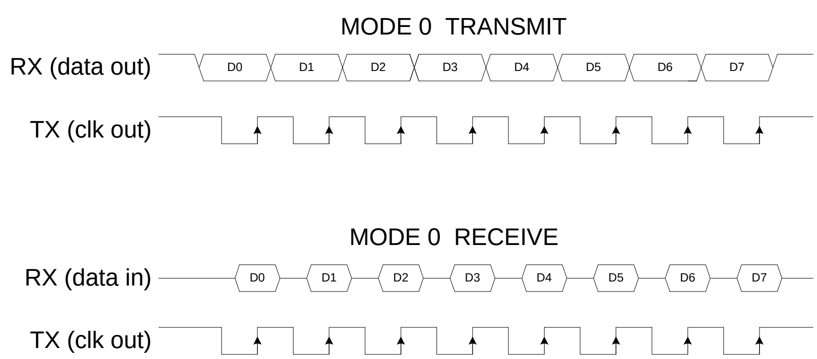


Figure 21.2. UART0 Mode 0 Timing Diagram

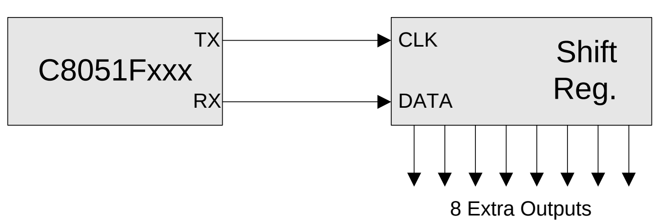


Figure 21.3. UART0 Mode 0 Interconnect

SFR Definition 23.2. TMOD: Timer Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
GATE1	C/T1	T1M1	T1M0	GATE0	C/T0	T0M1	T0M0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x89
SFR Page: 0

Bit7: GATE1: Timer 1 Gate Control.
0: Timer 1 enabled when TR1 = 1 irrespective of /INT1 logic level.
1: Timer 1 enabled only when TR1 = 1 AND /INT1 = logic 1.

Bit6: C/T1: Counter/Timer 1 Select.
0: Timer Function: Timer 1 incremented by clock defined by T1M bit (CKCON.4).
1: Counter Function: Timer 1 incremented by high-to-low transitions on external input pin (T1).

Bits5–4: T1M1–T1M0: Timer 1 Mode Select.
These bits select the Timer 1 operation mode.

T1M1	T1M0	Mode
0	0	Mode 0: 13-bit counter/timer
0	1	Mode 1: 16-bit counter/timer
1	0	Mode 2: 8-bit counter/timer with auto-reload
1	1	Mode 3: Timer 1 inactive

Bit3: GATE0: Timer 0 Gate Control.
0: Timer 0 enabled when TR0 = 1 irrespective of /INT0 logic level.
1: Timer 0 enabled only when TR0 = 1 AND /INT0 = logic 1.

Bit2: C/T0: Counter/Timer Select.
0: Timer Function: Timer 0 incremented by clock defined by T0M bit (CKCON.3).
1: Counter Function: Timer 0 incremented by high-to-low transitions on external input pin (T0).

Bits1–0: T0M1–T0M0: Timer 0 Mode Select.
These bits select the Timer 0 operation mode.

T0M1	T0M0	Mode
0	0	Mode 0: 13-bit counter/timer
0	1	Mode 1: 16-bit counter/timer
1	0	Mode 2: 8-bit counter/timer with auto-reload
1	1	Mode 3: Two 8-bit counter/timers

SFR Definition 23.5. TL1: Timer 1 Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x8B
SFR Page: 0

Bits 7–0: TL1: Timer 1 Low Byte.
The TL1 register is the low byte of the 16-bit Timer 1.

SFR Definition 23.6. TH0: Timer 0 High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x8C
SFR Page: 0

Bits 7–0: TH0: Timer 0 High Byte.
The TH0 register is the high byte of the 16-bit Timer 0.

SFR Definition 23.7. TH1: Timer 1 High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x8D
SFR Page: 0

Bits 7–0: TH1: Timer 1 High Byte.
The TH1 register is the high byte of the 16-bit Timer 1.

SFR Definition 24.4. PCA0L: PCA0 Counter/Timer Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xF9
SFR Page: 0

Bits 7–0: PCA0L: PCA0 Counter/Timer Low Byte.
The PCA0L register holds the low byte (LSB) of the 16-bit PCA0 Counter/Timer.

SFR Definition 24.5. PCA0H: PCA0 Counter/Timer High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xFA
SFR Page: 0

Bits 7–0: PCA0H: PCA0 Counter/Timer High Byte.
The PCA0H register holds the high byte (MSB) of the 16-bit PCA0 Counter/Timer.

SFR Definition 24.6. PCA0CPLn: PCA0 Capture Module Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: PCA0CPL0: 0xFB, PCA0CPL1: 0xFD, PCA0CPL2: 0xE9, PCA0CPL3: 0xEB, PCA0CPL4: 0xED, PCA0CPL5: 0xE1

SFR Page: PCA0CPL0: page 0, PCA0CPL1: page 0, PCA0CPL2: page 0, PCA0CPL3: page 0, PCA0CPL4: page 0, PCA0CPL5: page 0

Bits7–0: PCA0CPLn: PCA0 Capture Module Low Byte.
The PCA0CPLn register holds the low byte (LSB) of the 16-bit capture module n.