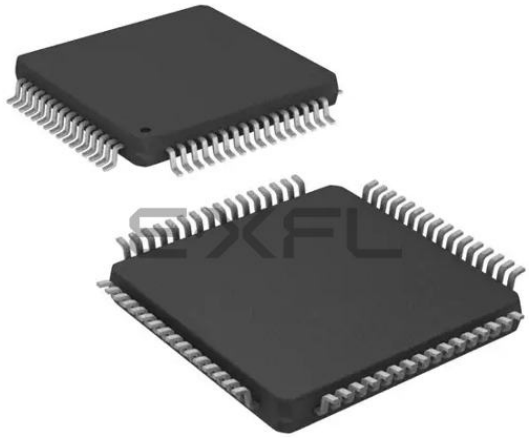

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	32
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x8b, 8x10b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f127-gqr

Table of Contents

1.2. On-Chip Memory

The CIP-51 has a standard 8051 program and data address configuration. It includes 256 bytes of data RAM, with the upper 128 bytes dual-mapped. Indirect addressing accesses the upper 128 bytes of general purpose RAM, and direct addressing accesses the 128 byte SFR address space. The lower 128 bytes of RAM are accessible via direct and indirect addressing. The first 32 bytes are addressable as four banks of general purpose registers, and the next 16 bytes can be byte addressable or bit addressable.

The devices include an on-chip 8k byte RAM block and an external memory interface (EMIF) for accessing off-chip data memory. The on-chip 8k byte block can be addressed over the entire 64k external data memory address range (overlapping 8k boundaries). External data memory address space can be mapped to on-chip memory only, off-chip memory only, or a combination of the two (addresses up to 8k directed to on-chip, above 8k directed to EMIF). The EMIF is also configurable for multiplexed or non-multiplexed address/data lines.

On the C8051F12x and C8051F130/1, the MCU's program memory consists of 128 k bytes of banked Flash memory. The 1024 bytes from addresses 0x1FC00 to 0x1FFFF are reserved. On the C8051F132/3, the MCU's program memory consists of 64 k bytes of Flash memory. This memory may be reprogrammed in-system in 1024 byte sectors, and requires no special off-chip programming voltage.

On all devices, there are also two 128 byte sectors at addresses 0x20000 to 0x200FF, which may be used by software for data storage. See Figure 1.8 for the MCU system memory map.

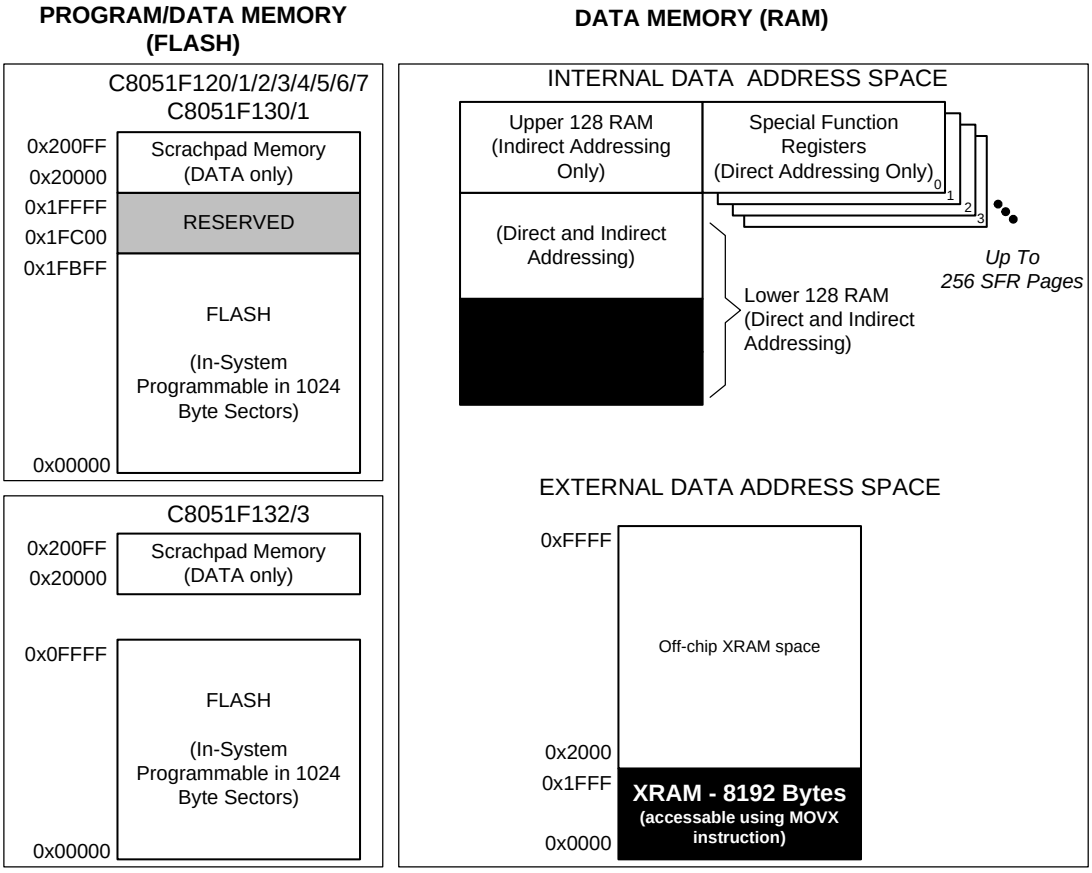


Figure 1.8. On-Chip Memory Map

12-bit ADC0 Data Word appears in the ADC0 Data Word Registers as follows:
ADC0H[3:0]:ADC0L[7:0], if AD0LJST = 0
(ADC0H[7:4] will be sign-extension of ADC0H.3 for a differential reading, otherwise =
0000b).

ADC0H[7:0]:ADC0L[7:4], if AD0LJST = 1
(ADC0L[3:0] = 0000b).

Example: ADC0 Data Word Conversion Map, AIN0.0 Input in Single-Ended Mode
(AMX0CF = 0x00, AMX0SL = 0x00)

AIN0.0–AGND (Volts)	**ADC0H:ADC0L** (AD0LJST = 0)	**ADC0H:ADC0L** (AD0LJST = 1)
VREF x (4095/4096)	0x0FFF	0xFFF0
VREF / 2	0x0800	0x8000
VREF x (2047/4096)	0x07FF	0x7FF0
0	0x0000	0x0000

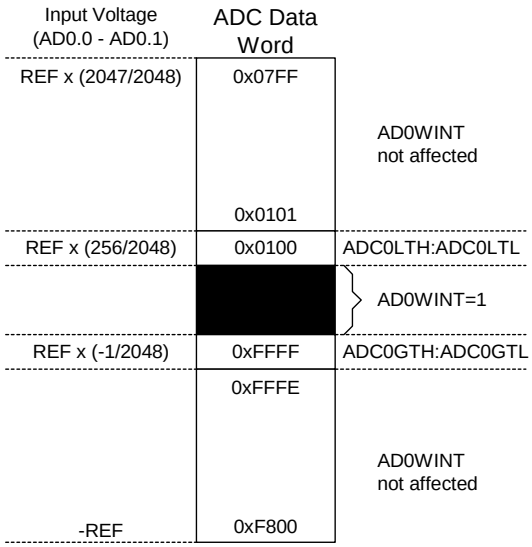
Example: ADC0 Data Word Conversion Map, AIN0.0-AIN0.1 Differential Input Pair
(AMX0CF = 0x01, AMX0SL = 0x00)

AIN0.0–AIN0.1 (Volts)	**ADC0H:ADC0L** (AD0LJST = 0)	**ADC0H:ADC0L** (AD0LJST = 1)
VREF x (2047/2048)	0x07FF	0x7FF0
VREF / 2	0x0400	0x4000
VREF x (1/2048)	0x0001	0x0010
0	0x0000	0x0000
–VREF x (1/2048)	0xFFFF (–1d)	0xFFF0
–VREF / 2	0xFC00 (–1024d)	0xC000
–VREF	0xF800 (–2048d)	0x8000

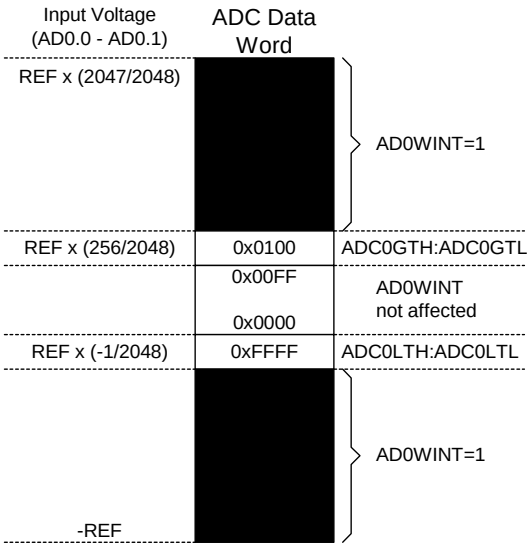
For AD0LJST = 0:

$$Code = Vin \times \frac{Gain}{VREF} \times 2^n$$; 'n' = 12 for Single-Ended; 'n'=11 for Differential.

Figure 5.5. ADC0 Data Word Example

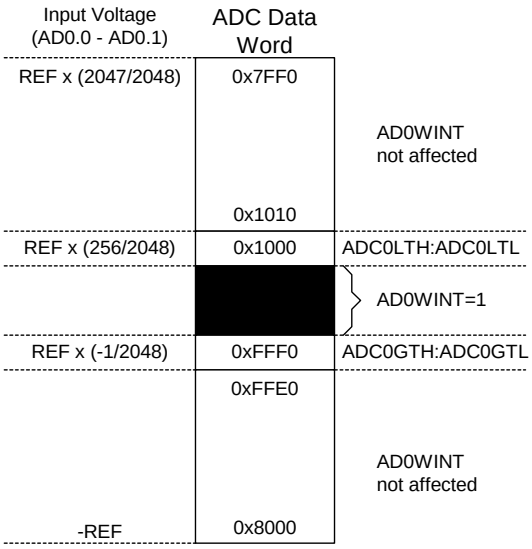


Given:
AMX0SL = 0x00, AMX0CF = 0x01,
AD0LJST = '0',
ADC0LTH:ADC0LTL = 0x0100,
ADC0GTH:ADC0GTL = 0xFFFF.
An ADC0 End of Conversion will cause an ADC0 Window Compare Interrupt (AD0WINT = '1') if the resulting ADC0 Data Word is < 0x0100 and > 0xFFFF. (In 2s-complement math, 0xFFFF = -1.)

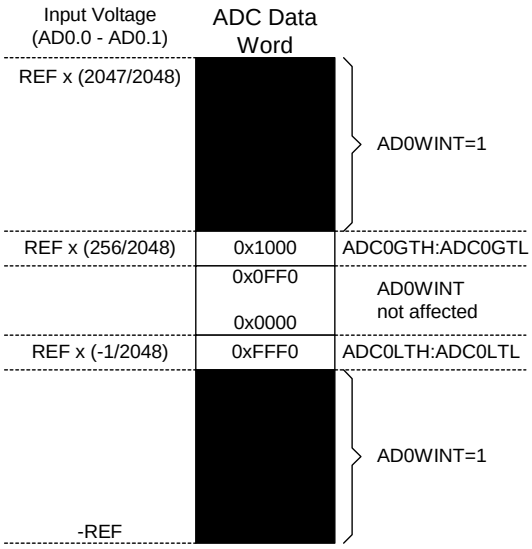


Given:
AMX0SL = 0x00, AMX0CF = 0x01,
AD0LJST = '0',
ADC0LTH:ADC0LTL = 0xFFFF,
ADC0GTH:ADC0GTL = 0x0100.
An ADC0 End of Conversion will cause an ADC0 Window Compare Interrupt (AD0WINT = '1') if the resulting ADC0 Data Word is < 0xFFFF or > 0x0100. (In 2s-complement math, 0xFFFF = -1.)

Figure 5.7. 12-Bit ADC0 Window Interrupt Example: Right Justified Differential Data



Given:
AMX0SL = 0x00, AMX0CF = 0x01,
AD0LJST = '1',
ADC0LTH:ADC0LTL = 0x1000,
ADC0GTH:ADC0GTL = 0xFFF0.
An ADC0 End of Conversion will cause an ADC0 Window Compare Interrupt (AD0WINT = '1') if the resulting ADC0 Data Word is < 0x1000 and > 0xFFF0. (2s-complement math.)



Given:
AMX0SL = 0x00, AMX0CF = 0x01,
AD0LJST = '1',
ADC0LTH:ADC0LTL = 0xFFF0,
ADC0GTH:ADC0GTL = 0x1000.
An ADC0 End of Conversion will cause an ADC0 Window Compare Interrupt (AD0WINT = '1') if the resulting ADC0 Data Word is < 0xFFF0 or > 0x1000. (2s-complement math.)

Figure 5.9. 12-Bit ADC0 Window Interrupt Example: Left Justified Differential Data

6.2.2. Tracking Modes

The AD0TM bit in register ADC0CN controls the ADC0 track-and-hold mode. In its default state, the ADC0 input is continuously tracked when a conversion is not in progress. When the AD0TM bit is logic 1, ADC0 operates in low-power track-and-hold mode. In this mode, each conversion is preceded by a tracking period of 3 SAR clocks (after the start-of-conversion signal). When the CNVSTR0 signal is used to initiate conversions in low-power tracking mode, ADC0 tracks only when CNVSTR0 is low; conversion begins on the rising edge of CNVSTR0 (see Figure 6.3). Tracking can also be disabled (shutdown) when the entire chip is in low power standby or sleep modes. Low-power track-and-hold mode is also useful when AMUX or PGA settings are frequently changed, to ensure that settling time requirements are met (see **Section "6.2.3. Settling Time Requirements" on page 77**).

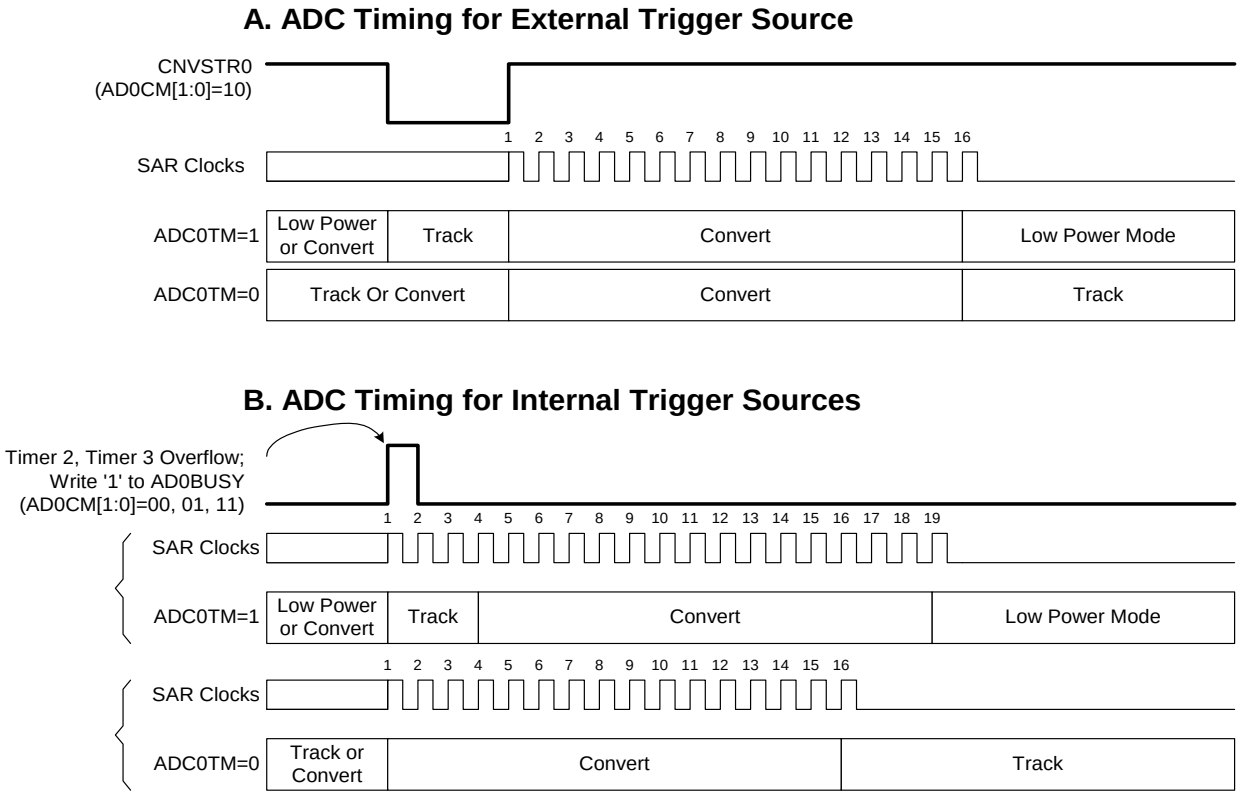


Figure 6.3. ADC0 Track and Conversion Example Timing

10-bit ADC0 Data Word appears in the ADC0 Data Word Registers as follows:
ADC0H[1:0]:ADC0L[7:0], if AD0LJST = 0
(ADC0H[7:2] will be sign-extension of ADC0H.1 for a differential reading, otherwise =
000000b).

ADC0H[7:0]:ADC0L[7:6], if AD0LJST = 1
(ADC0L[5:0] = 00b).

Example: ADC0 Data Word Conversion Map, AIN0.0 Input in Single-Ended Mode
(AMX0CF = 0x00, AMX0SL = 0x00)

AIN0.0–AGND (Volts)	**ADC0H:ADC0L** (AD0LJST = 0)	**ADC0H:ADC0L** (AD0LJST = 1)
VREF x (1023/1024)	0x03FF	0xFFC0
VREF / 2	0x0200	0x8000
VREF x (511/1024)	0x01FF	0x7FC0
0	0x0000	0x0000

Example: ADC0 Data Word Conversion Map, AIN0.0-AIN0.1 Differential Input Pair
(AMX0CF = 0x01, AMX0SL = 0x00)

AIN0.0–AIN0.1 (Volts)	**ADC0H:ADC0L** (AD0LJST = 0)	**ADC0H:ADC0L** (AD0LJST = 1)
VREF x (511/512)	0x01FF	0x7FC0
VREF / 2	0x0100	0x4000
VREF x (1/512)	0x0001	0x0040
0	0x0000	0x0000
–VREF x (1/512)	0xFFFF (–1d)	0xFFC0
–VREF / 2	0xFF00 (–256d)	0xC000
–VREF	0xFE00 (–512d)	0x8000

For AD0LJST = 0:

$$Code = Vin \times \frac{Gain}{VREF} \times 2^n$$; 'n' = 10 for Single-Ended; 'n'= 9 for Differential.

Figure 6.5. ADC0 Data Word Example

SFR Definition 7.1. AMX2CF: AMUX2 Configuration

SFR Page: 2
SFR Address: 0xBA

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	PIN67IC	PIN45IC	PIN23IC	PIN01IC	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits7–4: UNUSED. Read = 0000b; Write = don't care.
Bit3: PIN67IC: AIN2.6, AIN2.7 Input Pair Configuration Bit.
0: AIN2.6 and AIN2.7 are independent single-ended inputs.
1: AIN2.6 and AIN2.7 are (respectively) +, – differential input pair.
Bit2: PIN45IC: AIN2.4, AIN2.5 Input Pair Configuration Bit.
0: AIN2.4 and AIN2.5 are independent single-ended inputs.
1: AIN2.4 and AIN2.5 are (respectively) +, – differential input pair.
Bit1: PIN23IC: AIN2.2, AIN2.3 Input Pair Configuration Bit.
0: AIN2.2 and AIN2.3 are independent single-ended inputs.
1: AIN2.2 and AIN2.3 are (respectively) +, – differential input pair.
Bit0: PIN01IC: AIN2.0, AIN2.1 Input Pair Configuration Bit.
0: AIN2.0 and AIN2.1 are independent single-ended inputs.
1: AIN2.0 and AIN2.1 are (respectively) +, – differential input pair.

Note: The ADC2 Data Word is in 2's complement format for channels configured as differential.

9. Voltage Reference

The voltage reference options available on the C8051F12x and C8051F13x device families vary according to the device capabilities.

All devices include an internal voltage reference circuit, consisting of a 1.2 V, 15 ppm/°C (typical) bandgap voltage reference generator and a gain-of-two output buffer amplifier. The internal reference may be routed via the VREF pin to external system components or to the voltage reference input pins. The maximum load seen by the VREF pin must be less than 200 µA to AGND. Bypass capacitors of 0.1 µF and 4.7 µF are recommended from the VREF pin to AGND.

The Reference Control Register, REF0CN enables/disables the internal reference generator and the internal temperature sensor on all devices. The BIASE bit in REF0CN enables the on-board reference generator while the REFBE bit enables the gain-of-two buffer amplifier which drives the VREF pin. When disabled, the supply current drawn by the bandgap and buffer amplifier falls to less than 1 µA (typical) and the output of the buffer amplifier enters a high impedance state. If the internal bandgap is used as the reference voltage generator, BIASE and REFBE must both be set to logic 1. If the internal reference is not used, REFBE may be set to logic 0. Note that the BIASE bit must be set to logic 1 if any DACs or ADCs are used, regardless of whether the voltage reference is derived from the on-chip reference or supplied by an off-chip source. If no ADCs or DACs are being used, both of these bits can be set to logic 0 to conserve power.

When enabled, the temperature sensor connects to the highest order input of the ADC0 input multiplexer. The TEMPE bit within REF0CN enables and disables the temperature sensor. While disabled, the temperature sensor defaults to a high impedance state. Any ADC measurements performed on the sensor while disabled will result in undefined data.

The electrical specifications for the internal voltage reference are given in Table 9.1.

9.1. Reference Configuration on the C8051F120/2/4/6

On the C8051F120/2/4/6 devices, the REF0CN register also allows selection of the voltage reference source for ADC0 and ADC2, as shown in SFR Definition 9.1. Bits AD0VRS and AD2VRS in the REF0CN register select the ADC0 and ADC2 voltage reference sources, respectively. Three voltage reference input pins allow each ADC and the two DACs to reference an external voltage reference or the on-chip voltage reference output (with an external connection). ADC0 may also reference the DAC0 output internally, and ADC2 may reference the analog power supply voltage, via the VREF multiplexers shown in Figure 9.1.

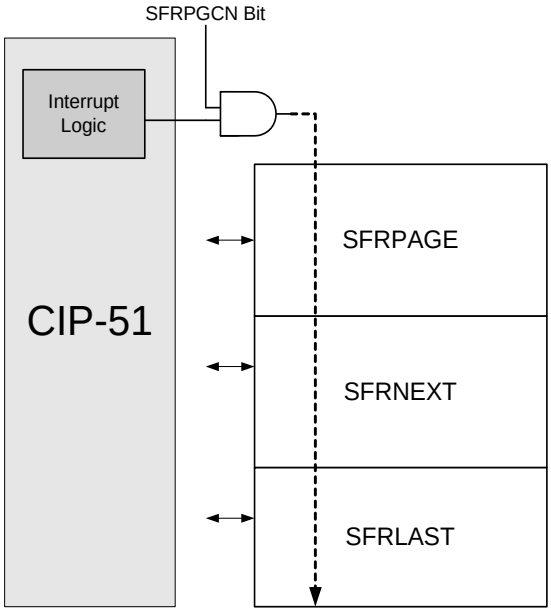


Figure 11.4. SFR Page Stack

Automatic hardware switching of the SFR Page on interrupts may be enabled or disabled as desired using the SFR Automatic Page Control Enable Bit located in the SFR Page Control Register (SFRPGCN). This function defaults to ‘enabled’ upon reset. In this way, the autoswitching function will be enabled unless disabled in software.

A summary of the SFR locations (address and SFR page) is provided in Table 11.2. in the form of an SFR memory map. Each memory location in the map has an SFR page row, denoting the page in which that SFR resides. Note that certain SFR’s are accessible from ALL SFR pages, and are denoted by the “**(ALL PAGES)**” designation. For example, the Port I/O registers P0, P1, P2, and P3 all have the “**(ALL PAGES)**” designation, indicating these SFR’s are accessible from all SFR pages regardless of the SFRPAGE register value.

SFR Definition 12.7. MAC0ACC3: MAC0 Accumulator Byte 3

R	R	R	R	R	R	R	R	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x96
SFR Page: 3

Bits 7–0: Byte 3 (bits 31–24) of MAC0 Accumulator.

***Note:** The contents of this register should not be changed by software during the first two MAC0 pipeline stages.

SFR Definition 12.8. MAC0ACC2: MAC0 Accumulator Byte 2

R	R	R	R	R	R	R	R	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x95
SFR Page: 3

Bits 7–0: Byte 2 (bits 23–16) of MAC0 Accumulator.

***Note:** The contents of this register should not be changed by software during the first two MAC0 pipeline stages.

SFR Definition 12.9. MAC0ACC1: MAC0 Accumulator Byte 1

R	R	R	R	R	R	R	R	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x94
SFR Page: 3

Bits 7–0: Byte 1 (bits 15–8) of MAC0 Accumulator.

***Note:** The contents of this register should not be changed by software during the first two MAC0 pipeline stages.

15.1.3. Writing Flash Memory From Software

Bytes in Flash memory can be written one byte at a time, or in small blocks. The CHBLKW bit in register CCH0CN (SFR Definition 16.1) controls whether a single byte or a block of bytes is written to Flash during a write operation. When CHBLKW is cleared to '0', the Flash will be written one byte at a time. When CHBLKW is set to '1', the Flash will be written in blocks of four bytes for addresses in code space, or blocks of two bytes for addresses in the Scratchpad area. Block writes are performed in the same amount of time as single byte writes, which can save time when storing large amounts of data to Flash memory.

For single-byte writes to Flash, bytes are written individually, and the Flash write is performed after each MOVX write instruction. The recommended procedure for writing Flash in single bytes is as follows:

Step 1. Disable interrupts.
Step 2. Clear CHBLKW (CCH0CN.0) to select single-byte write mode.
Step 3. If writing to bytes in Bank 1, Bank 2, or Bank 3, set the COBANK bits (PSBANK.5-4) for the appropriate bank.
Step 4. If writing to bytes in the Scratchpad area, set the SFLE bit (PSCTL.2).
Step 5. Set FLWE (FLSCL.0) to enable Flash writes/erases via user software.
Step 6. Set PSWE (PSCTL.0) to redirect MOVX commands to write to Flash.
Step 7. Use the MOVX instruction to write a data byte to the desired location (repeat as necessary).
Step 8. Clear the PSWE bit to redirect MOVX commands to the XRAM data space.
Step 9. Clear the FLWE bit, to disable Flash writes/erases.
Step 10. If writing to bytes in the Scratchpad area, clear the SFLE bit.
Step 11. Re-enable interrupts.

For block Flash writes, the Flash write procedure is only performed after the last byte of each block is written with the MOVX write instruction. When writing to addresses located in any of the four code banks, a Flash write block is four bytes long, from addresses ending in 00b to addresses ending in 11b. Writes must be performed sequentially (i.e. addresses ending in 00b, 01b, 10b, and 11b must be written in order). The Flash write will be performed following the MOVX write that targets the address ending in 11b. When writing to addresses located in the Flash Scratchpad area, a Flash block is two bytes long, from addresses ending in 0b to addresses ending in 1b. The Flash write will be performed following the MOVX write that targets the address ending in 1b. If any bytes in the block do not need to be updated in Flash, they should be written to 0xFF. The recommended procedure for writing Flash in blocks is as follows:

Step 1. Disable interrupts.
Step 2. Set CHBLKW (CCH0CN.0) to select block write mode.
Step 3. If writing to bytes in Bank 1, Bank 2, or Bank 3, set the COBANK bits (PSBANK.5-4) for the appropriate bank.
Step 4. If writing to bytes in the Scratchpad area, set the SFLE bit (PSCTL.2).
Step 5. Set FLWE (FLSCL.0) to enable Flash writes/erases via user software.
Step 6. Set PSWE (PSCTL.0) to redirect MOVX commands to write to Flash.
Step 7. Use the MOVX instruction to write data bytes to the desired block. The data bytes must be written sequentially, and the last byte written must be the high byte of the block (see text for details, repeat as necessary).
Step 8. Clear the PSWE bit to redirect MOVX commands to the XRAM data space.
Step 9. Clear the FLWE bit, to disable Flash writes/erases.
Step 10. If writing to bytes in the Scratchpad area, clear the SFLE bit.
Step 11. Re-enable interrupts.

SFR Definition 16.4. CCH0MA: Cache Miss Accumulator

R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
CHMSOV	CHMSCTH							00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x9A
SFR Page: F

Bit 7: CHMSOV: Cache Miss Penalty Overflow.
This bit indicates when the Cache Miss Penalty Accumulator has overflowed since it was last written.
0: The Cache Miss Penalty Accumulator has not overflowed since it was last written.
1: An overflow of the Cache Miss Penalty Accumulator has occurred since it was last written.

Bits 6–0: CHMSCTH: Cache Miss Penalty Accumulator (bits 11–5)
These are bits 11-5 of the Cache Miss Penalty Accumulator. The next four bits (bits 4-1) are stored in CHMSCTL in the CCH0TN register.
The Cache Miss Penalty Accumulator is incremented every clock cycle that the processor is delayed due to a cache miss. This is primarily used as a diagnostic feature, when optimizing code for execution speed.
Writing to CHMSCTH clears the lower 5 bits of the Cache Miss Penalty Accumulator.
Reading from CHMSCTH returns the current value of CHMSTCH, and latches bits 4-1 into CHMSTCL so that they can be read. Because bit 0 of the Cache Miss Penalty Accumulator is not available, the Cumulative Miss Penalty is equal to 2 * (CCHMSTCH:CCHMSTCL).

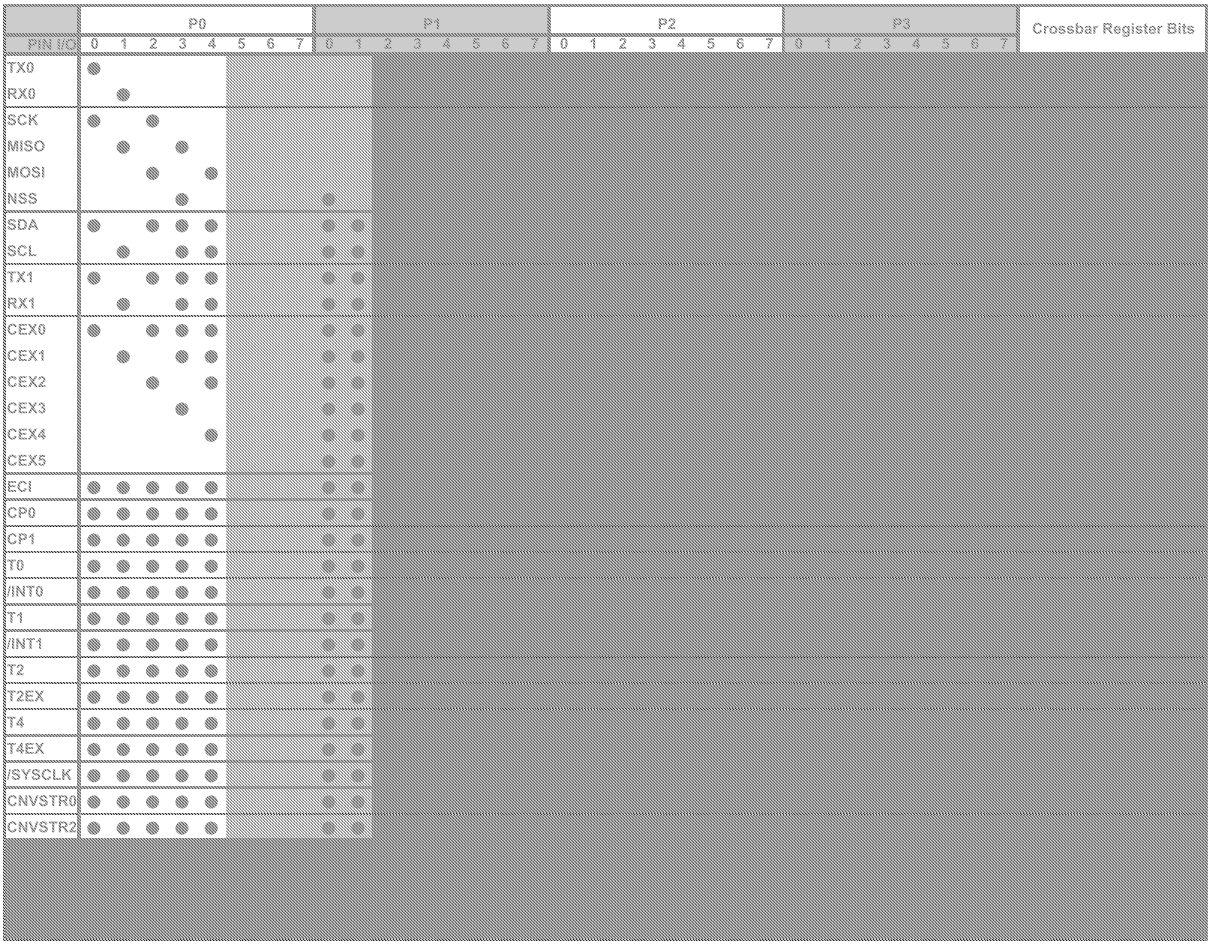
SFR Definition 16.5. FLSTAT: Flash Status

R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	-	-	-	FLBUSY	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0x88
SFR Page: F

Bit 7–1: Reserved.

Bit 0: FLBUSY: Flash Busy
This bit indicates when a Flash write or erase operation is in progress.
0: Flash is idle or reading.
1: Flash write/erase operation is currently in progress.



**(EMIFLE = 1; EMIF in Multiplexed Mode; P1MDIN = 0xE3;
XBR0 = 0x05; XBR1 = 0x14; XBR2 = 0x42)**

Figure 18.6. Crossbar Example

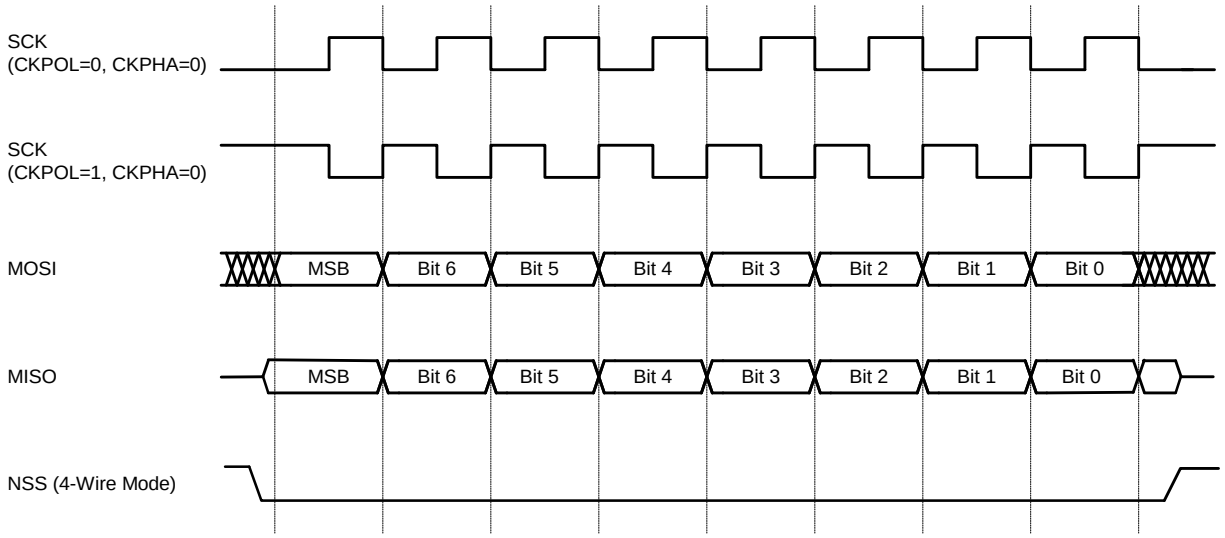


Figure 20.6. Slave Mode Data/Clock Timing (CKPHA = 0)

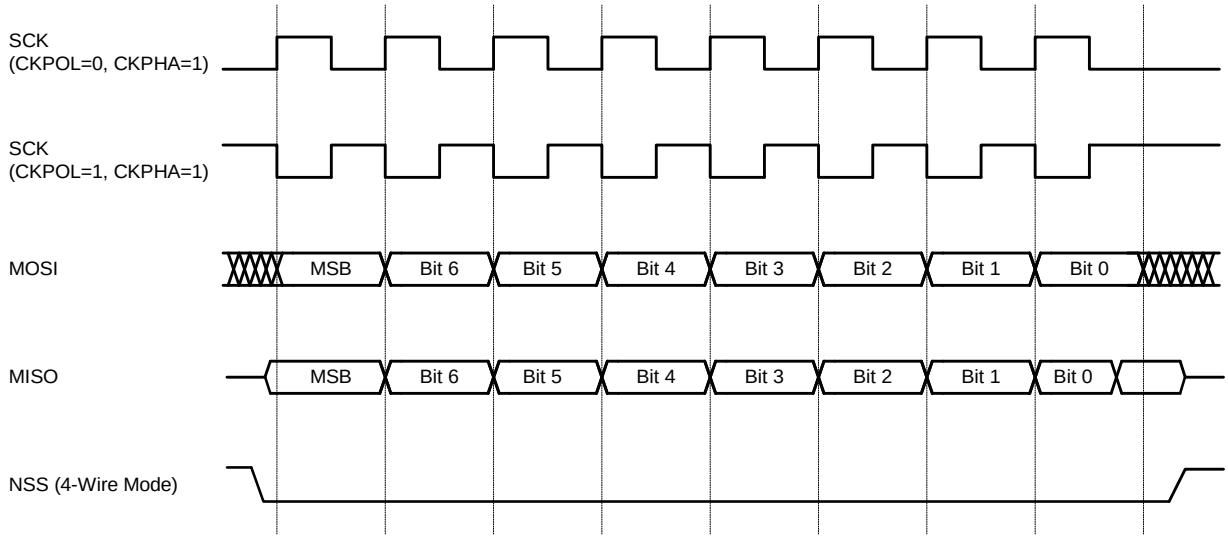


Figure 20.7. Slave Mode Data/Clock Timing (CKPHA = 1)

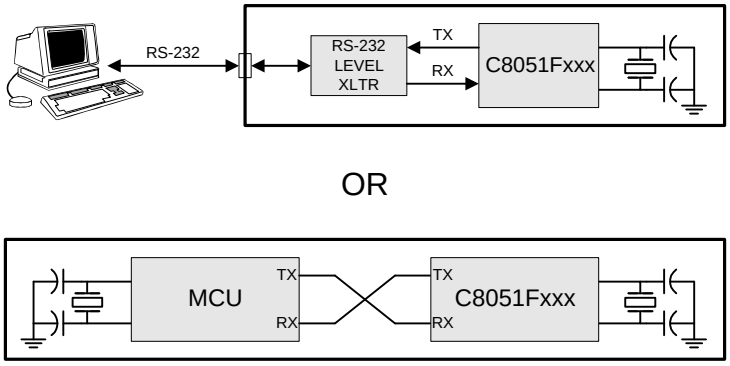


Figure 21.6. UART0 Modes 1, 2, and 3 Interconnect Diagram

21.1.4. Mode 3: 9-Bit UART, Variable Baud Rate

Mode 3 uses the Mode 2 transmission protocol with the Mode 1 baud rate generation. Mode 3 operation transmits 11 bits: a start bit, 8 data bits (LSB first), a programmable ninth data bit, and a stop bit. The baud rate is derived from Timer 1 or Timer 2, 3, or 4 overflows, as defined by Equation 21.1 and Equation 21.3. Multiprocessor communications and hardware address recognition are supported, as described in **Section 21.2**.

23.2.4. Toggle Output Mode (Timer 2 and Timer 4 Only)

Timers 2 and 4 have the capability to toggle the state of their respective output port pins (T2 or T4) to produce a 50% duty cycle waveform output. The port pin state will change upon the overflow or underflow of the respective timer (depending on whether the timer is counting *up* or *down*). The toggle frequency is determined by the clock source of the timer and the values loaded into RCAPnH and RCAPnL. When counting DOWN, the auto-reload value for the timer is 0xFFFF, and underflow will occur when the value in the timer matches the value stored in RCAPnH:RCAPnL. When counting UP, the auto-reload value for the timer is RCAPnH:RCAPnL, and overflow will occur when the value in the timer transitions from 0xFFFF to the reload value.

To output a square wave, the timer is placed in reload mode (the Capture/Reload Select Bit in TMRnCN and the Timer/Counter Select Bit in TMRnCN are cleared to '0'). The timer output is enabled by setting the Timer Output Enable Bit in TMRnCF to '1'. The timer should be configured via the timer clock source and reload/underflow values such that the timer overflow/underflows at 1/2 the desired output frequency. The port pin assigned by the crossbar as the timer's output pin should be configured as a digital output (see **Section "18. Port Input/Output" on page 235**). Setting the timer's Run Bit (TRn) to '1' will start the toggle of the pin. A Read/Write of the Timer's Toggle Output State Bit (TMRnCF.2) is used to read the state of the toggle output, or to force a value of the output. This is useful when it is desired to start the toggle of a pin in a known state, or to force the pin into a desired state when the toggle mode is halted.

Equation 23.1. Square Wave Frequency (Timer 2 and Timer 4 Only)

$$F_{sq} = \frac{F_{TCLK}}{2 \times (65536 - RCAPn)}$$

SFR Definition 24.3. PCA0CPMn: PCA0 Capture/Compare Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
PWM16n	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: PCA0CPM0: 0xDA, PCA0CPM1: 0xDB, PCA0CPM2: 0xDC, PCA0CPM3: 0xDD, PCA0CPM4: 0xDE, PCA0CPM5: 0xDF

SFR Page: PCA0CPM0: page 0, PCA0CPM1: page 0, PCA0CPM2: page 0, PCA0CPM3: 0, PCA0CPM4: page 0, PCA0CPM5: page 0

Bit7: PWM16n: 16-bit Pulse Width Modulation Enable
This bit selects 16-bit mode when Pulse Width Modulation mode is enabled (PWMn = 1).
0: 8-bit PWM selected.
1: 16-bit PWM selected.

Bit6: ECOMn: Comparator Function Enable.
This bit enables/disables the comparator function for PCA0 module n.
0: Disabled.
1: Enabled.

Bit5: CAPPn: Capture Positive Function Enable.
This bit enables/disables the positive edge capture for PCA0 module n.
0: Disabled.
1: Enabled.

Bit4: CAPNn: Capture Negative Function Enable.
This bit enables/disables the negative edge capture for PCA0 module n.
0: Disabled.
1: Enabled.

Bit3: MATn: Match Function Enable.
This bit enables/disables the match function for PCA0 module n. When enabled, matches of the PCA0 counter with a module's capture/compare register cause the CCFn bit in PCA0MD register to be set to logic 1.
0: Disabled.
1: Enabled.

Bit2: TOGn: Toggle Function Enable.
This bit enables/disables the toggle function for PCA0 module n. When enabled, matches of the PCA0 counter with a module's capture/compare register cause the logic level on the CEXn pin to toggle. If the PWMn bit is also set to logic 1, the module operates in Frequency Output Mode.
0: Disabled.
1: Enabled.

Bit1: PWMn: Pulse Width Modulation Mode Enable.
This bit enables/disables the PWM function for PCA0 module n. When enabled, a pulse width modulated signal is output on the CEXn pin. 8-bit PWM is used if PWM16n is logic 0; 16-bit mode is used if PWM16n logic 1. If the TOGn bit is also set, the module operates in Frequency Output Mode.
0: Disabled.
1: Enabled.

Bit0: ECCFn: Capture/Compare Flag Interrupt Enable.
This bit sets the masking of the Capture/Compare Flag (CCFn) interrupt.
0: Disable CCFn interrupts.
1: Enable a Capture/Compare Flag interrupt request when CCFn is set.

25.2. Flash Programming Commands

The Flash memory can be programmed directly over the JTAG interface using the Flash Control, Flash Data, Flash Address, and Flash Scale registers. These Indirect Data Registers are accessed via the JTAG Instruction Register. Read and write operations on indirect data registers are performed by first setting the appropriate DR address in the IR register. Each read or write is then initiated by writing the appropriate Indirect Operation Code (IndOpCode) to the selected data register. Incoming commands to this register have the following format:

19:18	17:0
IndOpCode	WriteData

IndOpCode: These bit set the operation to perform according to the following table:

IndOpCode	Operation
0x	Poll
10	Read
11	Write

The Poll operation is used to check the Busy bit as described below. Although a Capture-DR is performed, no Update-DR is allowed for the Poll operation. Since updates are disabled, polling can be accomplished by shifting in/out a single bit.

The Read operation initiates a read from the register addressed by the DRAddress. Reads can be initiated by shifting only 2 bits into the indirect register. After the read operation is initiated, polling of the Busy bit must be performed to determine when the operation is complete.

The write operation initiates a write of WriteData to the register addressed by DRAddress. Registers of any width up to 18 bits can be written. If the register to be written contains fewer than 18 bits, the data in WriteData should be left-justified, i.e. its MSB should occupy bit 17 above. This allows shorter registers to be written in fewer JTAG clock cycles. For example, an 8-bit register could be written by shifting only 10 bits. After a Write is initiated, the Busy bit should be polled to determine when the next operation can be initiated. The contents of the Instruction Register should not be altered while either a read or write operation is busy.

Outgoing data from the indirect Data Register has the following format:

19	18:1	0
0	ReadData	Busy

The Busy bit indicates that the current operation is not complete. It goes high when an operation is initiated and returns low when complete. Read and Write commands are ignored while Busy is high. In fact, if polling for Busy to be low will be followed by another read or write operation, JTAG writes of the next operation can be made while checking for Busy to be low. They will be ignored until Busy is read low, at which time the new operation will initiate. This bit is placed ate bit 0 to allow polling by single-bit shifts. When waiting for a Read to complete and Busy is 0, the following 18 bits can be shifted out to obtain the resulting data. ReadData is always right-justified. This allows registers shorter than 18 bits to be read using a reduced number of shifts. For example, the results from a byte-read requires 9 bit shifts (Busy + 8 bits).

DOCUMENT CHANGE LIST

Revision 1.3 to Revision 1.4

- Added new paragraph tags: SFR Definition and JTAG Register Definition.
- Product Selection Guide Table 1.1: Added RoHS-compliant ordering information.
- Overview Chapter, Figure 1.8, “On-Chip Memory Map”: Corrected on-chip XRAM size to “8192 Bytes”.
- SAR8 Chapter: Table 7.1, “ADC2 Electrical Characteristics”: Track/Hold minimum spec corrected to “300 ns”.
- SAR8 Chapter: Table 7.1, “ADC2 Electrical Characteristics”: Total Harmonic Distortion typical spec corrected to “-51 dB”.
- Oscillators Chapter, Figure 14.1, “Oscillator Diagram”: Corrected location of IOSCEN arrow.
- CIP51 Chapter, **Section 11.3**: Added note describing EA change behavior when followed by single-cycle instruction.
- CIP51 Chapter, Interrupt Summary Table: Added “SFRPAGE” column and SFRPAGE value for each interrupt source.
- CIP-51 Chapter, Figure 11.2, “Memory Map”: Corrected on-chip XRAM size to “8192 Bytes”.
- Port I/O Chapter, Crossbar Priority Figures: Character formatting problem corrected.
- Port I/O Chapter, P7MDOUT Register Description: Removed references to UART and SMBus peripherals.
- Port I/O Chapter, P3MDOUT Register Description: Corrected text to read “P3MDOUT.[7:0]”.
- Timers Chapter: References to “TnCON” corrected to read “TMRnCN”.
- PCA0 Chapter, Section 24.1: Added note about PCA0CN Register and effects of read-modify-write instructions on the CF bit.