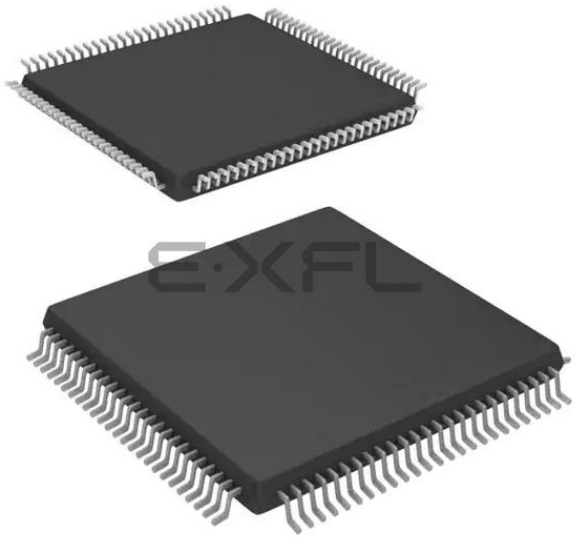

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	100MHz
Connectivity	EBI/EMI, SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	64
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8.25K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f130

List of Registers

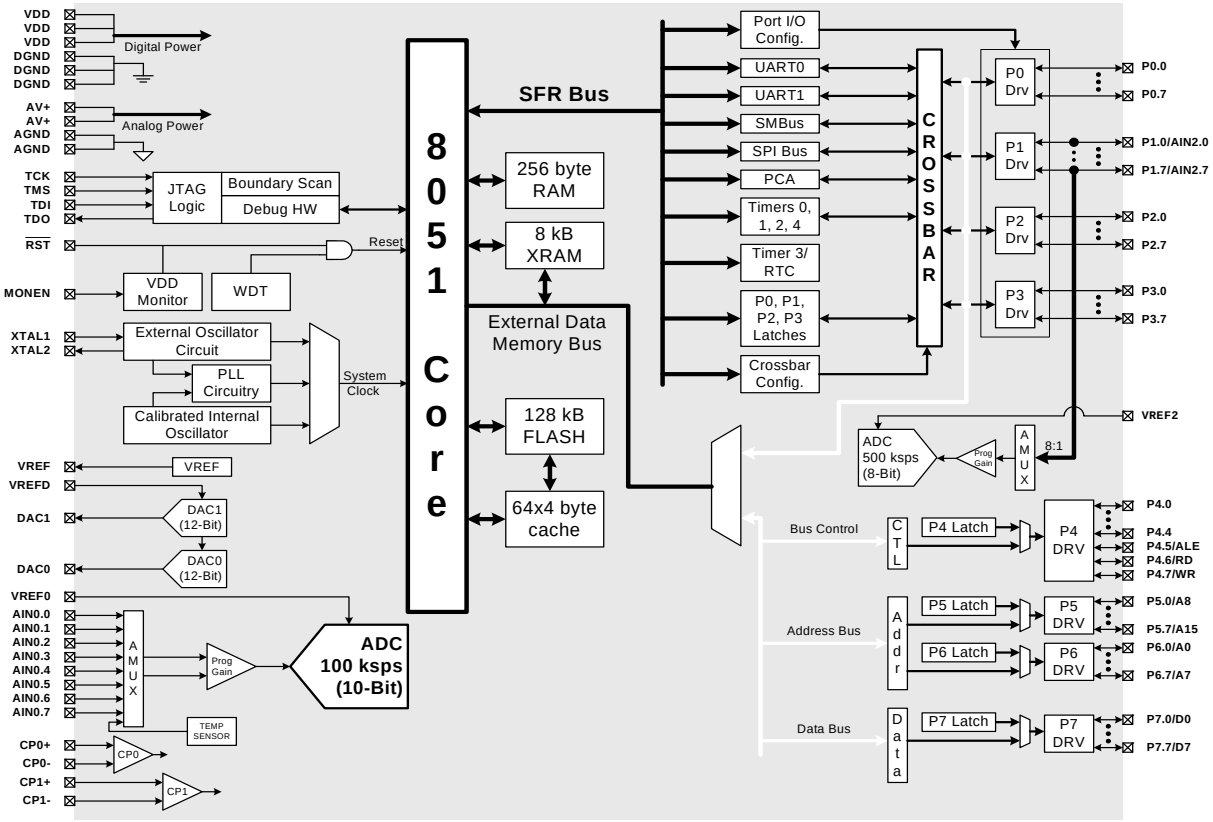

Figure 1.3. C8051F122/126 Block Diagram

4. Pinout and Package Definitions

Table 4.1. Pin Definitions

Name	Pin Numbers				Type	Description
	'F120 'F122 'F124 'F126	**'F121 'F123 'F125 'F127**	**'F130 'F132**	**'F131 'F133**		
V_{DD}	37, 64, 90	24, 41, 57	37, 64, 90	24, 41, 57		Digital Supply Voltage. Must be tied to +2.7 to +3.6 V.
DGND	38, 63, 89	25, 40, 56	38, 63, 89	25, 40, 56		Digital Ground. Must be tied to Ground.
AV+	11, 14	6	11, 14	6		Analog Supply Voltage. Must be tied to +2.7 to +3.6 V.
AGND	10, 13	5	10, 13	5		Analog Ground. Must be tied to Ground.
TMS	1	58	1	58	D In	JTAG Test Mode Select with internal pullup.
TCK	2	59	2	59	D In	JTAG Test Clock with internal pullup.
TDI	3	60	3	60	D In	JTAG Test Data Input with internal pullup. TDI is latched on the rising edge of TCK.
TDO	4	61	4	61	D Out	JTAG Test Data Output with internal pullup. Data is shifted out on TDO on the falling edge of TCK. TDO output is a tri-state driver.
$\overline{RST}$	5	62	5	62	D I/O	Device Reset. Open-drain output of internal V_{DD} monitor. Is driven low when V_{DD} is < V_{RST} and MONEN is high. An external source can initiate a system reset by driving this pin low.
XTAL1	26	17	26	17	A In	Crystal Input. This pin is the return for the internal oscillator circuit for a crystal or ceramic resonator. For a precision internal clock, connect a crystal or ceramic resonator from XTAL1 to XTAL2. If overdriven by an external CMOS clock, this becomes the system clock.
XTAL2	27	18	27	18	A Out	Crystal Output. This pin is the excitation driver for a crystal or ceramic resonator.
MONEN	28	19	28	19	D In	V_{DD} Monitor Enable. When tied high, this pin enables the internal V_{DD} monitor, which forces a system reset when V_{DD} is < V_{RST}. When tied low, the internal V_{DD} monitor is disabled. **This pin must be tied high or low.**

SFR Definition 5.3. ADC0CF: ADC0 Configuration

SFR Page: 0
SFR Address: 0xBC

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
AD0SC4	AD0SC3	AD0SC2	AD0SC1	AD0SC0	AMP0GN2	AMP0GN1	AMP0GN0	11111000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits7–3: AD0SC4–0: ADC0 SAR Conversion Clock Period Bits.
The SAR Conversion clock is derived from system clock by the following equation, where *AD0SC* refers to the 5-bit value held in AD0SC4-0, and CLK_{SAR0} refers to the desired ADC0 SAR clock (Note: the ADC0 SAR Conversion Clock should be less than or equal to 2.5 MHz).

$$AD0SC = \frac{SYSCLK}{2 \times CLK_{SAR0}} - 1 \qquad (AD0SC > 00000\text{b})$$

When the AD0SC bits are equal to 00000b, the SAR Conversion clock is equal to SYSCLK to facilitate faster ADC conversions at slower SYSCLK speeds.

Bits2–0: AMP0GN2–0: ADC0 Internal Amplifier Gain (PGA).
000: Gain = 1
001: Gain = 2
010: Gain = 4
011: Gain = 8
10x: Gain = 16
11x: Gain = 0.5

SFR Definition 6.4. ADC0CN: ADC0 Control

SFR Page: 0
SFR Address: 0xE8 (bit addressable)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
AD0EN	AD0TM	AD0INT	AD0BUSY	AD0CM1	AD0CM0	AD0WINT	AD0LJST	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bit7: AD0EN: ADC0 Enable Bit.
0: ADC0 Disabled. ADC0 is in low-power shutdown.
1: ADC0 Enabled. ADC0 is active and ready for data conversions.

Bit6: AD0TM: ADC Track Mode Bit.
0: When the ADC is enabled, tracking is continuous unless a conversion is in process.
1: Tracking Defined by ADCM1-0 bits.

Bit5: AD0INT: ADC0 Conversion Complete Interrupt Flag.
This flag must be cleared by software.
0: ADC0 has not completed a data conversion since the last time this flag was cleared.
1: ADC0 has completed a data conversion.

Bit4: AD0BUSY: ADC0 Busy Bit.
Read:
0: ADC0 Conversion is complete or a conversion is not currently in progress. AD0INT is set to logic 1 on the falling edge of AD0BUSY.
1: ADC0 Conversion is in progress.
Write:
0: No Effect.
1: Initiates ADC0 Conversion if AD0CM1-0 = 00b.

Bits3–2: AD0CM1–0: ADC0 Start of Conversion Mode Select.
If AD0TM = 0:
00: ADC0 conversion initiated on every write of ‘1’ to AD0BUSY.
01: ADC0 conversion initiated on overflow of Timer 3.
10: ADC0 conversion initiated on rising edge of external CNVSTR0.
11: ADC0 conversion initiated on overflow of Timer 2.
If AD0TM = 1:
00: Tracking starts with the write of ‘1’ to AD0BUSY and lasts for 3 SAR clocks, followed by conversion.
01: Tracking started by the overflow of Timer 3 and lasts for 3 SAR clocks, followed by conversion.
10: ADC0 tracks only when CNVSTR0 input is logic low; conversion starts on rising CNVSTR0 edge.
11: Tracking started by the overflow of Timer 2 and lasts for 3 SAR clocks, followed by conversion.

Bit1: AD0WINT: ADC0 Window Compare Interrupt Flag.
This bit must be cleared by software.
0: ADC0 Window Comparison Data match has not occurred since this flag was last cleared.
1: ADC0 Window Comparison Data match has occurred.

Bit0: AD0LJST: ADC0 Left Justify Select.
0: Data in ADC0H:ADC0L registers are right-justified.
1: Data in ADC0H:ADC0L registers are left-justified.

SFR Definition 7.3. ADC2CF: ADC2 Configuration

SFR Page: 2
SFR Address: 0xBC

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
AD2SC4	AD2SC3	AD2SC2	AD2SC1	AD2SC0	-	AMP2GN1	AMP2GN0	11111000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits7–3: AD2SC4–0: ADC2 SAR Conversion Clock Period Bits.
SAR Conversion clock is derived from system clock by the following equation, where *AD2SC* refers to the 5-bit value held in AD2SC4–0, and CLK_{SAR2} refers to the desired ADC2 SAR clock (Note: the ADC2 SAR Conversion Clock should be less than or equal to 6 MHz).

$$AD2SC = \frac{SYSCLK}{CLK_{SAR2}} - 1$$

Bit2: UNUSED. Read = 0b; Write = don't care.
Bits1–0: AMP2GN1–0: ADC2 Internal Amplifier Gain (PGA).
00: Gain = 0.5
01: Gain = 1
10: Gain = 2
11: Gain = 4

SFR Definition 8.1. DAC0H: DAC0 High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xD3
SFR Page: 0

Bits7–0: DAC0 Data Word Most Significant Byte.

SFR Definition 8.2. DAC0L: DAC0 Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xD2
SFR Page: 0

Bits7–0: DAC0 Data Word Least Significant Byte.

SFR Definition 10.4. CPT1MD: Comparator1 Mode Selection

SFR Page: 2
SFR Address: 0x89

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	CP1RIE	CP1FIE	-	-	CP1MD1	CP1MD0	00000010
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits7–6: UNUSED. Read = 00b, Write = don't care.
Bit 5: CP1RIE: Comparator 1 Rising-Edge Interrupt Enable Bit.
0: Comparator 1 rising-edge interrupt disabled.
1: Comparator 1 rising-edge interrupt enabled.
Bit 4: CP1FIE: Comparator 0 Falling-Edge Interrupt Enable Bit.
0: Comparator 1 falling-edge interrupt disabled.
1: Comparator 1 falling-edge interrupt enabled.
Bits3–2: UNUSED. Read = 00b, Write = don't care.
Bits1–0: CP1MD1–CP1MD0: Comparator1 Mode Select
These bits select the response time for Comparator1.

Mode	CP0MD1	CP0MD0	Notes
0	0	0	Fastest Response Time
1	0	1	—
2	1	0	—
3	1	1	Lowest Power Consumption

SFR Definition 12.4. MAC0AL: MAC0 A Low Byte

R	R	R	R	R	R	R	R	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xC1
SFR Page: 3

Bits 7–0: Low Byte (bits 7–0) of MAC0 A Register.

SFR Definition 12.5. MAC0BH: MAC0 B High Byte

R	R	R	R	R	R	R	R	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x92
SFR Page: 3

Bits 7–0: High Byte (bits 15–8) of MAC0 B Register.

SFR Definition 12.6. MAC0BL: MAC0 B Low Byte

R	R	R	R	R	R	R	R	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x91
SFR Page: 3

Bits 7–0: Low Byte (bits 7–0) of MAC0 B Register.
A write to this register initiates a Multiply or Multiply and Accumulate operation.

***Note:** The contents of this register should not be changed by software during the first MAC0 pipeline stage.

SFR Definition 14.4. OSCXCN: External Oscillator Control

R	R/W	R/W	R/W	R	R/W	R/W	R/W	Reset Value
XTLVLD	XOSCMD2	XOSCMD1	XOSCMD0	-	XFCN2	XFCN1	XFCN0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x8C
SFR Page: F

Bit7: XTLVLD: Crystal Oscillator Valid Flag.
(**Valid only when XOSCMD = 11x.**)
0: Crystal Oscillator is unused or not yet stable.
1: Crystal Oscillator is running and stable.

Bits6–4: XOSCMD2–0: External Oscillator Mode Bits.
00x: External Oscillator circuit off.
010: External CMOS Clock Mode (External CMOS Clock input on XTAL1 pin).
011: External CMOS Clock Mode with divide by 2 stage (External CMOS Clock input on XTAL1 pin).
10x: RC/C Oscillator Mode with divide by 2 stage.
110: Crystal Oscillator Mode.
111: Crystal Oscillator Mode with divide by 2 stage.

Bit3: RESERVED. Read = 0, Write = don't care.

Bits2–0: XFCN2–0: External Oscillator Frequency Control Bits.
000-111: see table below:

XFCN	Crystal (XOSCMD = 11x)	RC (XOSCMD = 10x)	C (XOSCMD = 10x)
000	f ≤ 32 kHz	f ≤ 25 kHz	K Factor = 0.87
001	32 kHz < f ≤ 84 kHz	25 kHz < f ≤ 50 kHz	K Factor = 2.6
010	84 kHz < f ≤ 225 kHz	50 kHz < f ≤ 100 kHz	K Factor = 7.7
011	225 kHz < f ≤ 590 kHz	100 kHz < f ≤ 200 kHz	K Factor = 22
100	590 kHz < f ≤ 1.5 MHz	200 kHz < f ≤ 400 kHz	K Factor = 65
101	1.5 MHz < f ≤ 4 MHz	400 kHz < f ≤ 800 kHz	K Factor = 180
110	4 MHz < f ≤ 10 MHz	800 kHz < f ≤ 1.6 MHz	K Factor = 664
111	10 MHz < f ≤ 30 MHz	1.6 MHz < f ≤ 3.2 MHz	K Factor = 1590

CRYSTAL MODE (Circuit from Figure 14.1, Option 1; XOSCMD = 11x)
Choose XFCN value to match crystal frequency.

RC MODE (Circuit from Figure 14.1, Option 2; XOSCMD = 10x)
Choose XFCN value to match frequency range:
f = **1.23(10^3) / (R * C)**, where
f = frequency of oscillation in MHz
C = capacitor value in pF
R = Pullup resistor value in kΩ

C MODE (Circuit from Figure 14.1, Option 3; XOSCMD = 10x)
Choose K Factor (KF) for the oscillation frequency desired:
f = **KF / (C *** V_{DD}**)**, where
f = frequency of oscillation in MHz
C = capacitor value on XTAL1, XTAL2 pins in pF
V_{DD} = Power Supply on MCU in Volts

SFR Definition 16.2. CCH0TN: Cache Tuning

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
CHMSCTL				CHALGM	CHFIXM	CHMSTH		00000100
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xA2
SFR Page: F

Bits 7–4: CHMSCTL: Cache Miss Penalty Accumulator (Bits 4–1).
These are bits 4-1 of the Cache Miss Penalty Accumulator. To read these bits, they must first be latched by reading the CHMSCTH bits in the CCH0MA Register (See SFR Definition 16.4).

Bit 3: CHALGM: Cache Algorithm Select.
This bit selects the cache replacement algorithm.
0: Cache uses Rebound algorithm.
1: Cache uses Pseudo-random algorithm.

Bit 2: CHFIXM: Cache Fix MOVC Enable.
This bit forces MOVC writes to the cache memory to use slot 0.
0: MOVC data is written according to the current algorithm selected by the CHALGM bit.
1: MOVC data is always written to cache slot 0.

Bits 1–0: CHMSTH: Cache Miss Penalty Threshold.
These bits determine when missed instruction data will be cached.
If data takes longer than CHMSTH clocks to obtain, it will be cached.

SFR Definition 16.3. CCH0LC: Cache Lock Control

R/W	R/W	R	R	R	R	R	R	Reset Value
CHPUSH	CHPOP	CHSLOT						00111110
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xA3
SFR Page: F

Bit 7: CHPUSH: Cache Push Enable.
This bit enables cache push operations, which will lock information in cache slots using MOVC instructions.
0: Cache push operations are disabled.
1: Cache push operations are enabled. When a MOVC read is executed, the requested 4-byte segment containing the data is locked into the cache at the location indicated by CHSLOT, and CHSLOT is decremented.
Note that no more than 61 cache slots should be locked at one time, since the entire cache will be unlocked when CHSLOT is equal to 0.

Bit 6: CHPOP: Cache Pop.
Writing a ‘1’ to this bit will increment CHSLOT and then unlock that location. This bit always reads ‘0’. Note that Cache Pop operations should not be performed while CHSLOT = 111110b. “Pop”ing more Cache slots than have been “Push”ed will have indeterminate results on the Cache performance.

Bits 5–0: CHSLOT: Cache Slot Pointer.
These read-only bits are the pointer into the cache lock stack. Locations above CHSLOT are locked, and will not be changed by the processor, except when CHSLOT equals 0.

SFR Definition 17.2. EMI0CF: External Memory Configuration

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	PRTSEL	EMD2	EMD1	EMD0	EALE1	EALE0	00000011
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xA3
SFR Page: 0

Bits7–6: Unused. Read = 00b. Write = don't care.

Bit5: PRTSEL: EMIF Port Select.
0: EMIF active on P0–P3.
1: EMIF active on P4–P7.

Bit4: EMD2: EMIF Multiplex Mode Select.
0: EMIF operates in multiplexed address/data mode.
1: EMIF operates in non-multiplexed mode (separate address and data pins).

Bits3–2: EMD1-0: EMIF Operating Mode Select.
These bits control the operating mode of the External Memory Interface.
00: Internal Only: MOVX accesses on-chip XRAM only. All effective addresses alias to on-chip memory space.
01: Split Mode without Bank Select: Accesses below the 8 k boundary are directed on-chip. Accesses above the 8 k boundary are directed off-chip. 8-bit off-chip MOVX operations use the current contents of the Address High port latches to resolve upper address byte. Note that in order to access off-chip space, EMI0CN must be set to a page that is not contained in the on-chip address space.
10: Split Mode with Bank Select: Accesses below the 8 k boundary are directed on-chip. Accesses above the 8k boundary are directed off-chip. 8-bit off-chip MOVX operations use the contents of EMI0CN to determine the high-byte of the address.
11: External Only: MOVX accesses off-chip XRAM only. On-chip XRAM is not visible to the CPU.

Bits1–0: EALE1–0: ALE Pulse-Width Select Bits (only has effect when EMD2 = 0).
00: ALE high and ALE low pulse width = 1 SYSCLK cycle.
01: ALE high and ALE low pulse width = 2 SYSCLK cycles.
10: ALE high and ALE low pulse width = 3 SYSCLK cycles.
11: ALE high and ALE low pulse width = 4 SYSCLK cycles.

SFR Definition 18.10. P2MDOUT: Port2 Output Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xA6
SFR Page: F

Bits7–0: P2MDOUT.[7:0]: Port2 Output Mode Bits.
0: Port Pin output mode is configured as Open-Drain.
1: Port Pin output mode is configured as Push-Pull.

Note: SDA, SCL, and RX0 (when UART0 is in Mode 0) and RX1 (when UART1 is in Mode 0) are always configured as Open-Drain when they appear on Port pins.

SFR Definition 18.11. P3: Port3 Data

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0xB0
SFR Page: All Pages

Bits7–0: P3.[7:0]: Port3 Output Latch Bits.
(Write - Output appears on I/O pins per XBR0, XBR1, and XBR2 Registers)
0: Logic Low Output.
1: Logic High Output (open if corresponding P3MDOUT.n bit = 0).
(Read - Regardless of XBR0, XBR1, and XBR2 Register settings).
0: P3.n pin is logic low.
1: P3.n pin is logic high.

Note: P3.[7:0] can be driven by the External Data Memory Interface (as AD[7:0] in Multiplexed mode, or as D[7:0] in Non-multiplexed mode). See **Section “17. External Data Memory Interface and On-Chip XRAM” on page 219** for more information about the External Memory Interface.

19.4.2. Clock Rate Register

SFR Definition 19.2. SMB0CR: SMBus0 Clock Rate

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xCF
SFR Page: 0

Bits7–0: SMB0CR.[7:0]: SMBus0 Clock Rate Preset
The SMB0CR Clock Rate register controls the frequency of the serial clock SCL in master mode. The 8-bit word stored in the SMB0CR Register preloads a dedicated 8-bit timer. The timer counts up, and when it rolls over to 0x00, the SCL logic state toggles.

The SMB0CR setting should be bounded by the following equation , where *SMB0CR* is the unsigned 8-bit value in register SMB0CR, and *SYSCLK* is the system clock frequency in MHz:

$$SMB0CR < \left(288 - 0.85 \cdot \frac{SYSCLK}{4}\right) / 1.125$$

The resulting SCL signal high and low times are given by the following equations, where SYSCLK is the system clock frequency in Hz:

$$T_{LOW} = 4 \times (256 - SMB0CR) / SYSCLK$$

$$T_{HIGH} \cong 4 \times (258 - SMB0CR) / SYSCLK + 625ns$$

Using the same value of SMB0CR from above, the Bus Free Timeout period is given in the following equation:

$$T_{BFT} \cong 10 \times \frac{4 \times (256 - SMB0CR) + 1}{SYSCLK}$$

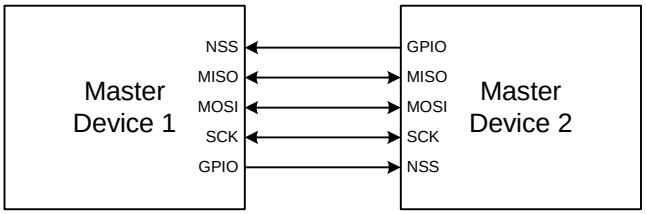

Figure 20.2. Multiple-Master Mode Connection Diagram

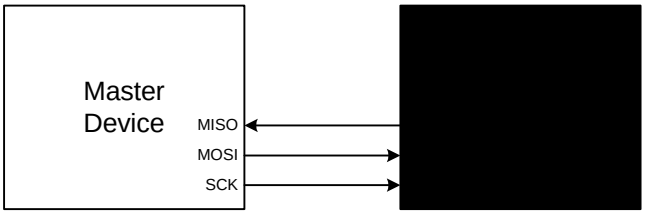

Figure 20.3. 3-Wire Single Master and Slave Mode Connection Diagram

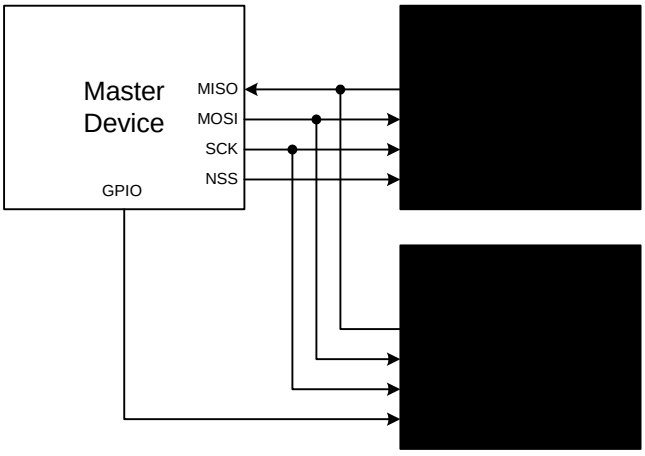

Figure 20.4. 4-Wire Single Master and Slave Mode Connection Diagram

Table 21.2. Oscillator Frequencies for Standard Baud Rates

System Clock Frequency (MHz)	Divide Factor	Timer 1 Reload Value[1]	Timer 2, 3, or 4 Reload Value	Resulting Baud Rate (Hz)[2]
100.0	864	0xCA	0xFFCA	115200 (115741)
99.5328	864	0xCA	0xFFCA	115200
50.0	432	0xE5	0xFFE5	115200 (115741)
49.7664	432	0xE5	0xFFE5	115200
24.0	208	0xF3	0xFFF3	115200 (115384)
22.1184	192	0xF4	0xFFF4	115200
18.432	160	0xF6	0xFFF6	115200
11.0592	96	0xFA	0xFFFA	115200
3.6864	32	0xFE	0xFFFE	115200
1.8432	16	0xFF	0xFFFF	115200
100.0	3472	0x27	0xFF27	28800 (28802)
99.5328	3456	0x28	0xFF28	28800
50.0	1744	0x93	0xFF93	28800 (28670)
49.7664	1728	0x94	0xFF94	28800
24.0	832	0xCC	0xFFCC	28800 (28846)
22.1184	768	0xD0	0xFFD0	28800
18.432	640	0xD8	0xFFD8	28800
11.0592	348	0xE8	0xFFE8	28800
3.6864	128	0xF8	0xFFF8	28800
1.8432	64	0xFC	0xFFFC	28800
100.0	10416	-	0xFD75	9600 (9601)
99.5328	10368	-	0xFD78	9600
50.0	5216	-	0xFEBA	9600 (9586)
49.7664	5184	-	0xFEBC	9600
24.0	2496	0x64	0xFF64	9600 (9615)
22.1184	2304	0x70	0xFF70	9600
18.432	1920	0x88	0xFF88	9600
11.0592	1152	0xB8	0xFFB8	9600
3.6864	384	0xE8	0xFFE8	9600
1.8432	192	0xF4	0xFFF4	9600

Notes:

1. Assumes SMOD0 = 1 and T1M = 1.
2. Numbers in parenthesis show the actual baud rate.

SFR Definition 23.1. TCON: Timer Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0x88
SFR Page: 0

Bit7: TF1: Timer 1 Overflow Flag.
Set by hardware when Timer 1 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 1 interrupt service routine.
0: No Timer 1 overflow detected.
1: Timer 1 has overflowed.

Bit6: TR1: Timer 1 Run Control.
0: Timer 1 disabled.
1: Timer 1 enabled.

Bit5: TF0: Timer 0 Overflow Flag.
Set by hardware when Timer 0 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 0 interrupt service routine.
0: No Timer 0 overflow detected.
1: Timer 0 has overflowed.

Bit4: TR0: Timer 0 Run Control.
0: Timer 0 disabled.
1: Timer 0 enabled.

Bit3: IE1: External Interrupt 1.
This flag is set by hardware when an edge/level of type defined by IT1 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 1 service routine if IT1 = 1. This flag is the inverse of the /INT1 signal.

Bit2: IT1: Interrupt 1 Type Select.
This bit selects whether the configured /INT1 interrupt will be falling-edge sensitive or active-low.
0: /INT1 is level triggered, active-low.
1: /INT1 is edge triggered, falling-edge.

Bit1: IE0: External Interrupt 0.
This flag is set by hardware when an edge/level of type defined by IT0 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 0 service routine if IT0 = 1. This flag is the inverse of the /INT0 signal.

Bit0: IT0: Interrupt 0 Type Select.
This bit selects whether the configured /INT0 interrupt will be falling-edge sensitive or active-low.
0: /INT0 is level triggered, active logic-low.
1: /INT0 is edge triggered, falling-edge.

SFR Definition 23.13. TMRnH Timer 2, 3, and 4 High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: TMR2H: 0xCD; TMR3H: 0xCD; TMR4H: 0xCD

SFR Page: TMR2H: page 0; TMR3H: page 1; TMR4H: page 2

Bits 7–0: TH2, 3, and 4: Timer 2, 3, and 4 High Byte.
The TH2, 3, and 4 register contains the high byte of the 16-bit Timer 2, 3, and 4

SFR Definition 24.4. PCA0L: PCA0 Counter/Timer Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xF9
SFR Page: 0

Bits 7–0: PCA0L: PCA0 Counter/Timer Low Byte.
The PCA0L register holds the low byte (LSB) of the 16-bit PCA0 Counter/Timer.

SFR Definition 24.5. PCA0H: PCA0 Counter/Timer High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xFA
SFR Page: 0

Bits 7–0: PCA0H: PCA0 Counter/Timer High Byte.
The PCA0H register holds the high byte (MSB) of the 16-bit PCA0 Counter/Timer.

SFR Definition 24.6. PCA0CPLn: PCA0 Capture Module Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: PCA0CPL0: 0xFB, PCA0CPL1: 0xFD, PCA0CPL2: 0xE9, PCA0CPL3: 0xEB, PCA0CPL4: 0xED, PCA0CPL5: 0xE1

SFR Page: PCA0CPL0: page 0, PCA0CPL1: page 0, PCA0CPL2: page 0, PCA0CPL3: page 0, PCA0CPL4: page 0, PCA0CPL5: page 0

Bits7–0: PCA0CPLn: PCA0 Capture Module Low Byte.
The PCA0CPLn register holds the low byte (LSB) of the 16-bit capture module n.