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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	68000
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	20MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-55°C ~ 125°C (TC)
Security Features	-
Package / Case	132-BCQFP
Supplier Device Package	132-CQFP (24.13x24.13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts68020mf1-20

Table 1. Signal Index

Signal Name	Mnemonic	Function
Address Bus	A0-A31	32-bit Address Bus Used to address any of 4, 294, 967, 296 bytes.
Data Bus	D0-D31	32-bit Data Bus Used to Transfer 8, 16, 24 or 32 bits of Data Per Bus Cycle.
Function Codes	FC0-FC2	3-bit Function Case Used to Identify the Address Space of Each Bus Cycle.
Size	SIZ0/SIZ1	Indicates the Number of Bytes Remaining to be Transferred for this Cycle. These Signals, Together with A0 And A1, Define the Active Sections of the Data Bus.
Read-Modify-Write Cycle	$\overline{RMC}$	Provides an Indicator that the Current Bus Cycle is Part of an Indivisibleread-modify-write Operation.
External Cycle Start	$\overline{ECS}$	Provides an Indication that a Bus Cycle is Beginning.
Operand Cycle Start	$\overline{OCS}$	Identical Operation to that of ECS Except that OCS Is Asserted Only During the First Bus Cycle of an Operand Transfer.
Address Strobe	$\overline{AS}$	Indicates that a Valid Address is on The Bus.
Data Strobe	$\overline{DS}$	Indicates that Valid Data is to be Placed on the Data Bus by an External Device or has been Laced on the Data Bus by the TS68020.
Read/Write	R/$\overline{W}$	Defines the Bus Transfer as an MPU Read or Write.
Data Buffer Enable	$\overline{DBEN}$	Provides an Enable Signal for External Data Buffers.
Data Transfer and Size Acknowledge	$\overline{DSACK0}$/$\overline{DSACK1}$	Bus Response Signals that Indicate the Requested Data Transfer Operation is Completed. In Addition, these Two Lines Indicate the Size of the External Bus Port on a Cycle-by-cycle Basis.
Cache Disable	$\overline{CDIS}$	Dynamically Disables the On-chip Cache to Assist Emulator Support.
Interrupt Priority Level	$\overline{IPL0}$-$\overline{IPL2}$	Provides an Encoded Interrupt Level to the Processor.
Autovector	$\overline{AVEC}$	Requests an Autovector During an Interrupt Acknowledge Cycle.
Interrupt Pending	$\overline{IPEND}$	Indicates that an Interrupt is Pending.
Bus Request	$\overline{BR}$	Indicates that an External Device Requires Bus Mastership.
Bus Grant	$\overline{BG}$	Indicates that an External Device may Assume Bus Mastership.
Bus Grant Acknowledge	$\overline{BGACK}$	Indicates that an External Device has Assumed Bus Mastership.
Reset	$\overline{RESET}$	System Reset.
Halt	$\overline{HALT}$	Indicates that the Processor Should Suspend Bus Activity.
Bus Error	$\overline{BERR}$	Indicates an Invalid or Illegal Bus Operation is Being Attempted.
Clock	CLK	Clock Input to the Processor.
Power Supply	V_{CC}	+5-volt ± 10% Power Supply.
Ground	GND	Ground Connection.

Electrical Characteristics

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{CC}	Supply Voltage		-0.3	+7.0	V
V_I	Input Voltage		-0.5	+7.0	V
P_{dmax}	Max Power Dissipation	T_{case} = -55°C		2.0	W
		T_{case} = +125°C		1.9	W
T_{case}	Operating Temperature	M Suffix	-55	+125	°C
		V Suffix	-40	+85	°C
T_{stg}	Storage Temperature		-55	+150	°C
T_{leads}	Lead Temperature	Max 5 Sec. Soldering		+270	°C

Table 3. Recommended Condition of Use

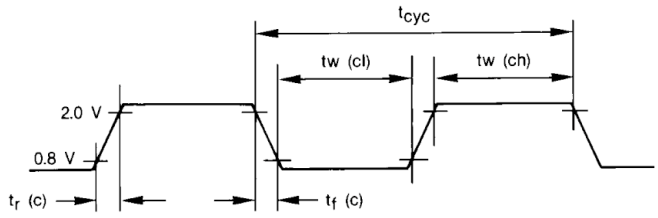
Unless otherwise stated, all voltages are referenced to the reference terminal (see Table 1).

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		4.5	5.5	V
V_{IL}	Low Level Input Voltage		-0.3	0.5	V
V_{IH}	High Level Input Voltage		2.4	5.25	V
T_{case}	Operating Temperature		-55	+125	°C
R_L	Value of Output Load Resistance		(1)		Ω
C_L	Output Loading Capacitance			(1)	pF
$t_r(c)$–$t_f(c)$	Clock Rise Time (See Figure 5)	68020-16		5	ns
		68020-20		5	
		68020-25		4	
f_c	Clock Frequency (See Figure 5)	68020-16	8	16.67	MHz
		68020-20	12.5	20	
		68020-25	12.5	25	
t_{cyc}	Cycle Time (see Figure 5)	68020-16	60	125	ns
		68020-20	50	80	
		68020-25	40	80	
$t_W(CL)$	Clock Pulse Width Low (See Figure 5)	68020-16	24	95	ns
		68020-20	20	54	
		68020-25	19	61	
$t_W(CH)$	Clock Pulse Width High (See Figure 5)	68020-16	24	95	ns
		68020-20	20	50	
		68020-25	19	61	

Note: 1. Load network number 1 to 4 as specified (Table 7) gives the maximum loading of the relevant output.

This device contains protective circuitry against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

Figure 5. Clock Input Timing Diagram



Note: Timing measurements are referenced to and from a low voltage of 0.8V and a high voltage of 2.0V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8V and 2.0V.

Table 4. Thermal Characteristics at 25°C

Package	Symbol	Parameter	Value	Unit
PGA 114	θ_{JA}	Thermal Resistance - Ceramic Junction to Ambient	26	°C/W
	θ_{JC}	Thermal Resistance - Ceramic Junction to Case	5	°C/W
CQFP 132	θ_{JA}	Thermal Resistance - Ceramic Junction to Ambient	34	°C/W
	θ_{JC}	Thermal Resistance - Ceramic Junction to Case	2	°C/W

Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \cdot V_{CC}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K + (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273) + \theta_{JA} \cdot P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part K can be determined from equation **(3)** by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations **(1)** and **(2)** iterativley for any value of T_A.

Table 6. Dynamic Electrical Characteristics (Continued)

Symbol	Parameter	Interval Number	68020-16		68020-20		68020-25		Unit	Notes
			Min	Max	Min	Max	Min	Max		
f	Frequency of Operation		8.0	16.67	12.5	20.0	12.5	25	MHz	
t_{RADC}	R/W Asserted to Data Bus Impedance Change	55	30		25		20			(11)
t_{HRPW}	$\overline{RESET}$ Pulse Width (Reset Instruction)	56	512		512		512		Clks	(11)
t_{BNHN}	$\overline{BERR}$ Negated to $\overline{HALT}$ Negated (Rerun)	57	0		0		0		ns	(11)
t_{GANBD}	$\overline{BGACK}$ Negated to Bus Driven	58	1		1		1		Clks	(10)(11)
t_{GNBD}	$\overline{BG}$ Negated to Bus Driven	59	1		1		1		Clks	(10)(11)

Notes:
1. This number can be reduced to 5 nanoseconds if the strobes have equal loads.
2. If the asynchronous setup time (= 47) requirements are satisfied, the DSACKx low to data setup time (= 31) and $\overline{DSACKx}$ low to $\overline{BERR}$ low setup time (= 48) can be ignored. The data must only satisfy the data in to clock low setup time (= 27) for the following clock cycle, $\overline{BERR}$ must only satisfy the late $\overline{BERR}$ low to clock setup time (= 27) for the following clock cycle.
3. This parameter specifies the maximum allowable skew between $\overline{DSACK0}$ to $\overline{DSACK1}$ asserted or $\overline{DSACK1}$ to $\overline{DSACK0}$ asserted pattern = 47 must be met by $\overline{DSACK0}$ and $\overline{DSACK1}$.
4. In the absence of $\overline{DSACKx}$, $\overline{BERR}$ is an asynchronous input using the asynchronous input setup time (= 47).
5. $\overline{DBEN}$ may stay asserted on consecutive write cycles.
6. Actual value depends on the clock input waveform.
7. This pattern indicates the minimum high time for $\overline{ECS}$ and $\overline{OCS}$ in the event of an internal cache hit followed immediately by a cache miss or operand cycle.
8. This specification guarantees operations with the 68881 co-processor, and defines a minimum time for DS negated to AS asserted (= 13A). Without this parameter, incorrect interpretation of = 9A and = 15 would indicate that the 68020 does not meet 68881 requirements.
9. This pattern allows the systems designer to guarantee data hold times on the output side of data buffers that have output enable signals generated with $\overline{DBEN}$.
10. Guarantees that an alternate bus master has stopped driving the bus when the 68020 regains control of the bus after an arbitration sequence.
11. Cannot be tested. Provided for system design purposes only.
12. T_{case} = -55°C and +130°C in a Power off condition under Thermal soak for 4 minutes or until thermal equilibrium. Electrical parameters are tested “instant on” 100 m sec. after power is applied.
13. All outputs unload except for load capacitance. Clock = fmax,
    LOW: $\overline{HALT}$, $\overline{RESET}$
    HIGH: $\overline{DSACK0}$, $\overline{DSACK1}$, $\overline{CDIS}$, $\overline{IPL0}$-$\overline{IPL2}$, $\overline{DBEN}$, $\overline{AVEC}$, $\overline{BERR}$.

Test Conditions Specific to the Device

Loading Network

The applicable loading network shall be defined in column “Test conditions” of Table 6, referring to the loading network number as shown in Figure 6, Figure 7, Figure 8 below.

Figure 6. RESET Test Loads

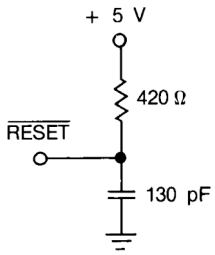


Figure 7. HALT Test Load

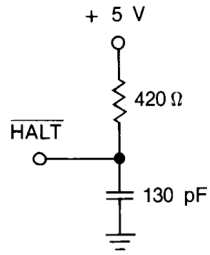


Figure 8. Test Load

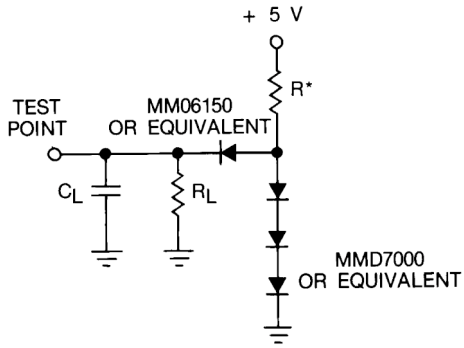
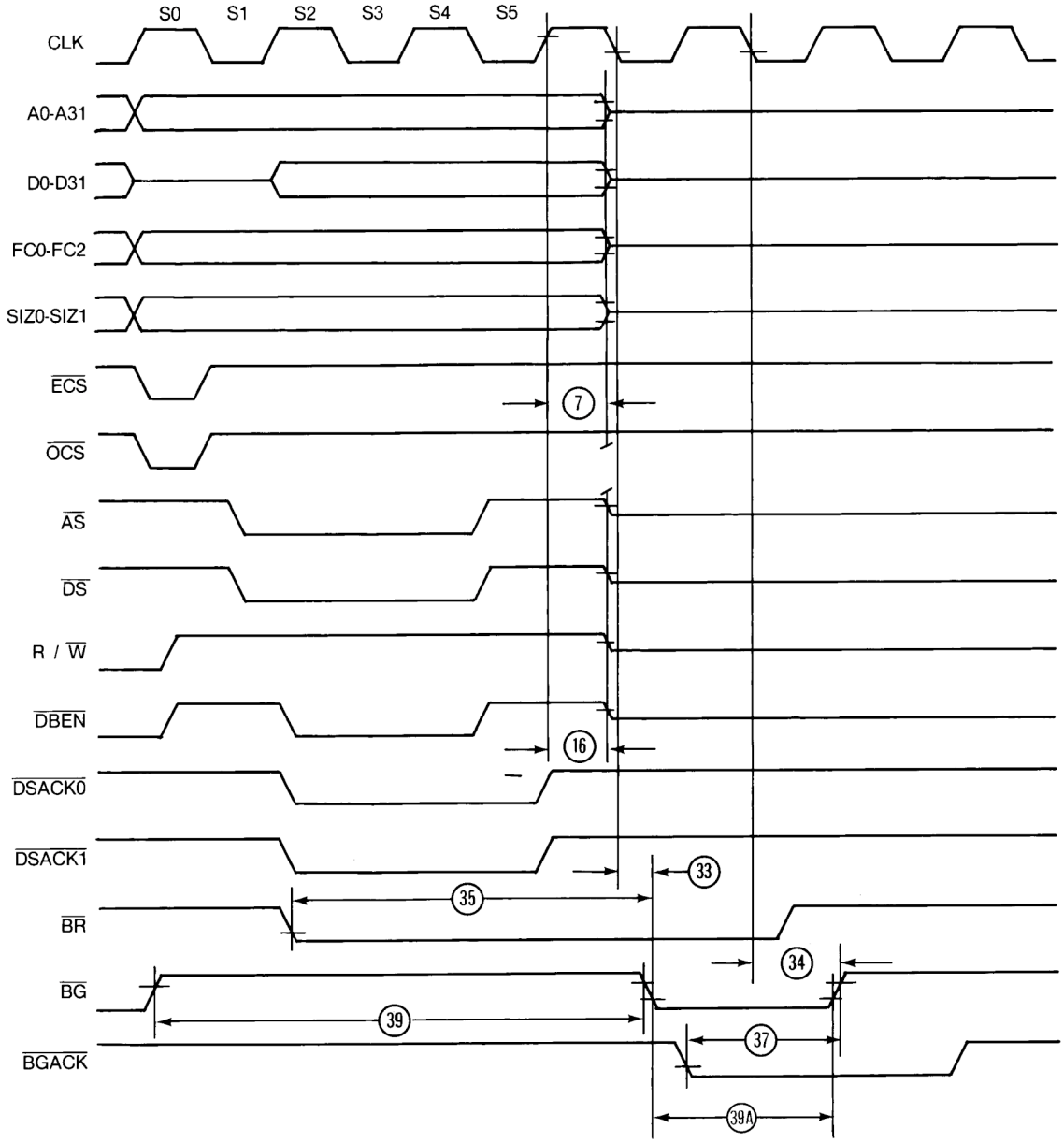


Table 7. Load Network

Load NBR	Figure	R	R_L	C_L	Output Application
1	7	2 k	6.0 k	50 pF	$\overline{OCS}$, $\overline{ECS}$
2	7	1.22 k	6.0 k	130 pF	A0-A31, D0-D31, $\overline{BG}$, FC0-FC2, SIZ0-SIZ1
3	7	0.74 k	6.0 k	130 pF	$\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, $\overline{RMC}$, $\overline{DBEN}$, $\overline{IPEND}$

Note: 1. Equivalent loading may be simulated by the tester.

Figure 11. Bus Arbitration Timing Diagram



Note: Timing measurements are referenced to and from a low voltage of 0.8V and a high voltage of 2.0V, unless otherwise noted. The voltage swing thorough this range should start outside and pass through the range such that the rise or fall will be linear between 0.8V and 2.0V.

Input and Output Signals for Dynamic Measurements

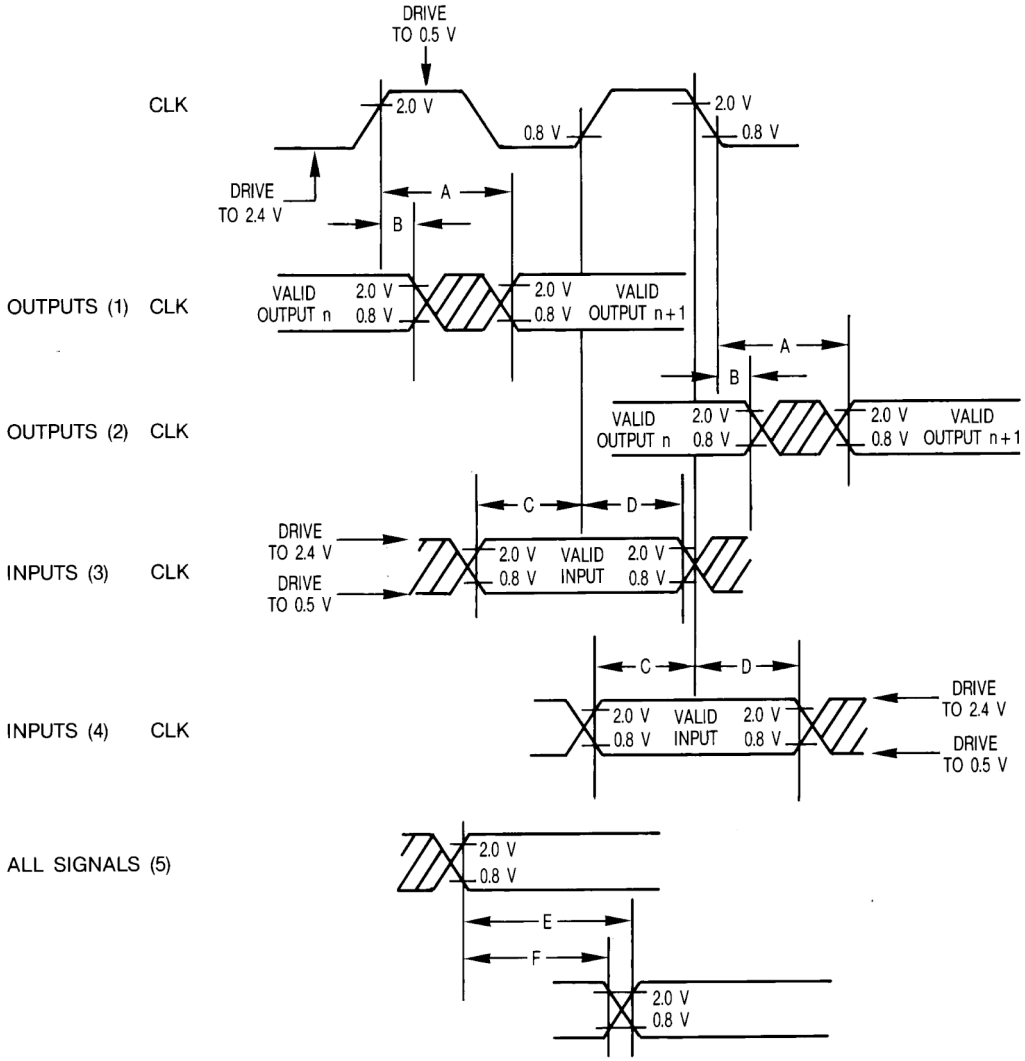
AC Electrical Specifications Definitions

The AC specifications presented consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of the TS68020 clock input and, possibly, relative to one or more other signals.

The measurement of the AC specifications is defined by the waveforms in Figure 12. In order to test the parameters guaranteed by Atmel, inputs must be driven to the voltage levels specified in Figure 12. Outputs of the TS68020 are specified with minimum and/or maximum limits, as appropriate, and are measured as shown. Inputs to the TS68020 are specified with minimum and, as appropriate, maximum setup and hold times, and are measurement as shown. Finally, the measurements for signal-to-signal specification are also shown.

Note that the testing levels used to verify conformance of the TS68020 to the AC specifications does not affect the guaranteed DC operation of the device as specified in the DC electrical characteristics.

Figure 12. Drive Levels and Test Points for AC Specification



Legend:

A) Maximum Output Delay Specification

B) Minimum Output Hold Time

C) Minimum Input Setup Time Specification

D) Minimum Input Hold Time Specification

E) Signal Valid to Signal Valid Specification (Maximum or Minimum)

F) Signal Valid to Signal Invalid Specification (Maximum or Minimum)

Notes:
1. This output timing is applicable to all parameters specified relative to the rising edge of the clock.
2. This out put timing is applicable to all parameters specified relative to the falling edge of the clock.
3. This input timing is applicable to all parameters specified relative to the falling edge of the clock.
4. This input timing is applicable to all parameters specified relative to the falling edge of the clock.
5. This timing is applicable to all parameters specified relative to the assertion/negation of another signal.

Figure 14. ECS and OCS Capacitance Derating Curve

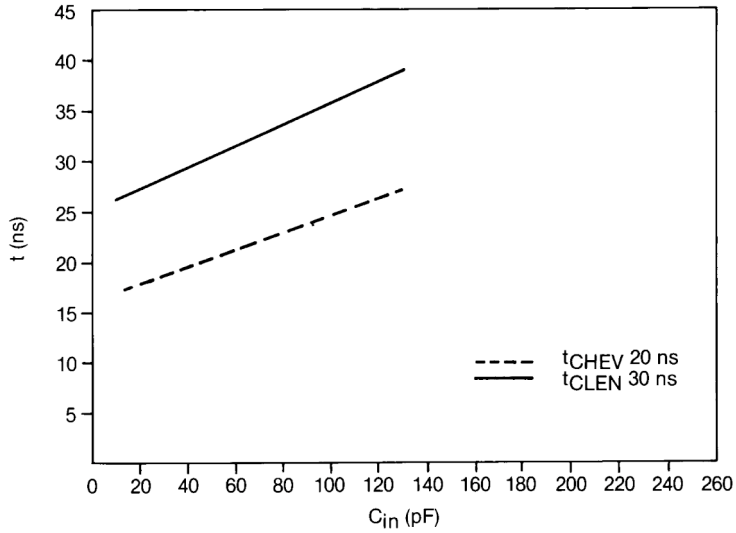


Figure 15. R/W, FC, SIZ0-SIZ1, and RMC Capacitance Derating Curve

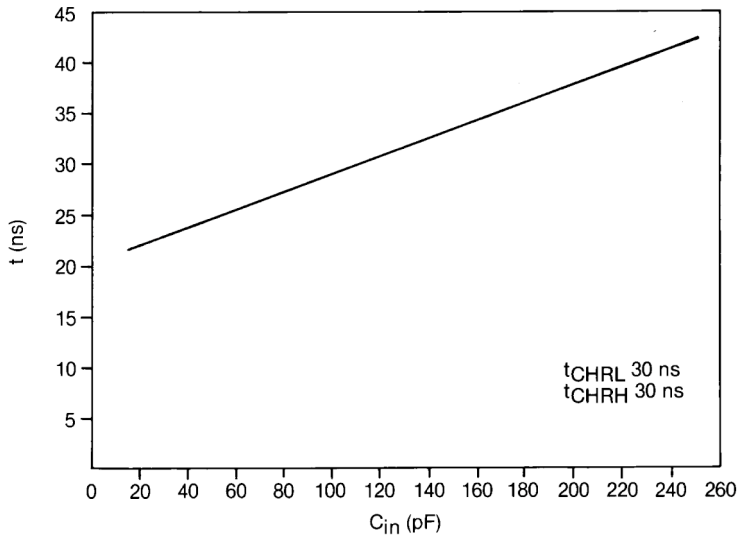


Figure 16. DS, AS, IPEND, and BG Capacitance Derating Curve

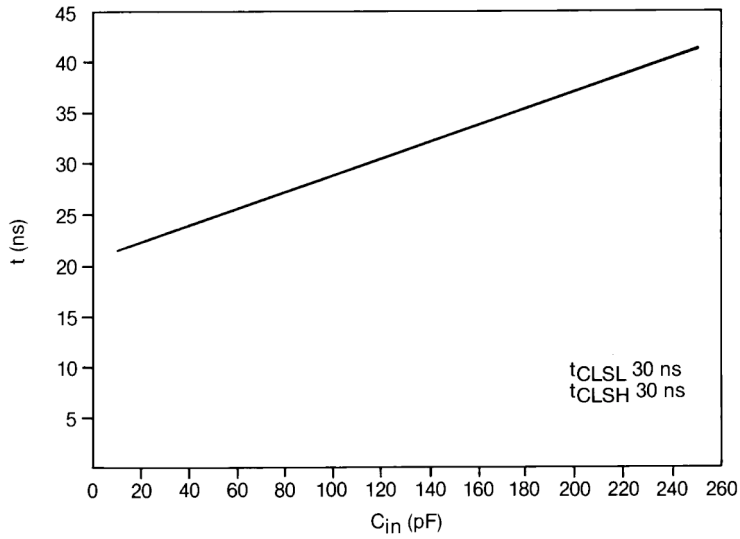


Figure 17. DBEN Capacitance Derating Curve

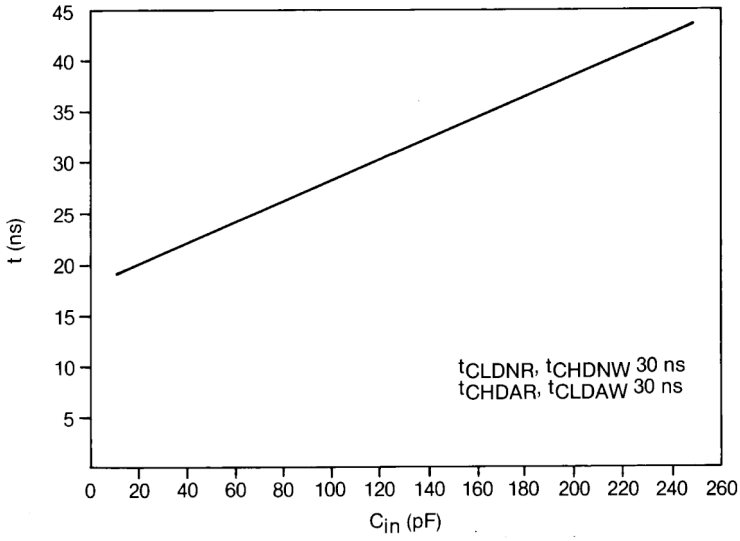
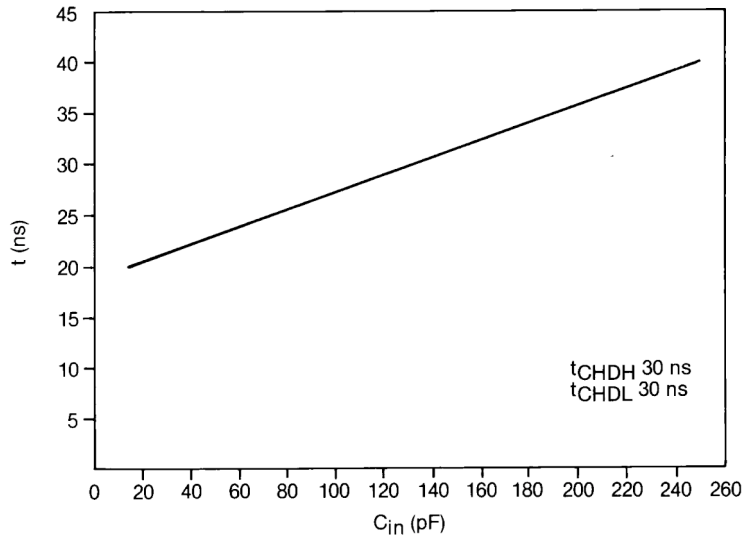


Figure 18. Data Capacitance Derating Curve



Functional Description

Description of Registers

As shown in the programming models (Figure 19 and Figure 20) the TS68020 has sixteen 32-bit general-purpose registers, a 32-bit program counter, two 32-bit supervisor stack pointers, a 16-bit status register, a 32-bit vector base register, two 3-bit alternate function code registers, and two 32-bit cache handling (address and control) registers. Registers D0-D7 are used as data registers for bit and bit field (1- to 32-bit), byte (8-bit), long word (32-bit), and quad word (64-bit) operations. Registers A0-A6 and the user, interrupt, and master stack pointers are address registers that may be used as software stack pointers or base address registers. In addition, the address registers may be used for word and long word operations. All of the 16 (D0-D7, A0-A7) registers may be used as index registers.

The status register (Figure 21) contains the interrupt priority mask (three bits) as well as the condition codes: extend (X), negated (N), zero (Z), overflow (V), and carry (C). Additional control bits indicate that the processor is in the trace mode (T1 or T0), supervisor/user state (S), and master/interrupt state (M).

All microprocessors of the TS68000 Family support instruction tracing (via the T0 status bit in the TS68020) where each instruction executed is followed by a trap to a user-defined trace routine. The TS68020 adds the capability to trace only the change of flow instructions (branch, jump, subroutine call and return, etc.) using the T1 status bit. These features are important for software program development and debug.

The vector base register is used to determine the runtime location of the exception vector table in memory, hence it supports multiple vector tables so each process or task can properly manage exceptions independent of each other.

The 18 addressing modes, shown in Table 8, include nine basic types:

- Register Direct
- Register Indirect
- Register Indirect with Index
- Memory Indirect
- Program Counter Indirect with Displacement
- Program Counter Indirect with Index
- Program Counter Memory Indirect
- Absolute
- Immediate

The register indirect addressing modes support postincrement, predecrement, offset, and indexing. Programmers find these capabilities particularly useful for handling advanced data structures common to sophisticated applications and high level languages. The program counter relative mode also has index and offset capabilities; programmers find that this addressing mode is required to support position-independent software. In addition to these addressing modes, the TS68020 provides data operand sizing and scaling; these features provide performance enhancements to the programmer.

Table 8. TS68020 Addressing Modes

Addressing Modes	Syntax
Register Direct	
Data Register Direct	Dn
Address Register Direct	An
Register Indirect	
Address Register Indirect	(An)
Address Register Indirect with Post Increment	(An) +
Address Register Indirect with Predecrement	– (An)
Address Register Indirect with Displacement	(d_{16}An)
Register Indirect with Index	
Address Register Indirect with Index (8-bit Displacement)	(d_8, An, Xn)
Address Register Indirect with Index (Base Displacement)	(bd, An, Xn)
Memory Indirect	
Memory Indirect Post-Indexed	([bd, An], Xn, od)
Memory Indirect Pre-Indexed	([bd, An, Xn], od)
Program Counter Indirect with Displacement	(d_{16}, PC)
Program Counter Indirect with Index	
PC Indirect with Index (8-bit Displacement)	(d_8, PC, Xn)
PC Indirect with Index (Base Displacement)	(bd, PC, Xn)
Program Counter Memory Indirect	
PC Memory Indirect Post-Indexed	([bd, PC], Xn, od)
PC Memory Indirect Pre-Indexed	([bd, PC, Xn]), od)

Table 9. Instruction Set (Continued)

Mnemonic	Description
CALLM	Call Module
CAS	Compare and Swap Operands
CAS2	Compare and Swap Dual Operands
CHK	Check Register Against Bound
CHK2	Check Register Against Upper and Lower Bounds
CLR	Clear
CMP	Compare
CMPA	Compare Address
CMPI	Compare Immediate
CMPM	Compare Memory to Memory
CMP2	Compare Register Against Upper and Lower Bounds
DBcc	Test Condition, Decrement and Branch
DIVS, DIVSL	Signed Divide
DIVU, DIVUL	Unsigned Divide
EOR	Logical Exclusive OR
EORI	Logical Exclusive OR Immediate
EXG	Exchange Registers
EXT, EXTB	Sign Extend
ILLEGAL	Take Illegal Instruction Tape
JMP	Jump
JSR	Jump to Subroutine
LEA	Load Effective Address
LINK	Link and Allocate
LSL, LSR	Logical Shift Left and Right
MOVE	Move
MOVEA	Move Address
MOVE CCR	Move Condition Code Register
MOVE SR	Move Status Register
MOVE USP	Move User Stack Pointer
MOVEC	Move Control Register
MOVEM	Move Multiple Registers
MOVEP	Move Peripheral
MOVEQ	Move Quick
MOVES	Move Alternate Address Space
MULS	Signed Multiply
MULU	Unsigned Multiply
NBCD	Negate Decimal with Extend
NEG	Negate
NEGX	Negate with Extend
NOP	No Operation
NOT	Logical Complement

Table 9. Instruction Set (Continued)

Mnemonic	Description
OR	Logical Inclusive OR
ORI	Logical Inclusive OR Immediate
PACK	Pack BCD
PEA	Push Effective Address
RESET	Reset External Devices
ROL, ROR	Rotate Left and Right
ROXL, ROXR	Rotate with Extend Left and Right
RTD	Return and Deallocate
RTE	Return and Exception
RTM	Return from Module
RTR	Return and Restore Codes
RTS	Return from Subroutine
SBCD	Subtract Decimal with Extend
Scc	Set Conditionally
STOP	Stop
SUB	Subtract
SUBA	Subtract Address
SUBI	Subtract Immediate
SUBQ	Subtract Quick
SUBX	Subtract with Extend
SWAP	Swap Register Words
TAS	Test Operand and Set
TRAP	Trap
TRAPcc	Trap Conditionally
TRAPV	Trap on Overflow
TST	Test Operand
UNLK	Unlink
UNPK	Unpack BCD
Co-processor Instructions	
cpBCC	Branch Conditionally
cpDBcc	Test Co-processor Condition, Decrement and Branch
cpGEN	Co-processor General Instruction
cpRESTORE	Restore Internal State of Co-processor
cpSAVE	Save Internal State of Co-processor
cpScc	Set Conditionally
cpTRAPcc	Trap Conditionally

Bit Field Operation

The TS68020 supports variable length bit field operations up to 32-bit. A bit field may start in any bit position and span any address boundary for the full length of the bit field, up to the 32-bit maximum. The bit field insert (BFINS) inserts a value into a field. Bit field extract unsigned (BFEXTU) and bit field extract signed (BFEXTS) extract an unsigned or signed value from the field. BFFFO finds the first bit in a bit field that is set. To complement the TS68000 bit manipulation instruction, there are bit field change, clear, set and test instructions (BFCHG, BFCLR, BFSET, BFTST). Using the on-chip barrel shifter, the bit and bit field instructions are very fast and particularly useful in applications using packed bits and bit fields, such as graphics and communications.

Binary Coded Decimal (BCD) Support

The TS68000 Family supports BCD operations including add, subtract, and negation. The TS68020 adds the PACK and UNPACK operations for BCD conversions to and from binary form as well as other conversions, e.g., ASCII and EBCDIC. The PACK instruction reduces two bytes of data into a single byte while UNPACK reverses the operation.

Bounds Checking

Previous 68000 Family members offer variable bounds checking only on the upper limit of the bound. The underlying assumption is that the lower bound is zero. This is expanded on the TS68020 by providing two new instructions, CHK2 and CMP2. These instructions allow checking and comparing of both the upper and lower bounds. These instructions may be either signed or unsigned. The CMP2 instructions sets the condition codes upon completion while the CHK2 instruction, in addition to setting the condition codes, will take a system trap if either boundary condition is exceeded.

System Traps

Three additions have been made to the system trap capabilities of the TS68020. The current TRAPV (trap on overflow) instruction has been expanded to a TRAPcc format where any condition code is allowed to be the trapping condition. And, the TRAPcc instruction is expanded to optionally provide one or two additional words following the trap instruction so user-specified information may be presented to the trap handler. These additional words can be used when needed to provide simple error codes or debug information for interactive runtime debugging or post-mortem program dumps. Compilers may provide direction to run-time execution routines towards handling of specific conditions.

The breakpoint instruction, BKPT, is used to support the program breakpoint function for debug monitors and real-time in-circuit or hardware emulators, and the operation will be dependent on the actual system implementation. Execution of this instruction causes the TS68020 to run a breakpoint acknowledge bus cycle, with a 3-bit breakpoint identifier placed on address lines A2, A3, and A4. This 3-bit identifier permits up to eight breakpoints to be easily differentiated. The normal response to the TS68020 is an operation word (typically an instruction, originally replaced by the debugger with the breakpoint instruction) placed on the data lines by external debugger hardware and the breakpoint acknowledge cycle properly terminated. The TS68020 then executes this operation word in place of the breakpoint instruction. The debugger hardware can count the number of executions of each breakpoint and halt execution after a pre-determined number of cycles.

The TS68020 uses instruction continuation to support virtual memory. In order for the TS68020 to use instruction continuation, it stores its internal state on the supervisor stack when a bus cycle is terminated with a bus error signal. It then loads the program counter with the address of the virtual memory bus error handler from the exception vector table (entry number two) and resumes program execution to that new address. When the bus error exception handler routine has completed execution, an RTE instruction is executed which reloads the TS68020 with the internal state stored on the stack, reruns the faulted bus cycle (when required), and continues the suspended instruction.

Instruction continuation is crucial to the support of virtual I/O devices in memory-mapped input/output systems. Since the registers of a virtual device may be simulated in the memory map, an access to such a register will cause a fault and the function of the register can be emulated by software.

Virtual Machine

A typical use for a virtual machine system is the development of software, such as an operating system, for a new machine also under development and not yet available for programming use. In such a system, a governing operating system emulates the hardware of the prototype system and allows the new operating system to be executed and debugged as though it were running on the new hardware. Since the new operating system is controlled by the governing operating system, it is executed at a lower privilege level than the governing operating system. Thus, any attempts by the new operating system to use virtual resources that are not physically present (and should be emulated) are trapped to the governing system and handled by its software. In the TS68020, a virtual machine is fully supported by running the new operating system in the user mode. The governing operating system executes in the supervisor mode and any attempt by the new operating system to access supervisor resources or execute privileged instructions will cause a trap to the governing operating system.

Operand Transfer Mechanism

Though the TS68020 has a full 32-bit data bus, it offers the ability to automatically and dynamically downsize its bus to 8- or 16-bit if peripheral devices are unable to accommodate the entire 32-bit. This feature allows the programmer the ability to write code that is not bus-width specific. For example, long word (32-bit) accesses to peripherals may be used in the code, yet the TS68020 will transfer only the amount of data that the peripheral can manage. This feature allows the peripheral to define its port size as 8-, 16-, or 32-bit wide and the TS68020 will dynamically size the data transfer accordingly, using multiple bus cycles when necessary. Hence, programmers are not required to program for each device port size or know the specific port size before coding; hardware designers have flexibility to choose implementations independent of software prejudices.

This is accomplished through the use of the $\overline{\text{DSACK}}$ pins and occurs on a cycle-by-cycle basis. For example, if the processor is executing an instruction that requires the reading of a long word operand, it will attempt to read 32-bit during the first bus cycle to a long word address boundary. If the port responds that it is 32-bit wide, the TS68020 latches all 32-bit of data and continues. If the port responds that it is 16-bit wide, the TS68020 latches 16 valid bits of data and runs another cycle to obtain the other 16-bit of data. An 8-bit port is handled similarly by with four bus read cycles. Each port is fixed in assignment to particular sections of the data bus.

Justification of data on the bus is handled automatically by dynamic bus sizing. When reading 16-bit data from a 32-bit port, the data may appear on the top or bottom half of the bus, depending on the address of the data. The TS68020 determines which portion of the bus is needed to support the transfer and dynamically adjusts to read or write the data on those data lines.

The TS68020 provides an extension to the exception stacking process. If the M bit in the status register is set, the master stack pointer (MSP) is used for all task related exceptions. When a non-task exception occurs (i.e., an interrupt), the M bit is cleared and the interrupt stack pointer (ISP) is used. This feature allows all the task's stack area to be carried within a single processor control block and new tasks may be initiated by simply reloading the master stack pointer and setting the M bit.

The fourth and last step of the exception processing is the same for all exceptions. The exception vector offset is determined by multiplying the vector number by four. This offset is then added to the contents of the vector base register (VBR) to determine the memory address of the exception vector. The new program counter value is fetched from the exception vector. The instruction at the address given in the exception vector is fetched, and the normal instruction decoding and execution is started.

On-chip Instruction Cache

Studies have shown that typical programs spend most of their execution time in a few main routines or tight loops. This phenomenon is known as locality of reference, and has an impact on performance of the program. The TS68020 takes limited advantage of this phenomenon in the form of its loop mode operation which allows certain instructions, when coupled with the DBcc instruction, to execute without the overhead of instruction fetches. In effect, this is a three word cache. Although the cache hardware has been supplied in a full range of computer systems for many years, technology now allows this feature to be integrated into the microprocessor.

TS68020 Cache Goals

There were two primary goals for the TS68020 microprocessor cache. The first design goal was to reduce the processor external bus activity. In a given TS68000 system, the TS68000 processor will use approximately 80 to 90 percent (for greater) of the available bus bandwidth. This is due to its extremely efficient perfecting algorithm and the overall speed of its internal architecture design. Thus, in an TS68000 system with more than one bus master (such as a processor and DMA device) or in a multiprocessor system, performance degradation can occur due to lack of available bus bandwidth. Therefore, an important goal for an TS68020 on-chip cache was to provide a substantial increase in the total available bus bandwidth.

The second primary design goal was to increase effective CPU throughput as larger memory sizes or slower memories increased average access time. By placing a high speed cache between the processor and the rest of the memory system, the effective access time now becomes:

$$t_{ACC} = h^{**}t_{CACHE} = (1 - h)^{*}t_{ext}$$

where t_{ACC} is the effective system access time, t_{CACHE} is the cache access time, t_{ext} is the access time of the rest of the system, and h is the hit ratio or the percentage of time that the data is found in the cache. Thus, for a given system design, an TS68020 on-chip cache provides a substantial CPU performance increase, or allows much slower and less expensive memories to be used for the same processor performance.

The throughput increase in the TS68020 is gained in two ways. First, the TS68020 cache is accessed in two clock cycles versus the three cycles (minimum) required for an external access. Any instruction fetch that is currently resident in the cache will provide a 33% improvement over the corresponding external access.

Preparation for Delivery

Certificate of Compliance

Atmel offers a certificate of compliance with each shipment of parts, affirming the products are in compliance with MIL-STD-883 and guaranteeing the parameters are tested at extreme temperatures for the entire temperature range.

Handling

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

a) Device should be handled on benches with conductive and grounded surface.

b) Ground test equipment, tools and operator

c) Do not handle devices by the leads.

d) Store devices in conductive foam or carriers.

e) Avoid use of plastic, rubber, or silk in MOS areas.

f) Maintain relative humidity above 50%, if practical.

Ordering Information

Hi-REL Product

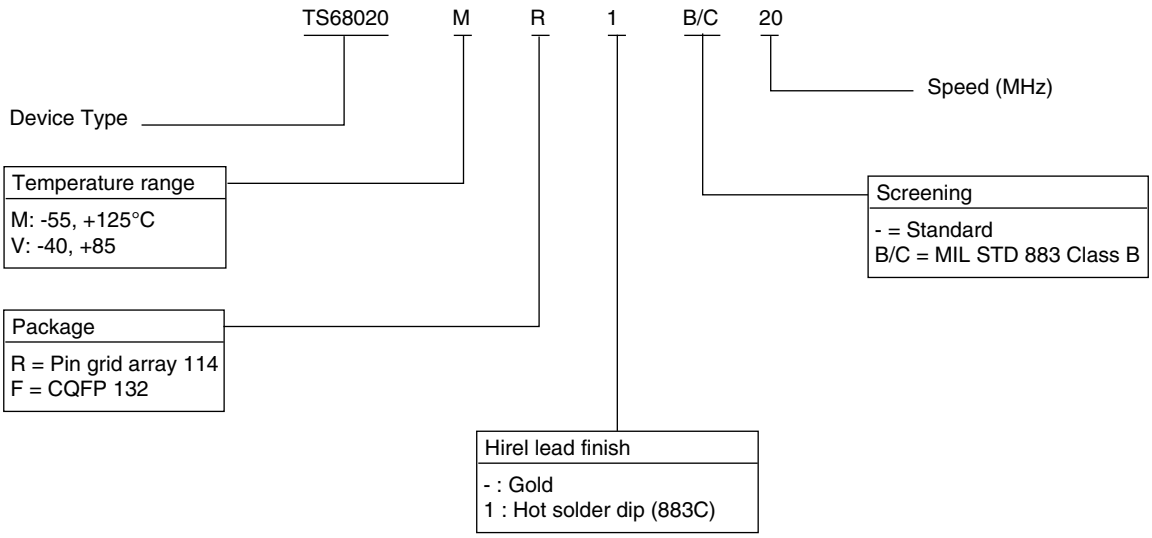
Commercial Atmel Part-Number	Norms	Package	Temperature Range T_c (°C)	Frequency (MHz)	Drawing Number
TS68020MRB/C16	MIL-STD-883	PGA 114	-55/+125	16.67	-
TS68020MR1B/C16	MIL-STD-883	PGA 114/tin	-55/+125	16.67	-
TS68020MRB/C20	MIL-STD-883	PGA 114	-55/+125	20	-
TS68020MR1B/C20	MIL-STD-883	PGA 114/tin	-55/+125	20	-
TS68020MRB/C25	MIL-STD-883	PGA 114	-55/+125	25	-
TS68020MR1B/C25	MIL-STD-883	PGA 114/tin	-55/+125	25	-
TS68020MFB/C16	MIL-STD-883	CQFP 132	-55/+125	16.67	-
TS68020MF1B/C16	MIL-STD-883	CQFP 132/tin	-55/+125	16.67	-
TS68020MFB/C20	MIL-STD-883	CQFP 132	-55/+125	20	-
TS68020MF1B/C20	MIL-STD-883	CQFP 132/tin	-55/+125	20	-
TS68020MFB/C25	MIL-STD-883	CQFP 132	-55/+125	25	-
TS68020MF1B/C25	MIL-STD-883	CQFP 132/tin	-55/+125	25	-
TS68020DESC02XA	DESC	PGA 114/tin	-55/+125	16.67	5962-8603202XA
TS68020DESC03XA	DESC	PGA 114/tin	-55/+125	20	5962-8603203XA
TS68020DESC04XA	DESC	PGA 114/tin	-55/+125	25	5962-8603204XA
TS68020DESC02XC	DESC	PGA 114	-55/+125	16.67	5962-8603202XC
TS68020DESC03XC	DESC	PGA 114	-55/+125	20	5962-8603203XC
TS68020DESC04XC	DESC	PGA 114	-55/+125	25	5962-8603204XC
TS68020DESC02YA	DESC	CQFP 132/tin	-55/+125	16.67	5962-8603202YA
TS68020DESC03YA	DESC	CQFP 132/tin	-55/+125	20	5962-8603203YA
TS68020DESC04YA	DESC	CQFP 132/tin	-55/+125	25	5962-8603204YA
TS68020DESC02YC	DESC	CQFP 132	-55/+125	16.67	5962-8603202YC
TS68020DESC03YC	DESC	CQFP 132	-55/+125	20	5962-8603203YC
TS68020DESC04YC	DESC	CQFP 132	-55/+125	25	5962-8603204YC

Standard Product

Commercial Atmel Part-Number	Norms	Package	Temperature Range T_c (°C)	Frequency (MHz)	Drawing Number
TS68020VR16	Internal Standard	PGA 114	-40/+85	16.67	Internal
TS68020VR20	Internal Standard	PGA 114	-40/+85	20	Internal
TS68020VR25	Internal Standard	PGA 114	-40/+85	25	Internal
TS68020MR16	Internal Standard	PGA 114	-55/+125	16.67	Internal
TS68020MR20	Internal Standard	PGA 114	-55/+125	20	Internal
TS68020MR25	Internal Standard	PGA 114	-55/+125	25	Internal

Standard Product

Commercial Atmel Part-Number	Norms	Package	Temperature Range T_c (°C)	Frequency (MHz)	Drawing Number
TS68020VF16	Internal Standard	CQFP 132	-40/+85	16.67	Internal
TS68020VF120	Internal Standard	CQFP 132	-40/+85	20	Internal
TS68020VF25	Internal Standard	CQFP 132	-40/+85	25	Internal
TS68020MF16	Internal Standard	CQFP 132	-55/+125	16.67	Internal
TS68020MF20	Internal Standard	CQFP 132	-55/+125	20	Internal
TS68020MF25	Internal Standard	CQFP 132	-55/+125	25	Internal



Note: For availability of the different versions, contact your Atmel sales office.