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Understanding Embedded - Microprocessors

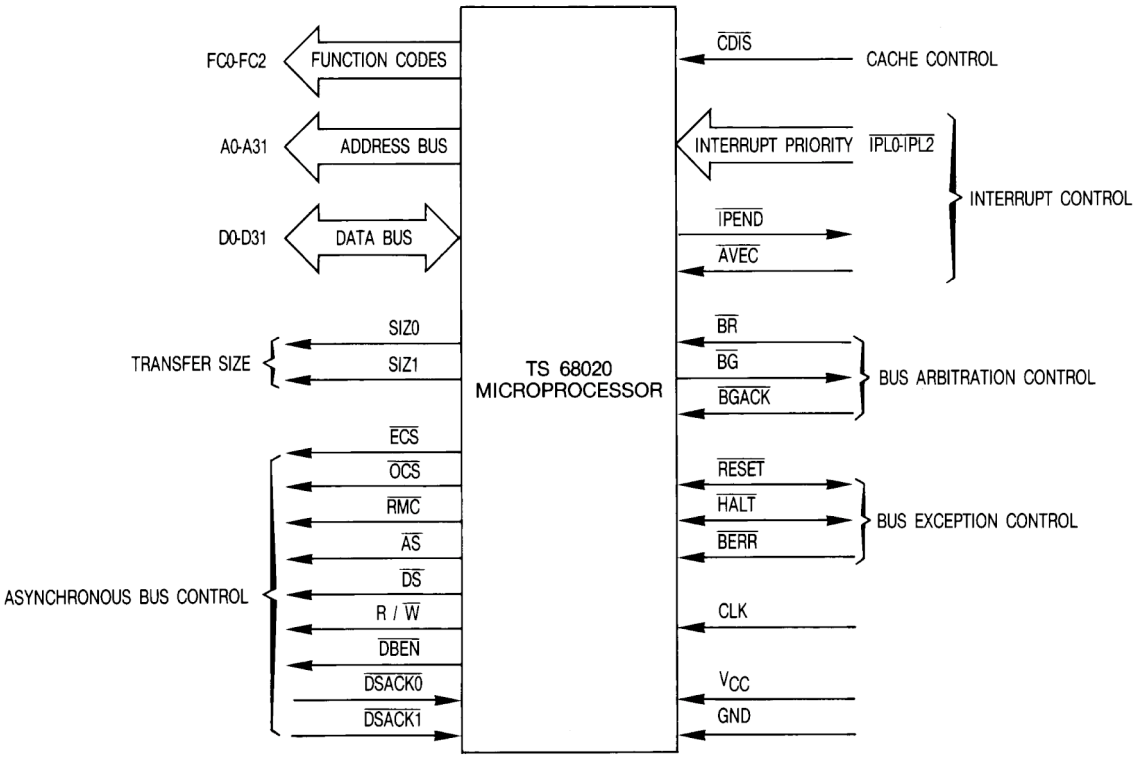
Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	68000
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	16.67MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-55°C ~ 125°C (TC)
Security Features	-
Package / Case	132-BCQFP
Supplier Device Package	132-CQFP (24.13x24.13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts68020mf16

Figure 4. Functional Signal Groups



Signal Description

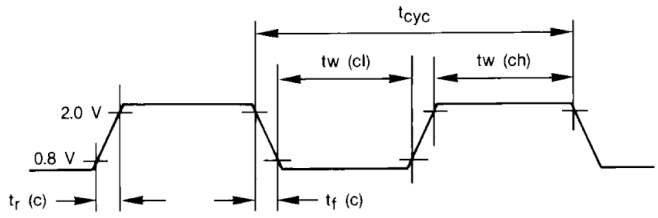
Figure 4 illustrates the functional signal groups and Table 1 lists the signals and their function.

The V_{CC} and GND pins are separated into four groups to provide individual power supply connections for the address bus buffers, data bus buffers, and all other output buffers and internal logic.

Group	V_{CC}	GND
Address Bus	A9, D3	A10, B9,C3, F12
Data Bus	M8, N8, N13	L7, L11, N7, K3
Logic	D1, D2, E3, G11, G13	G12, H13, J3, K1
Clock	—	B1

This device contains protective circuitry against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

Figure 5. Clock Input Timing Diagram



Note: Timing measurements are referenced to and from a low voltage of 0.8V and a high voltage of 2.0V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8V and 2.0V.

Table 4. Thermal Characteristics at 25°C

Package	Symbol	Parameter	Value	Unit
PGA 114	θ_{JA}	Thermal Resistance - Ceramic Junction to Ambient	26	°C/W
	θ_{JC}	Thermal Resistance - Ceramic Junction to Case	5	°C/W
CQFP 132	θ_{JA}	Thermal Resistance - Ceramic Junction to Ambient	34	°C/W
	θ_{JC}	Thermal Resistance - Ceramic Junction to Case	2	°C/W

Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \cdot V_{CC}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K + (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273) + \theta_{JA} \cdot P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part K can be determined from equation **(3)** by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations **(1)** and **(2)** iterativley for any value of T_A.

For dynamic characteristics (Table 6), test methods refer to IEC 748-2 method, where existing.

Indication of “min.” or “max.” in the column “test temperature” means minimum or maximum operating temperature.

Table 5. Static Characteristics. V_{CC} = 5.0V_{DC} ± 10%; GND = 0V_{DC}; T_c = -55/+125°C or -40/+85°C (Figure 4 to Figure 8)

Symbol	Parameter	Condition	Min	Max	Units
I_{CC}	Maximum Supply Current	V_{CC} = 5.5V T_{case} -55°C to +25°C		333	mA
I_{CC}	Maximum Supply Current	V_{CC} = 5.5V T_{case} = 125°C		207	mA
V_{IH}	High Level Input Voltage	V_O = 0.5V or 2.5 V_{CC} = 4.5V to 5.5V	2.0	V_{CC}	V
V_{IL}	Low Level Input Voltage	V_O = 0.5V or 2.4V V_{CC} = 4.5V to 5.5V	-0.5	0.8	V
V_{OH}	High Level Output Voltage All Outputs	I_{OH} = 400 µA	2.4		V
V_{OL}	Low Level Output Voltage Outputs A0-A31, FC0-FC2, D0-D31, SIZ0-SIZ1, $\overline{BG}$	I_{OL} = 3.2 mA Load Circuit as Figure 8 R = 1.22 kΩ		0.5	V
V_{OL}	Low Level Output Voltage Outputs $\overline{AS}$, $\overline{DS}$, $\overline{RMC}$, R/$\overline{W}$, $\overline{DBEN}$, $\overline{IPEND}$	I_{OL} = 5.3 mA Load Circuit as Figure 8 R = 740Ω		0.5	V
V_{OL}	Low Level Output Voltage Outputs $\overline{ECS}$, $\overline{OCS}$	I_{OL} = 2.0 mA Load Circuit as Figure 8 R = 2 kΩ		0.5	V
V_{OL}	Low Level Output Voltage Outputs $\overline{HALT}$, $\overline{RESET}$	I_{OL} = 10.7 mA Load Circuit as Figure 6 and Figure 7		0.5	V
$\lvert I_{IN} \rvert$	Input Leakage Current (High and Low State)	-0.5V ≤ V_{IN} ≤ V_{CC} (Max)		2.5	µA
$\lvert I_{OHZ} \rvert$	High level leakage current at three-state outputs Outputs A0-A31, $\overline{AS}$, $\overline{DBEN}$, $\overline{DS}$, D0-D31, R/$\overline{W}$, FC0-FC2, $\overline{RMC}$, SIZ0-SIZ1	V_{OH} = 2.4V		2.5	µA
$\lvert I_{OLZ} \rvert$	Low Level Leakage Current at Three-state Outputs Outputs A0-A31, $\overline{AS}$, $\overline{DBEN}$, $\overline{DS}$, D0-D31 R/$\overline{W}$, FC0-FC2, $\overline{RMC}$, SIZ0-SIZ1	V_{OL} = 0.5V		2.5	µA
I_{OS}	Output Short-circuit Current (Any Output)	V_{CC} = 5.5V V_O = 0V (Pulsed. Duration 1 ms Duty Cycle 10:1)		200	mA

Dynamic (Switching) Characteristics

The limits and values given in this section apply over the full case temperature range -55°C to +125°C and V_{CC} in the range 4.5V to 5.5V V_{IL} = 0.5V and V_{IH} = 2.4V (See also note 12 and 13). The INTERVAL numbers refer to the timing diagrams. See Figure 5, Figure 9 and Figure 12.

Table 6. Dynamic Electrical Characteristics

Symbol	Parameter	Interval Number	68020-16		68020-20		68020-25		Unit	Notes
			Min	Max	Min	Max	Min	Max		
t_{CPW}	Clock Pulse Width	2 , 3	24	95	20	54	19	61	ns	
t_{CHAV}	Clock High to Address/FC/Size/$\overline{RMC}$ Valid	6	0	30	0	25	0	25	ns	
t_{CHEV}	Clock High to $\overline{ECS}$, $\overline{OCS}$ Asserted	6A	0	20	0	15	0	12	ns	
t_{CHAZX}	Clock High to Address/Data/FC/$\overline{RMC}$/ Size High Impedance	7	0	60	0	50	0	40	ns	(11)
t_{CHAZn}	Clock High to Address/FC/Size/$\overline{RMC}$ Invalid	8	0		0		0		ns	
t_{CLSA}	Clock Low to $\overline{AS}$, $\overline{DS}$ Asserted	9	3	30	3	25	3	18	ns	
t_{STSA}	$\overline{AS}$ to $\overline{DS}$ Assertion (Read)(Skew)	9A	-15	15	-10	10	-10	10	ns	(1)
t_{ECSA}	$\overline{ECS}$ Width Asserted	10	20		15		15		ns	
t_{OCSA}	$\overline{OCS}$ Width Asserted	10A	20		15		15		ns	
t_{EOCSN}	$\overline{ECS}$, $\overline{OCS}$ Width Negated	10B	15		10		5		ns	(11)
t_{AVSA}	Address/FC/Size/$\overline{RMC}$ Valid to $\overline{AS}$ Asserted (and $\overline{DS}$ Asserted, Read)	11	15		10		6		ns	(6)
t_{CLSN}	Clock Low to $\overline{AS}$, $\overline{DS}$ Negated	12	0	30	0	25	0	15	ns	
t_{CLEN}	Clock Low to $\overline{ECS}$/$\overline{OCS}$ Negated	12A	0	30	0	25	0	15	ns	
t_{SNAI}	$\overline{AS}$, $\overline{DS}$ Negated to Address/FC/ Size/$\overline{RMC}$ Invalid	13	15		10		10		ns	
t_{SWA}	$\overline{AS}$ (and $\overline{DS}$, Read) Width Asserted	14	100		85		70		ns	
t_{SWAW}	$\overline{DS}$ Width Asserted, Write	14A	40		38		30		ns	
t_{SN}	$\overline{AS}$, $\overline{DS}$ Width Negated	15	40		38		30		ns	(11)
t_{SNSA}	$\overline{DS}$ Negated to $\overline{AS}$ Asserted	15A	35		30		25		ns	(8)
t_{CSZ}	Clock High to $\overline{AS}$/$\overline{DS}$/R/$\overline{W}$/$\overline{DBEN}$ High Impedance	16		60		50		40	ns	(11)
t_{SNRN}	$\overline{AS}$, $\overline{DS}$ Negated to R/$\overline{W}$ High	17	15		10		10		ns	(6)
t_{CHRH}	Clock High to R/$\overline{W}$ High	18	0	30	0	25	0	20	ns	
t_{CHRL}	Clock High to R/$\overline{W}$ Low	20	0	30	0	25	0	20	ns	
t_{RAAA}	R/$\overline{W}$ High to $\overline{AS}$ Asserted	21	15		10		5		ns	(6)
t_{RASA}	R/$\overline{W}$ Low to $\overline{DS}$ Asserted (Write)	22	75		60		50		ns	(6)
t_{CHDO}	Clock High to Data Out Valid	23		30		25		25	ns	
t_{SNDI}	AS, DS Negated to Data Out Valid	25	15		10		5		ns	(6)
t_{DNDBN}	$\overline{DS}$ Negated to $\overline{DBEN}$ Negated (Write)	25A	15		10		5		ns	(9)

Table 6. Dynamic Electrical Characteristics (Continued)

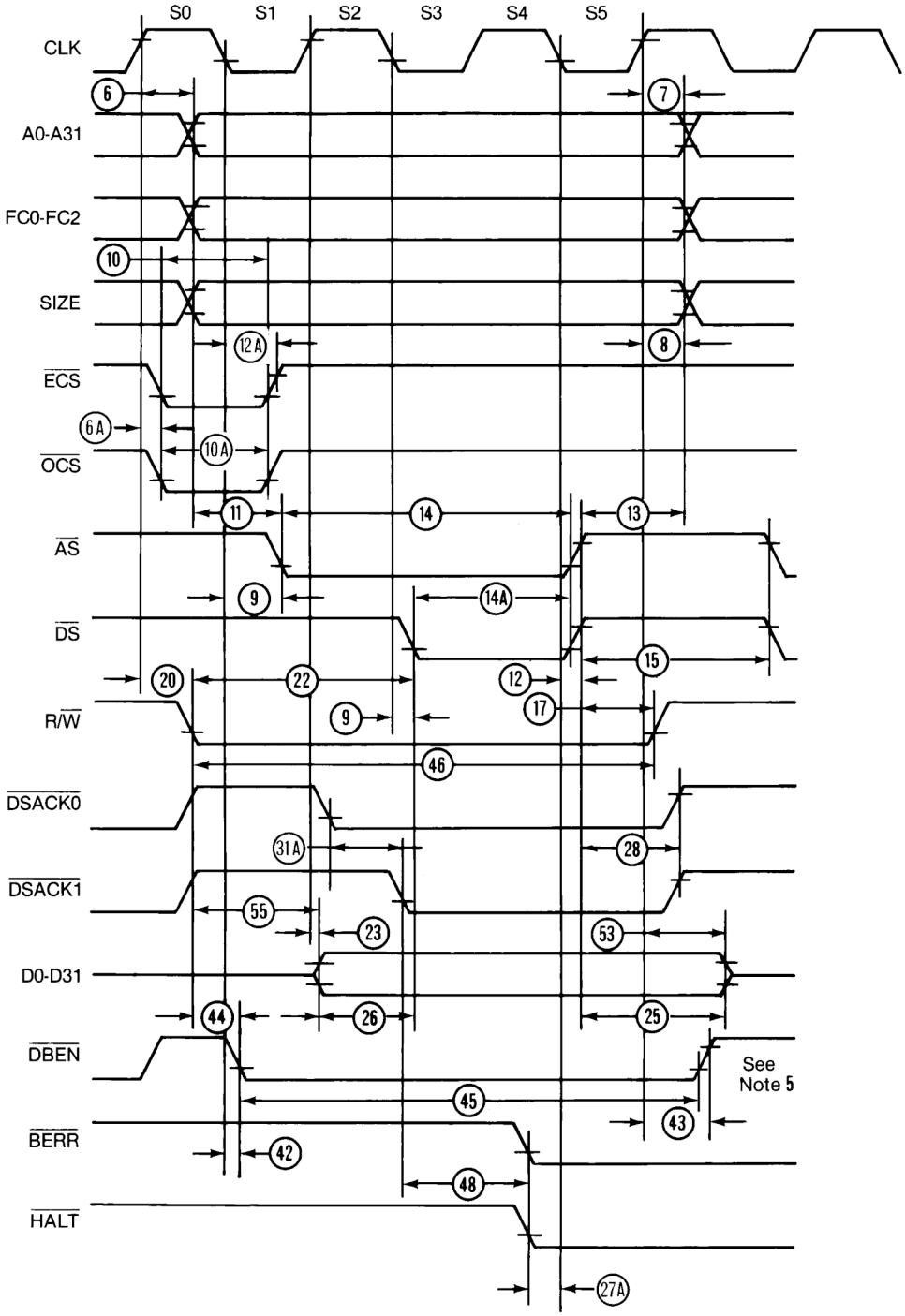
Symbol	Parameter	Interval Number	68020-16		68020-20		68020-25		Unit	Notes
			Min	Max	Min	Max	Min	Max		
t_{DVSA}	Data Out Valid to $\overline{DS}$ Asserted (Write) 26	26	15		10		5		ns	(6)
t_{DICL}	Data in Valid to Clock Low (Data Setup)	27	5		5		5		ns	
t_{BELCL}	Late $\overline{BERR}/\overline{HALT}$ Asserted to Clock Low Setup Time	27A	20		15		10		ns	
t_{SNDN}	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{DSACKx}/\overline{BERR}/\overline{HALT}/\overline{AVEC}$ Negated	28	0	80	0	65	0	50	ns	
t_{SNDI}	$\overline{DS}$ Negated to Data On Invalid (Data in Hold Time)	29	0		0		0		ns	(6)
t_{SNDIZ}	$\overline{DS}$ Negated to Data in High Impedance	29A		60		50		40	ns	
t_{DADI}	$\overline{DSACKx}$ Asserted to Data In Valid	31		50		43		32		(2)(11)
t_{DADV}	$\overline{DSACK}$ Asserted to $\overline{DSACKx}$ Valid ($\overline{DSACK}$ Asserted Skew)	31A		15		10		10	ns	(3)(11)
t_{HRrf}	$\overline{RESET}$ Input Transition Time	32		1.5		1.5		1.5	Clks	
t_{CLBA}	Clock Low to $\overline{BG}$ Asserted	33	0	30	0	25	0	20	ns	
t_{CLBN}	Clock Low to $\overline{BG}$ Negated	34	0	30	0	25	0	20	ns	
t_{BRAGA}	$\overline{BR}$ Asserted to $\overline{BG}$ Asserted (RMC Not Asserted)	35	1.5	3.5	1.5	3.5	1.5	3.5	Clks	(11)
t_{GAGN}	$\overline{BGACK}$ Asserted to $\overline{BG}$ Negated	37	1.5	3.5	1.5	3.5	1.5	3.5	Clks	(11)
t_{GABRN}	$\overline{BGACK}$ Asserted to $\overline{BR}$ Negated	37A	0	1.5	0	1.5	0	1.5	Clks	(11)
t_{GN}	$\overline{BG}$ Width Negated	39	90		75		60		ns	(11)
t_{GA}	$\overline{BG}$ Width Asserted	39A	90		75		60		ns	
t_{CHDAR}	Clock High to $\overline{DBEN}$ Asserted (Read)	40	0	30	0	25	0	20	ns	
t_{CLDNR}	Clock Low to $\overline{DBEN}$ Negated (Read)	41	0	30	0	25	0	20	ns	
t_{CLDAW}	Clock Low to $\overline{DBEN}$ Negated (Read)	42	0	30	0	25	0	20	ns	
t_{CHDNW}	Clock High to $\overline{DBEN}$ Asserted (Read)	43	0	30	0	25	0	20	ns	
t_{RADA}	R/W Low to $\overline{DBEN}$ Asserted (Write)	44	15		10		10		ns	(6)
t_{DA}	$\overline{DBEN}$ Width Asserted	45								
	READ		60		50		40		ns	(5)
	WRITE		120		100		80		ns	(5)
t_{RWA}	R/$\overline{W}$ Width Asserted (Write or Read)	46	150		125		100		ns	
t_{AIST}	Asynchronous Input Setup Time	47A	5		5		5		ns	(11)
t_{AIHT}	Asynchronous Input Hold Time	47B	15		15		10		ns	(11)
t_{DABA}	$\overline{DSACKx}$ Asserted to $\overline{BERR}/\overline{HALT}$ Asserted	48		30		20		18	ns	(4)(11)
t_{DOCH}	Data Out Hold from Clock High	53	0		0		0		ns	
t_{BNHN}	$\overline{BERR}$ Negated to $\overline{HALT}$ Negated (Rerun)		0		0		0		ns	

Table 6. Dynamic Electrical Characteristics (Continued)

Symbol	Parameter	Interval Number	68020-16		68020-20		68020-25		Unit	Notes
			Min	Max	Min	Max	Min	Max		
f	Frequency of Operation		8.0	16.67	12.5	20.0	12.5	25	MHz	
t_{RADC}	R/W Asserted to Data Bus Impedance Change	55	30		25		20			(11)
t_{HRPW}	$\overline{RESET}$ Pulse Width (Reset Instruction)	56	512		512		512		Clks	(11)
t_{BNHN}	$\overline{BERR}$ Negated to $\overline{HALT}$ Negated (Rerun)	57	0		0		0		ns	(11)
t_{GANBD}	$\overline{BGACK}$ Negated to Bus Driven	58	1		1		1		Clks	(10)(11)
t_{GNBD}	$\overline{BG}$ Negated to Bus Driven	59	1		1		1		Clks	(10)(11)

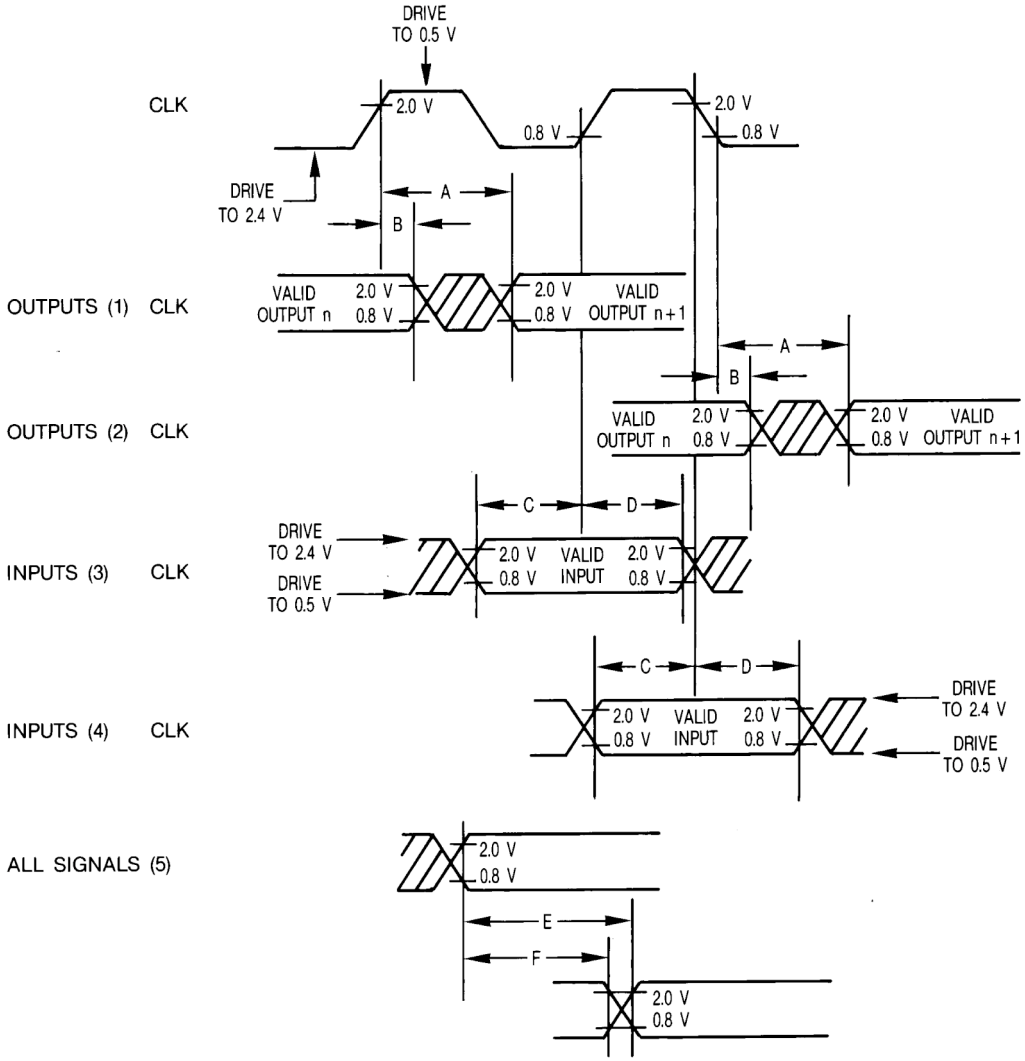
Notes:
1. This number can be reduced to 5 nanoseconds if the strobes have equal loads.
2. If the asynchronous setup time (= 47) requirements are satisfied, the DSACKx low to data setup time (= 31) and $\overline{DSACKx}$ low to $\overline{BERR}$ low setup time (= 48) can be ignored. The data must only satisfy the data in to clock low setup time (= 27) for the following clock cycle, $\overline{BERR}$ must only satisfy the late $\overline{BERR}$ low to clock setup time (= 27) for the following clock cycle.
3. This parameter specifies the maximum allowable skew between $\overline{DSACK0}$ to $\overline{DSACK1}$ asserted or $\overline{DSACK1}$ to $\overline{DSACK0}$ asserted pattern = 47 must be met by $\overline{DSACK0}$ and $\overline{DSACK1}$.
4. In the absence of $\overline{DSACKx}$, $\overline{BERR}$ is an asynchronous input using the asynchronous input setup time (= 47).
5. $\overline{DBEN}$ may stay asserted on consecutive write cycles.
6. Actual value depends on the clock input waveform.
7. This pattern indicates the minimum high time for $\overline{ECS}$ and $\overline{OCS}$ in the event of an internal cache hit followed immediately by a cache miss or operand cycle.
8. This specification guarantees operations with the 68881 co-processor, and defines a minimum time for DS negated to AS asserted (= 13A). Without this parameter, incorrect interpretation of = 9A and = 15 would indicate that the 68020 does not meet 68881 requirements.
9. This pattern allows the systems designer to guarantee data hold times on the output side of data buffers that have output enable signals generated with $\overline{DBEN}$.
10. Guarantees that an alternate bus master has stopped driving the bus when the 68020 regains control of the bus after an arbitration sequence.
11. Cannot be tested. Provided for system design purposes only.
12. T_{case} = -55°C and +130°C in a Power off condition under Thermal soak for 4 minutes or until thermal equilibrium. Electrical parameters are tested “instant on” 100 m sec. after power is applied.
13. All outputs unload except for load capacitance. Clock = fmax,
    LOW: $\overline{HALT}$, $\overline{RESET}$
    HIGH: $\overline{DSACK0}$, $\overline{DSACK1}$, $\overline{CDIS}$, $\overline{IPL0}$-$\overline{IPL2}$, $\overline{DBEN}$, $\overline{AVEC}$, $\overline{BERR}$.

Figure 10. Write Cycle Timing Diagram (Continued)



Note: Timing measurements are referenced to and from a low voltage of 0.8V and a high voltage of 2.0V, unless otherwise noted. The voltage swing thorough this range should start outside and pass through the range such that the rise or fall will be linear between 0.8V and 2.0V.

Figure 12. Drive Levels and Test Points for AC Specification



Legend:

A) Maximum Output Delay Specification

B) Minimum Output Hold Time

C) Minimum Input Setup Time Specification

D) Minimum Input Hold Time Specification

E) Signal Valid to Signal Valid Specification (Maximum or Minimum)

F) Signal Valid to Signal Invalid Specification (Maximum or Minimum)

Notes:
1. This output timing is applicable to all parameters specified relative to the rising edge of the clock.
2. This out put timing is applicable to all parameters specified relative to the falling edge of the clock.
3. This input timing is applicable to all parameters specified relative to the falling edge of the clock.
4. This input timing is applicable to all parameters specified relative to the falling edge of the clock.
5. This timing is applicable to all parameters specified relative to the assertion/negation of another signal.

Figure 14. ECS and OCS Capacitance Derating Curve

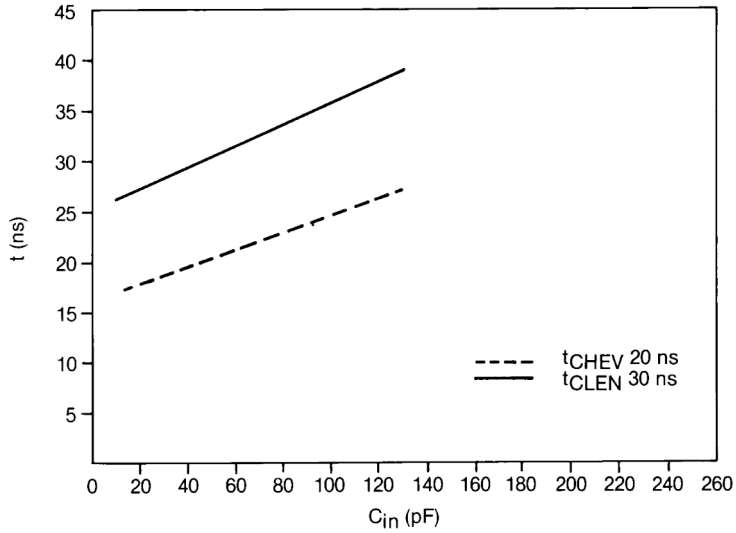


Figure 15. R/W, FC, SIZ0-SIZ1, and RMC Capacitance Derating Curve

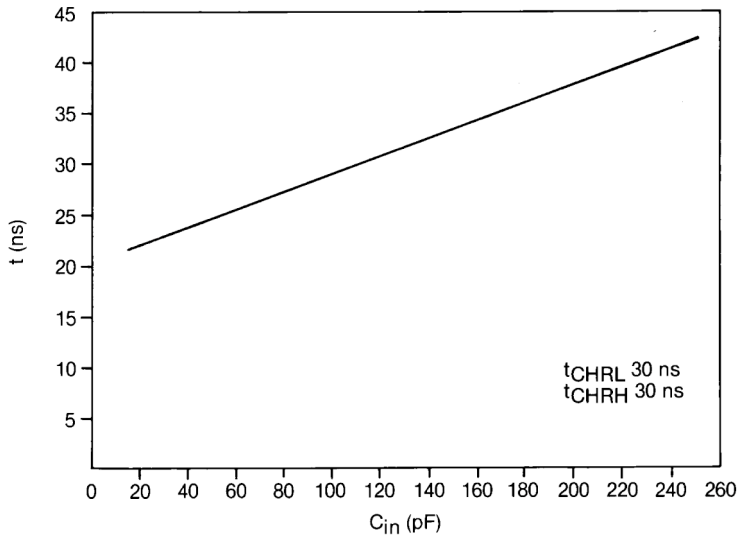


Figure 20. Supervisor Programming Model Supplement

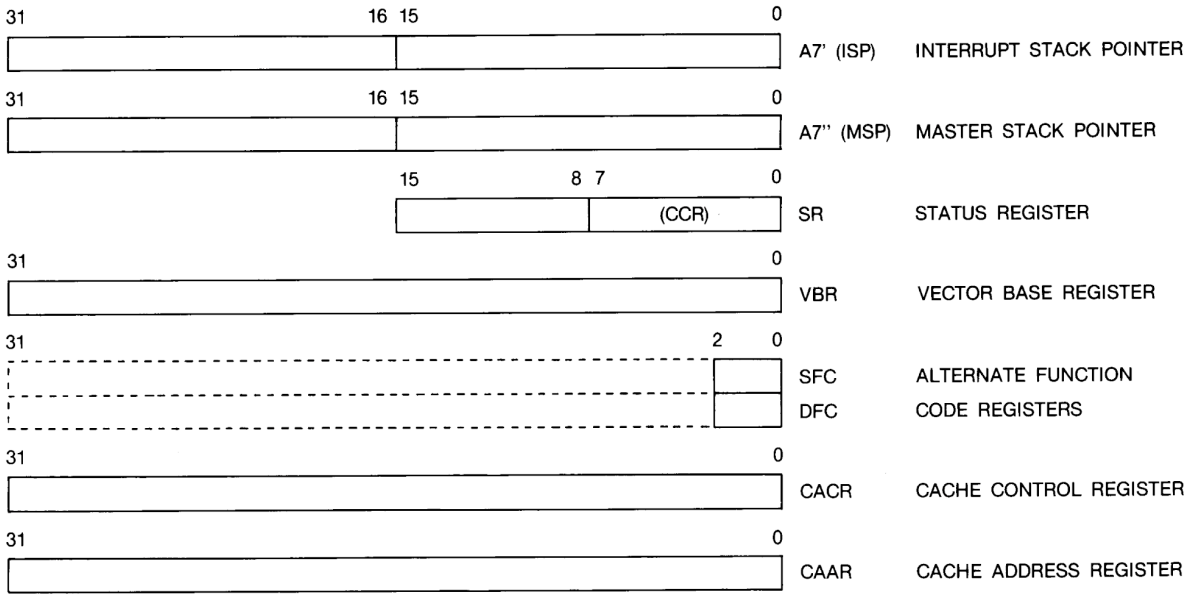
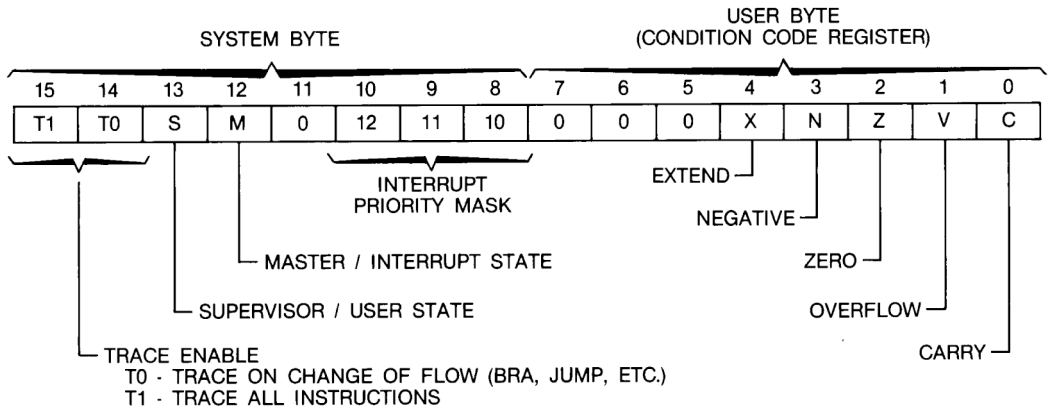


Figure 21. Status Register



Data Types and Addressing Modes

Seven basic types are supported. These data types are:

- Bits
- Bits Flieds (String of consecutive bits, 1-32 bits long)
- BCD Digits (Packed: 2 digits/byte, Unpacked: 1 digit/byte)
- Byte Integers (8-bit)
- Word Integers (16-bit)
- Long Word Integers (32-bit)
- Quad Word Integers (64-bit)

In addition, operations on other data types, such as memory addresses, status word data, etc...., are provided in the instruction set. The co-processor mechanism allows direct support of floating-point data type with the TS68881 and TS68882 floating-point co-processors, as well as specialized user-defined data types and functions.

Instruction Set Overview

The TS68020 instruction set is shown in Table 9. Special emphasis has been given to the instruction set's support of structured high-level languages and sophisticated operating systems. Each instruction, with few exceptions, operates on bytes, words, and long words and most instructions can use any of the 18 addressing modes. Many instruction extensions have been made on the TS68020 to take advantage of the full 32-bit operation where, on the earlier 68000 Family members, only 8 and 16 bits values were used. The TS68020 is upward source- and object-level code compatible with the family because it supports all of the instructions that previous family members offer. Additional instructions are now provided by the TS68020 in support of its advanced features.

Table 9. Instruction Set

Mnemonic	Description
ABCD	Add Decimal with Extend
ADD	Add
ADDA	Add Address
ADDI	Add Immediate
ADDQ	Add Quick
ADDX	Add with Extend
AND	Logical AND
ANDI	Logical AND Immediate
ASL, ASR	Arithmetic Shift Left and Right
Bcc	Branch Conditionally
BCHG	Test Bit and Change
BCLR	Test Bit and Clear
BFCHG	Test Bit Field and Change
BFCLR	Test Bit Field and Clear
BFEXTS	Signed Bit Field Extract
BFEXTU	Unsigned Bit Field Extract
BFFFO	Bit Field Find First One
BFINS	Bit Field Insert
BFSET	Test Bit Field and Set
BFTST	Test Bit Field
BKPT	Breakpoint
BRA	Branch
BSET	Test Bit and Set
BSR	Branch to Subroutine
BTST	Test Bit

Bit Field Operation

The TS68020 supports variable length bit field operations up to 32-bit. A bit field may start in any bit position and span any address boundary for the full length of the bit field, up to the 32-bit maximum. The bit field insert (BFINS) inserts a value into a field. Bit field extract unsigned (BFEXTU) and bit field extract signed (BFEXTS) extract an unsigned or signed value from the field. BFFFO finds the first bit in a bit field that is set. To complement the TS68000 bit manipulation instruction, there are bit field change, clear, set and test instructions (BFCHG, BFCLR, BFSET, BFTST). Using the on-chip barrel shifter, the bit and bit field instructions are very fast and particularly useful in applications using packed bits and bit fields, such as graphics and communications.

Binary Coded Decimal (BCD) Support

The TS68000 Family supports BCD operations including add, subtract, and negation. The TS68020 adds the PACK and UNPACK operations for BCD conversions to and from binary form as well as other conversions, e.g., ASCII and EBCDIC. The PACK instruction reduces two bytes of data into a single byte while UNPACK reverses the operation.

Bounds Checking

Previous 68000 Family members offer variable bounds checking only on the upper limit of the bound. The underlying assumption is that the lower bound is zero. This is expanded on the TS68020 by providing two new instructions, CHK2 and CMP2. These instructions allow checking and comparing of both the upper and lower bounds. These instructions may be either signed or unsigned. The CMP2 instructions sets the condition codes upon completion while the CHK2 instruction, in addition to setting the condition codes, will take a system trap if either boundary condition is exceeded.

System Traps

Three additions have been made to the system trap capabilities of the TS68020. The current TRAPV (trap on overflow) instruction has been expanded to a TRAPcc format where any condition code is allowed to be the trapping condition. And, the TRAPcc instruction is expanded to optionally provide one or two additional words following the trap instruction so user-specified information may be presented to the trap handler. These additional words can be used when needed to provide simple error codes or debug information for interactive runtime debugging or post-mortem program dumps. Compilers may provide direction to run-time execution routines towards handling of specific conditions.

The breakpoint instruction, BKPT, is used to support the program breakpoint function for debug monitors and real-time in-circuit or hardware emulators, and the operation will be dependent on the actual system implementation. Execution of this instruction causes the TS68020 to run a breakpoint acknowledge bus cycle, with a 3-bit breakpoint identifier placed on address lines A2, A3, and A4. This 3-bit identifier permits up to eight breakpoints to be easily differentiated. The normal response to the TS68020 is an operation word (typically an instruction, originally replaced by the debugger with the breakpoint instruction) placed on the data lines by external debugger hardware and the breakpoint acknowledge cycle properly terminated. The TS68020 then executes this operation word in place of the breakpoint instruction. The debugger hardware can count the number of executions of each breakpoint and halt execution after a pre-determined number of cycles.

Multi-processing

To further support multi-processing with the TS68020, a compare and swap instruction, CAS, has been added. This instruction makes use of the read-modify-write cycle to compare two operands and swap a third operand pending the results of the compare. A variant of this instruction, CAS2, performs similarly comparing dual operand pairs, and updating two operands.

These multi-processing operations are useful when using common memory to share or pass data between multiple processing elements. The read-modify-write cycle is an indivisible operand that allows reading and updating a “lock” operand used to control access to the common memory elements. The CAS2 instruction is more powerful since dual operands allow the “lock” to the checked and two values (i.e., both pointers in a doubly-linked list) to be updated according to the lock’s status, all in a single operation.

Module Support

The TS68020 includes support for modules with the call module (CALLM) and return from module (RTM) instructions. The CALLM instruction references a module descriptor. This descriptor contains control information for entry into the associated module. The CALLM instruction creates a module stack frame and stores the module state in that frame. The RTM instruction recovers the previous module state from the stack frame and returns to the calling module.

The module interface also provides a mechanism for finer resolution of access control by external hardware. Although the TS68020 does not interrupt the access control information, it does communicate with external hardware when the access control is to be changed, and relies on the external hardware to verify that the changes are legal.

CALLM and RTM, when used as subroutine calls and returns with proper descriptor formats, cause the TS68020 to perform the necessary actions to verify legitimate access to modules.

Virtual Memory/Machine Concepts

The full addressing range of the TS68020 is 4-Gbyte (4, 294, 967, 296). However, most TS68020 systems implement a smaller physical memory. Nonetheless, by using virtual memory techniques, the system can be made to appear to have a full 4-Gbyte of physical memory available to each user program. These techniques have been used for many years in large mainframe computers and minicomputers. With the TS68020 (as with the TS68010 and TS68012), virtual memory can be fully supported in microprocessor-based systems.

In a virtual memory system, a user program can be written as though it has a large amount of memory available to it when actually only a smaller amount of memory is physically present in the system. In a similar fashion, a system provides user programs access to other devices that are not physically present in the system, such as tape drives, disk drives, printers, or terminals. With proper software emulation, a physical system can be made to appear to a user program as any other 68000 computer system and the program may be given full access to all of the resources of that emulated system. Such an emulator system is called a virtual machine.

Virtual Memory

The basic mechanism for supporting virtual memory is to provides a limited amount of high-speed physical memory that can be accessed directly by the processor while maintaining of a much larger “virtual” memory on secondary storage devices such as large capacity disk drives. When the processor attempts to access a location in the virtual memory map that is not resident in the physical memory (referred to as a page fault), the access to that location is temporarily suspended while the necessary data is fetched from secondary storage and placed in physical memory; the suspended access is then either restarted or continued.

Other microprocessors in the TS68000 Family can operate any TS68000 co-processor even though they may not have the hardware implementation of the co-processor interface as does the TS68020. Since the co-processor is operated through the co-processor interface registers which are accessed via normal asynchronous bus cycles, the co-processor may be used as a peripheral device. Software easily emulates the communication protocol by addressing the co-processor interface registers appropriately and passing the necessary commands and operands required by the co-processor.

The co-processor interface registers are implemented by the co-processor in addition to those registers implemented as extensions to the TS68020 programmer's model. For example, the TS68881 implements the co-processor interface registers shown in Table 10 and the registers in the programming model, including eight 80-bit floating-point data registers and three 32-bit control/status registers used by the TS68881 programmer.

Table 10. Co-processor Interface Registers

Register	Function	R/W
Response	Requests Action from CPU	R
Control	CPU	W
Save	Initiate Save of Internal State	R
Restore	Initiate Restore of Internal State	R/W
Operation Word	Current Co-processor Instruction	W
Command Word	Co-processor Specific Command	W
Condition Word	Condition to be Evaluated	W
Operand	32-bit Operand	R/W
Register Select	Specifies CPU Register or Mask	R
Instruction Address	Pointer to Co-processor Instruction	R/W
Operand Address	Pointer to Co-processor Operand	R/W

Table 11. Co-processor Primitives

Processor Synchronization Busy with Current Instruction Proceed with Next Instruction, If No Trace Service Interrupts and Re-query, If Trace Enable Proceed with Execution, Condition True/False
Instruction Manipulation Transfer Operation Word Transfer Words from Instruction Stream
Exception Handling Take Privilege Violation if S Bit Not Set Take Pre-Instruction Exception Take Mid-Instruction Exception Take Post-Instruction Exception

Table 11. Co-processor Primitives (Continued)

General Operand Transfer
Evaluate and Pass (Ea.)
Evaluate (Ea.) and Transfer Data
Write to Previously Evaluated (Ea.)
Take Address and Transfer Data
Transfer to/from Top of Stack
Register Transfer
Transfer CPU Register
Transfer CPU Control Register
Transfer Multiple CPU Registers
Transfer Multiple Co-processor Registers
Transfer CPU SR and/or ScanPC

Up to eight processors are supported in a single system with a system-unique co-processor identifier encoded in the co-processor instruction. When accessing a co-processor, the TS68020 executes standard read and write bus cycle in CPU address space, as encoded by the function codes, and places the co-processor identifier on the address bus to be used by chip-select logic to select the particular co-processor. Since standard bus cycle are used to access the co-processor, the co-processor may be located according to system design requirements, whether it be located on the micro-processor local bus, on another board on the system bus, or any other place where the chip-select and co-processor protocol using standard TS68000 bus cycles can be supported.

Co-processor Protocol

Interprocessor transfers are all initiated by the main processor during co-processor instruction execution. During the processing of a co-processor instruction, the main processor transfers instruction information and data to the associated co-processor, and receives data, requests, and status information from the co-processor. These transfers are all based on the TS68000 bus cycles.

The typical co-processor protocol which the main processor follows is:

a) The main processor initiates the communications by writing command information to a location in the co-processor interface.

b) The main processor reads the co-processor response to that information.

1) The response may indicate that the co-processor is busy, and the main processor should again query the co-processor. This allows the main processor and co-processor to synchronize their concurrent operations.

2) The response may indicate some exception condition; the main processor acknowledges the exception and begins exception processing.

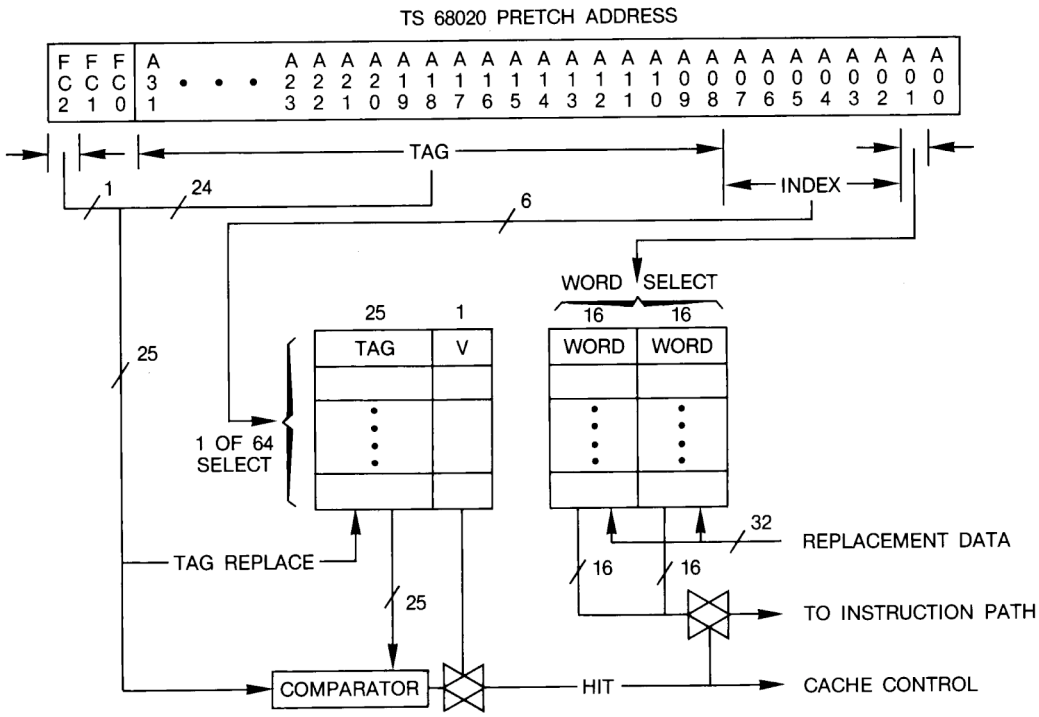
3) The response may indicate that the co-processor needs the main processor to perform some service such as transferring data to or from the co-processor. The co-processor may also request that the main processor query the co-processor again after the service is complete.

4) The response may indicate that the main processor is not needed for further processing of the instruction. The communication is terminated, and the main processor is free to begin execution of the next instruction. At this point in the co-processor protocol, as the main processor continues to execute the instruction stream, the main processor may operate concurrently with the co-processor.

Second, and probably the most important benefit of the cache, is that it allows instruction stream fetches and operand accesses to proceed in parallel. For example, if the TS68020 requires both an instruction stream access and an operand access, and the instruction is resident in the cache, the operand access will proceed unimpeded rather than being queued behind the instruction fetch. Similarly, the TS68020 is fully capable of executing several internal instructions (instructions that do not require the bus) while completing an operand access for another instruction.

The TS68020 instruction cache is a 256-byte direct mapped cache organized as 64 long word entries. Each cache entry consists of a tag field made up of the upper 24 address bits, the FC2 (user/supervisor) value, one valid bit, and 32-bit of instruction data (Figure 22).

Figure 22. TS68020 On-chip Cache Organization



The TS68020 employs a 32-bit data bus and fetches instructions on long word address boundaries. Hence, each 32-bit instruction fetch brings in two 16-bit instruction words which are then written into the on-chip cache. When the cache is enabled, the subsequent prefetch will find the next 16-bit instruction word is already present in the cache and the related bus cycle is saved. If the cache were not enabled, the subsequent prefetch will find the bus controller still holds the full 32-bit and can satisfy the prefetch and again save the related bus cycle. So, even when the on-chip instruction cache is not enabled, the bus controller provides an instruction “cache hit” rate up to 50%.

Package Mechanical Data

Figure 23. 114-lead - Ceramic Pin Grid Array

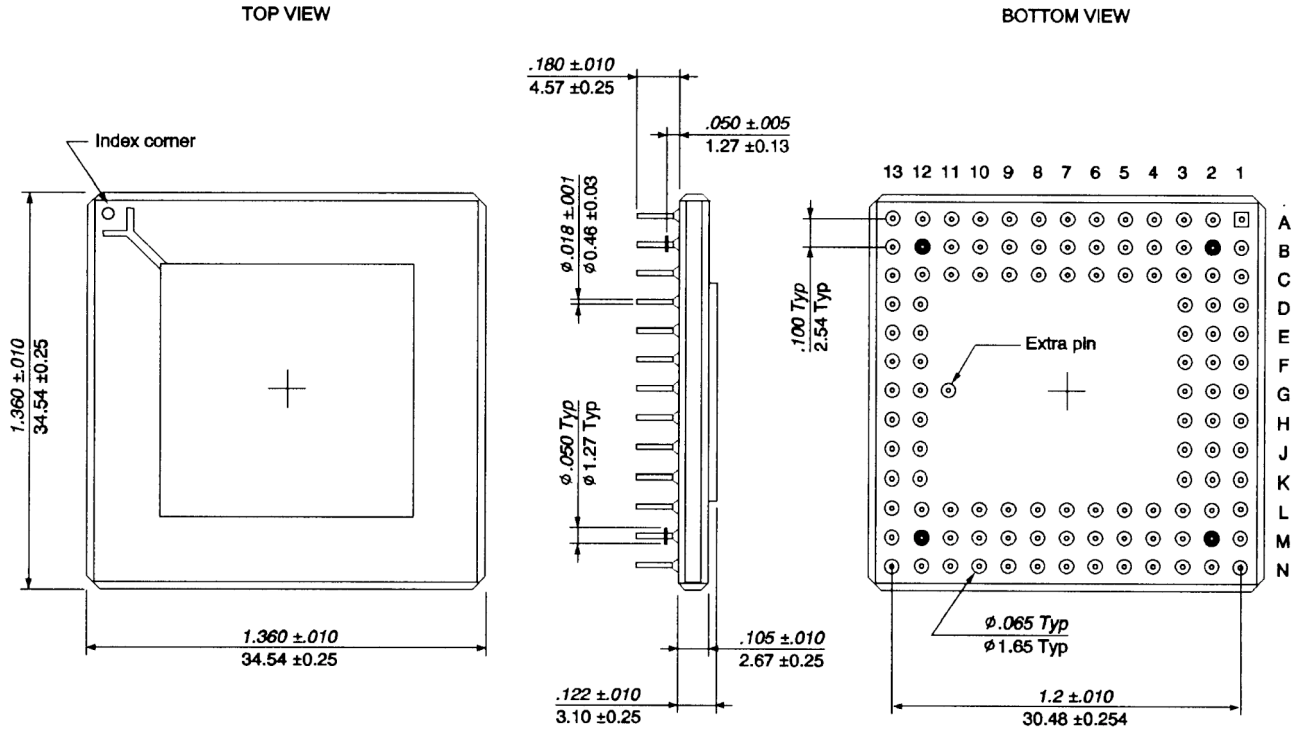
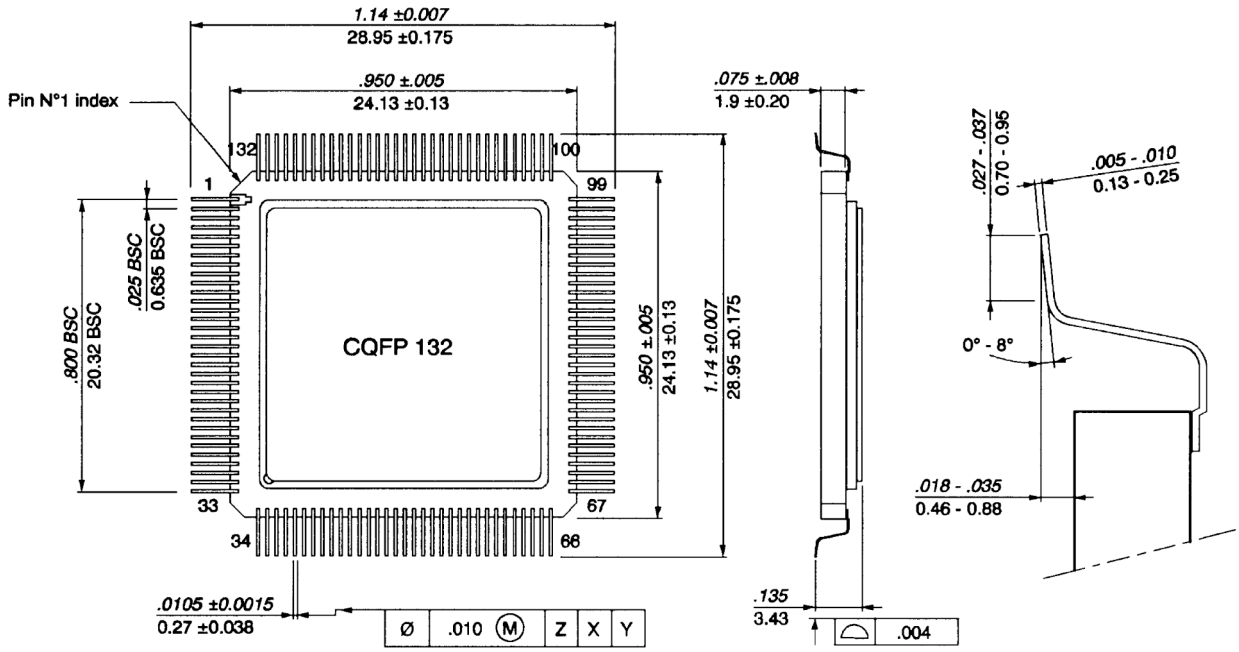


Figure 24. 132 Pins - Ceramic Quad Flat Pack



Mass

PGA 114 - 6 grams typically
CQFP 132 - 14 grams typically

Terminal Connections

114-lead - Ceramic Pin Grid Array

See Figure 2.

132-lead - Ceramic Quad Flat Pack

See Figure 3.

Ordering Information

Hi-REL Product

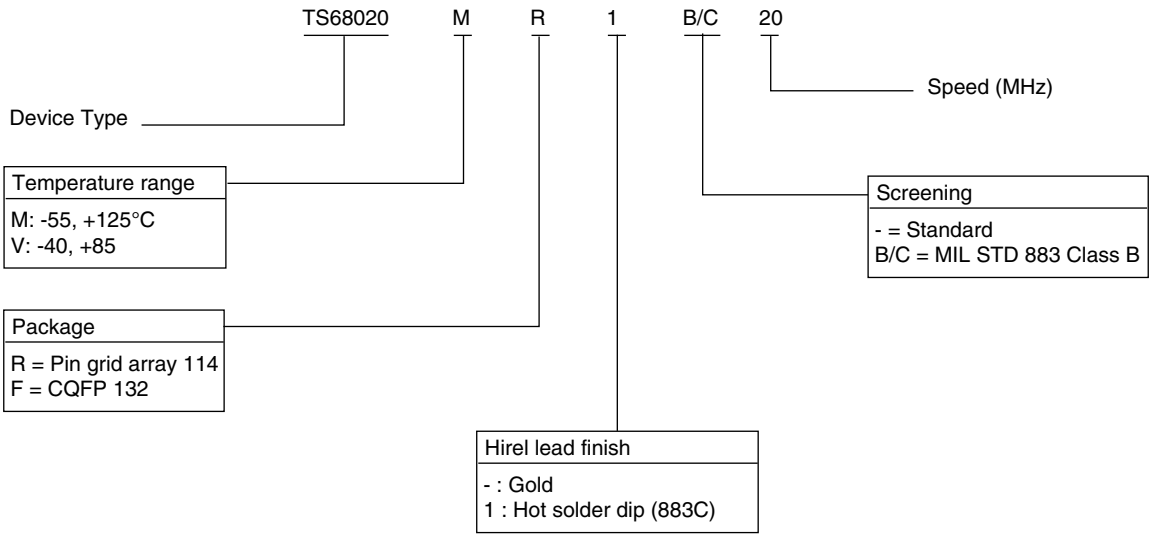
Commercial Atmel Part-Number	Norms	Package	Temperature Range T_c (°C)	Frequency (MHz)	Drawing Number
TS68020MRB/C16	MIL-STD-883	PGA 114	-55/+125	16.67	-
TS68020MR1B/C16	MIL-STD-883	PGA 114/tin	-55/+125	16.67	-
TS68020MRB/C20	MIL-STD-883	PGA 114	-55/+125	20	-
TS68020MR1B/C20	MIL-STD-883	PGA 114/tin	-55/+125	20	-
TS68020MRB/C25	MIL-STD-883	PGA 114	-55/+125	25	-
TS68020MR1B/C25	MIL-STD-883	PGA 114/tin	-55/+125	25	-
TS68020MFB/C16	MIL-STD-883	CQFP 132	-55/+125	16.67	-
TS68020MF1B/C16	MIL-STD-883	CQFP 132/tin	-55/+125	16.67	-
TS68020MFB/C20	MIL-STD-883	CQFP 132	-55/+125	20	-
TS68020MF1B/C20	MIL-STD-883	CQFP 132/tin	-55/+125	20	-
TS68020MFB/C25	MIL-STD-883	CQFP 132	-55/+125	25	-
TS68020MF1B/C25	MIL-STD-883	CQFP 132/tin	-55/+125	25	-
TS68020DESC02XA	DESC	PGA 114/tin	-55/+125	16.67	5962-8603202XA
TS68020DESC03XA	DESC	PGA 114/tin	-55/+125	20	5962-8603203XA
TS68020DESC04XA	DESC	PGA 114/tin	-55/+125	25	5962-8603204XA
TS68020DESC02XC	DESC	PGA 114	-55/+125	16.67	5962-8603202XC
TS68020DESC03XC	DESC	PGA 114	-55/+125	20	5962-8603203XC
TS68020DESC04XC	DESC	PGA 114	-55/+125	25	5962-8603204XC
TS68020DESC02YA	DESC	CQFP 132/tin	-55/+125	16.67	5962-8603202YA
TS68020DESC03YA	DESC	CQFP 132/tin	-55/+125	20	5962-8603203YA
TS68020DESC04YA	DESC	CQFP 132/tin	-55/+125	25	5962-8603204YA
TS68020DESC02YC	DESC	CQFP 132	-55/+125	16.67	5962-8603202YC
TS68020DESC03YC	DESC	CQFP 132	-55/+125	20	5962-8603203YC
TS68020DESC04YC	DESC	CQFP 132	-55/+125	25	5962-8603204YC

Standard Product

Commercial Atmel Part-Number	Norms	Package	Temperature Range T_c (°C)	Frequency (MHz)	Drawing Number
TS68020VR16	Internal Standard	PGA 114	-40/+85	16.67	Internal
TS68020VR20	Internal Standard	PGA 114	-40/+85	20	Internal
TS68020VR25	Internal Standard	PGA 114	-40/+85	25	Internal
TS68020MR16	Internal Standard	PGA 114	-55/+125	16.67	Internal
TS68020MR20	Internal Standard	PGA 114	-55/+125	20	Internal
TS68020MR25	Internal Standard	PGA 114	-55/+125	25	Internal

Standard Product

Commercial Atmel Part-Number	Norms	Package	Temperature Range T_c (°C)	Frequency (MHz)	Drawing Number
TS68020VF16	Internal Standard	CQFP 132	-40/+85	16.67	Internal
TS68020VF120	Internal Standard	CQFP 132	-40/+85	20	Internal
TS68020VF25	Internal Standard	CQFP 132	-40/+85	25	Internal
TS68020MF16	Internal Standard	CQFP 132	-55/+125	16.67	Internal
TS68020MF20	Internal Standard	CQFP 132	-55/+125	20	Internal
TS68020MF25	Internal Standard	CQFP 132	-55/+125	25	Internal



Note: For availability of the different versions, contact your Atmel sales office.