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Understanding Embedded - Microprocessors

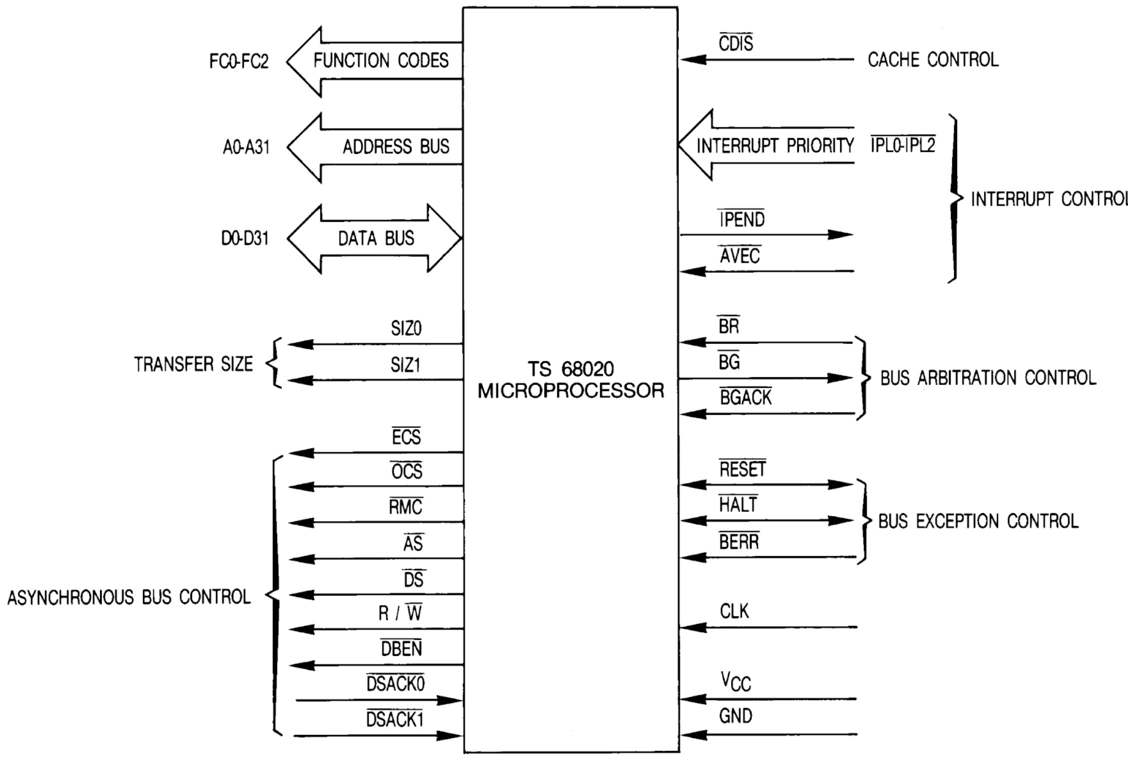
Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	68000
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	25MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 85°C (TC)
Security Features	-
Package / Case	114-BCPGA
Supplier Device Package	114-CPGA (34.54x34.54)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts68020vr1-25

Figure 4. Functional Signal Groups



Signal Description

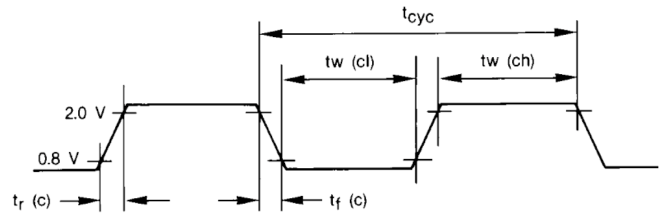
Figure 4 illustrates the functional signal groups and Table 1 lists the signals and their function.

The V_{CC} and GND pins are separated into four groups to provide individual power supply connections for the address bus buffers, data bus buffers, and all other output buffers and internal logic.

Group	V_{CC}	GND
Address Bus	A9, D3	A10, B9,C3, F12
Data Bus	M8, N8, N13	L7, L11, N7, K3
Logic	D1, D2, E3, G11, G13	G12, H13, J3, K1
Clock	—	B1

This device contains protective circuitry against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

Figure 5. Clock Input Timing Diagram



Note: Timing measurements are referenced to and from a low voltage of 0.8V and a high voltage of 2.0V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8V and 2.0V.

Table 4. Thermal Characteristics at 25°C

Package	Symbol	Parameter	Value	Unit
PGA 114	θ_{JA}	Thermal Resistance - Ceramic Junction to Ambient	26	°C/W
	θ_{JC}	Thermal Resistance - Ceramic Junction to Case	5	°C/W
CQFP 132	θ_{JA}	Thermal Resistance - Ceramic Junction to Ambient	34	°C/W
	θ_{JC}	Thermal Resistance - Ceramic Junction to Case	2	°C/W

Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \cdot V_{CC}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K + (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273) + \theta_{JA} \cdot P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part K can be determined from equation **(3)** by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations **(1)** and **(2)** iterativley for any value of T_A.

For dynamic characteristics (Table 6), test methods refer to IEC 748-2 method, where existing.

Indication of “min.” or “max.” in the column “test temperature” means minimum or maximum operating temperature.

Table 5. Static Characteristics. V_{CC} = 5.0V_{DC} ± 10%; GND = 0V_{DC}; T_c = -55/+125°C or -40/+85°C (Figure 4 to Figure 8)

Symbol	Parameter	Condition	Min	Max	Units
I_{CC}	Maximum Supply Current	V_{CC} = 5.5V T_{case} -55°C to +25°C		333	mA
I_{CC}	Maximum Supply Current	V_{CC} = 5.5V T_{case} = 125°C		207	mA
V_{IH}	High Level Input Voltage	V_O = 0.5V or 2.5 V_{CC} = 4.5V to 5.5V	2.0	V_{CC}	V
V_{IL}	Low Level Input Voltage	V_O = 0.5V or 2.4V V_{CC} = 4.5V to 5.5V	-0.5	0.8	V
V_{OH}	High Level Output Voltage All Outputs	I_{OH} = 400 µA	2.4		V
V_{OL}	Low Level Output Voltage Outputs A0-A31, FC0-FC2, D0-D31, SIZ0-SIZ1, $\overline{BG}$	I_{OL} = 3.2 mA Load Circuit as Figure 8 R = 1.22 kΩ		0.5	V
V_{OL}	Low Level Output Voltage Outputs $\overline{AS}$, $\overline{DS}$, $\overline{RMC}$, R/$\overline{W}$, $\overline{DBEN}$, $\overline{IPEND}$	I_{OL} = 5.3 mA Load Circuit as Figure 8 R = 740Ω		0.5	V
V_{OL}	Low Level Output Voltage Outputs $\overline{ECS}$, $\overline{OCS}$	I_{OL} = 2.0 mA Load Circuit as Figure 8 R = 2 kΩ		0.5	V
V_{OL}	Low Level Output Voltage Outputs $\overline{HALT}$, $\overline{RESET}$	I_{OL} = 10.7 mA Load Circuit as Figure 6 and Figure 7		0.5	V
$\mid I_{IN} \mid$	Input Leakage Current (High and Low State)	-0.5V ≤ V_{IN} ≤ V_{CC} (Max)		2.5	µA
$\mid I_{OHZ} \mid$	High level leakage current at three-state outputs Outputs A0-A31, $\overline{AS}$, $\overline{DBEN}$, $\overline{DS}$, D0-D31, R/$\overline{W}$, FC0-FC2, $\overline{RMC}$, SIZ0-SIZ1	V_{OH} = 2.4V		2.5	µA
$\mid I_{OLZ} \mid$	Low Level Leakage Current at Three-state Outputs Outputs A0-A31, $\overline{AS}$, $\overline{DBEN}$, $\overline{DS}$, D0-D31 R/$\overline{W}$, FC0-FC2, $\overline{RMC}$, SIZ0-SIZ1	V_{OL} = 0.5V		2.5	µA
I_{OS}	Output Short-circuit Current (Any Output)	V_{CC} = 5.5V V_O = 0V (Pulsed. Duration 1 ms Duty Cycle 10:1)		200	mA

Table 6. Dynamic Electrical Characteristics (Continued)

Symbol	Parameter	Interval Number	68020-16		68020-20		68020-25		Unit	Notes
			Min	Max	Min	Max	Min	Max		
f	Frequency of Operation		8.0	16.67	12.5	20.0	12.5	25	MHz	
t_{RADC}	R/W Asserted to Data Bus Impedance Change	55	30		25		20			(11)
t_{HRPW}	$\overline{RESET}$ Pulse Width (Reset Instruction)	56	512		512		512		Clks	(11)
t_{BNHN}	$\overline{BERR}$ Negated to $\overline{HALT}$ Negated (Rerun)	57	0		0		0		ns	(11)
t_{GANBD}	$\overline{BGACK}$ Negated to Bus Driven	58	1		1		1		Clks	(10)(11)
t_{GNBD}	$\overline{BG}$ Negated to Bus Driven	59	1		1		1		Clks	(10)(11)

Notes:
1. This number can be reduced to 5 nanoseconds if the strobes have equal loads.
2. If the asynchronous setup time (= 47) requirements are satisfied, the DSACKx low to data setup time (= 31) and $\overline{DSACKx}$ low to $\overline{BERR}$ low setup time (= 48) can be ignored. The data must only satisfy the data in to clock low setup time (= 27) for the following clock cycle, $\overline{BERR}$ must only satisfy the late $\overline{BERR}$ low to clock setup time (= 27) for the following clock cycle.
3. This parameter specifies the maximum allowable skew between $\overline{DSACK0}$ to $\overline{DSACK1}$ asserted or $\overline{DSACK1}$ to $\overline{DSACK0}$ asserted pattern = 47 must be met by $\overline{DSACK0}$ and $\overline{DSACK1}$.
4. In the absence of $\overline{DSACKx}$, $\overline{BERR}$ is an asynchronous input using the asynchronous input setup time (= 47).
5. $\overline{DBEN}$ may stay asserted on consecutive write cycles.
6. Actual value depends on the clock input waveform.
7. This pattern indicates the minimum high time for $\overline{ECS}$ and $\overline{OCS}$ in the event of an internal cache hit followed immediately by a cache miss or operand cycle.
8. This specification guarantees operations with the 68881 co-processor, and defines a minimum time for DS negated to AS asserted (= 13A). Without this parameter, incorrect interpretation of = 9A and = 15 would indicate that the 68020 does not meet 68881 requirements.
9. This pattern allows the systems designer to guarantee data hold times on the output side of data buffers that have output enable signals generated with $\overline{DBEN}$.
10. Guarantees that an alternate bus master has stopped driving the bus when the 68020 regains control of the bus after an arbitration sequence.
11. Cannot be tested. Provided for system design purposes only.
12. T_{case} = -55°C and +130°C in a Power off condition under Thermal soak for 4 minutes or until thermal equilibrium. Electrical parameters are tested "instant on" 100 m sec. after power is applied.
13. All outputs unload except for load capacitance. Clock = fmax,
    LOW: $\overline{HALT}$, $\overline{RESET}$
    HIGH: $\overline{DSACK0}$, $\overline{DSACK1}$, $\overline{CDIS}$, $\overline{IPL0\text{-}IPL2}$, $\overline{DBEN}$, $\overline{AVEC}$, $\overline{BERR}$.

Test Conditions Specific to the Device

Loading Network

The applicable loading network shall be defined in column “Test conditions” of Table 6, referring to the loading network number as shown in Figure 6, Figure 7, Figure 8 below.

Figure 6. RESET Test Loads

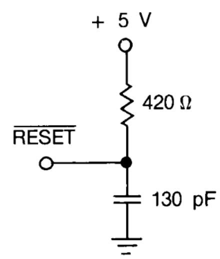


Figure 7. HALT Test Load

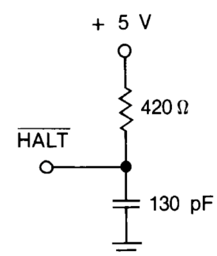


Figure 8. Test Load

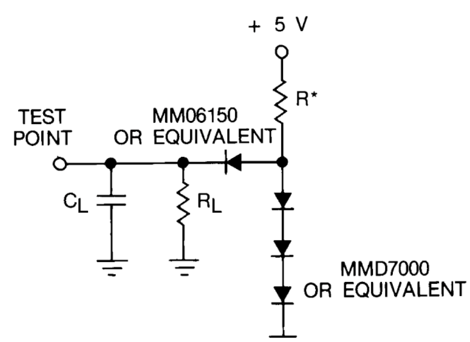


Table 7. Load Network

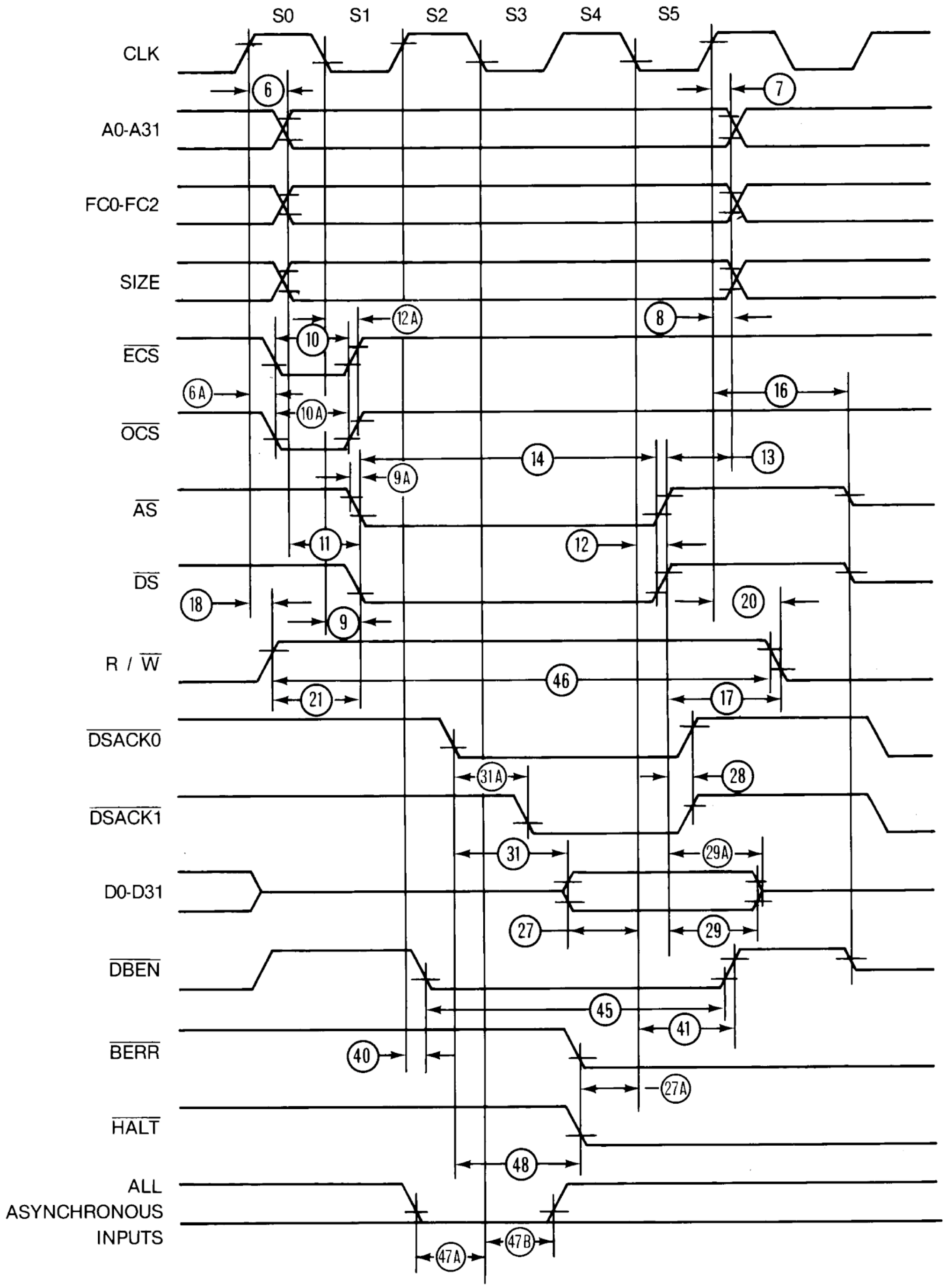
Load NBR	Figure	R	R_L	C_L	Output Application
1	7	2 k	6.0 k	50 pF	$\overline{OCS}$, $\overline{ECS}$
2	7	1.22 k	6.0 k	130 pF	A0-A31, D0-D31, $\overline{BG}$, FC0-FC2, SIZ0-SIZ1
3	7	0.74 k	6.0 k	130 pF	$\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, $\overline{RMC}$, $\overline{DBEN}$, $\overline{IPEND}$

Note: 1. Equivalent loading may be simulated by the tester.

Time Definitions

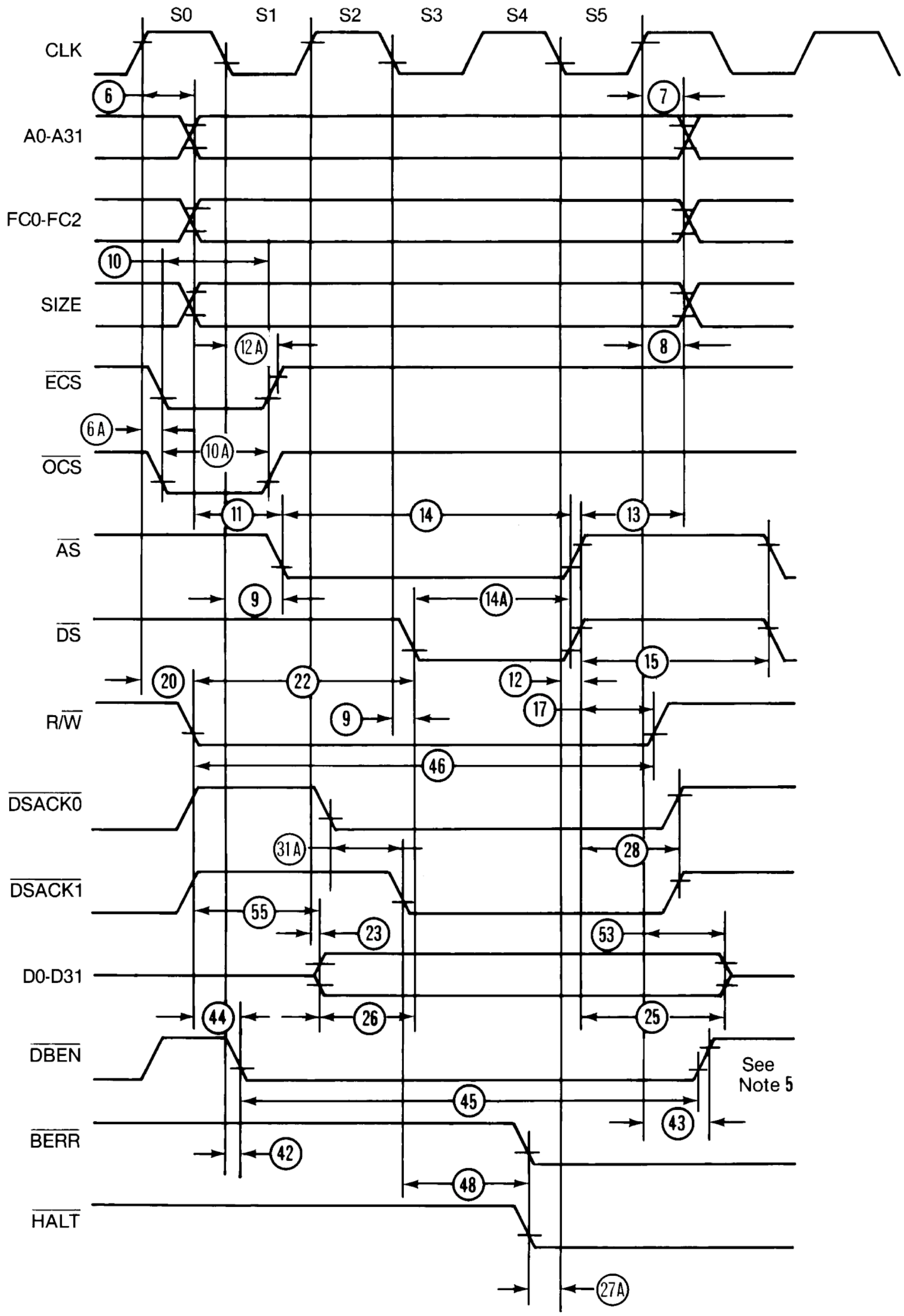
The times specified in Table 6 as dynamic characteristics are defined in Figure 9 below, by a reference number given the column “interval N°” of the tables together with the relevant figure number.

Figure 9. Read Cycle Timing Diagram



Note: Timing measurements are referenced to and from a low voltage of 0.8V and a high voltage of 2.0V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8V and 2.0V.

Figure 10. Write Cycle Timing Diagram (Continued)



Note: Timing measurements are referenced to and from a low voltage of 0.8V and a high voltage of 2.0V, unless otherwise noted. The voltage swing thorough this range should start outside and pass through the range such that the rise or fall will be linear between 0.8V and 2.0V.

Input and Output Signals for Dynamic Measurements

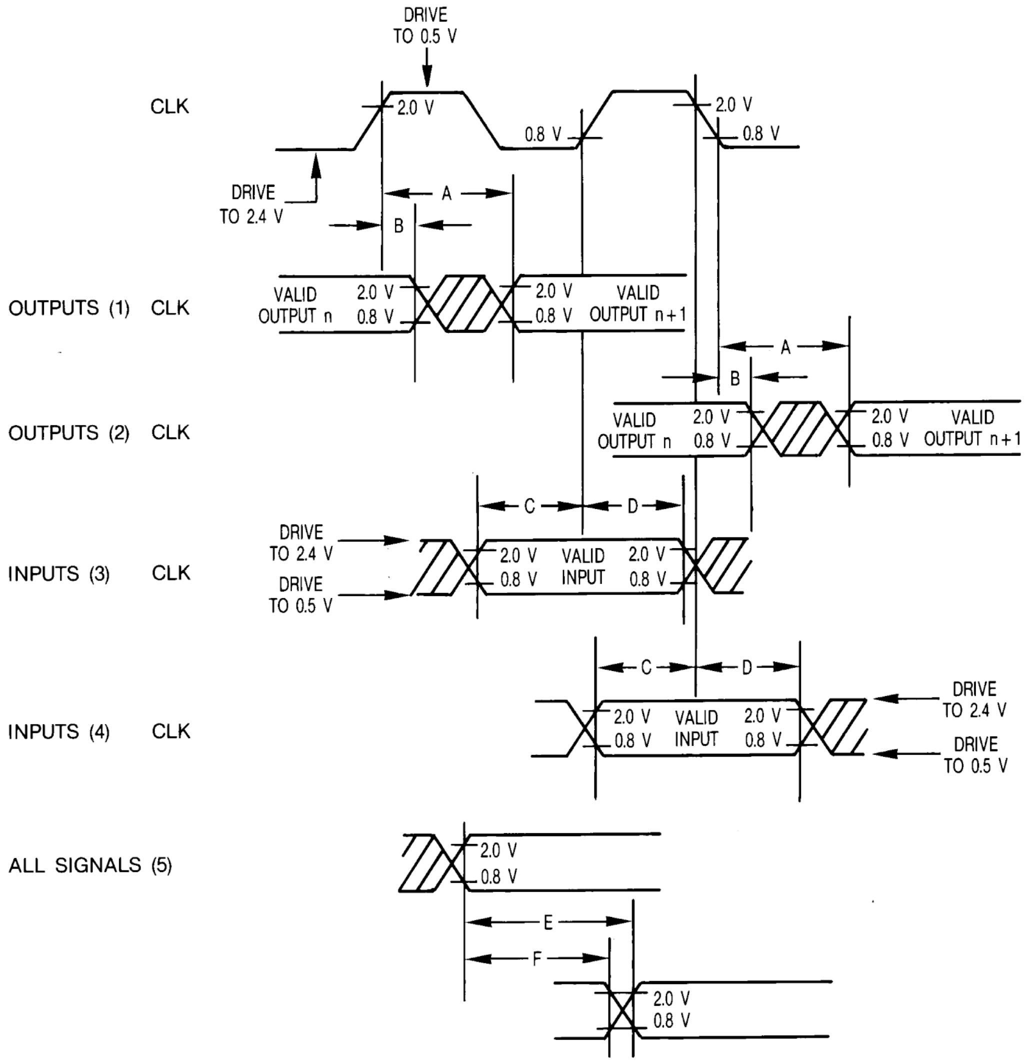
AC Electrical Specifications Definitions

The AC specifications presented consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of the TS68020 clock input and, possibly, relative to one or more other signals.

The measurement of the AC specifications is defined by the waveforms in Figure 12. In order to test the parameters guaranteed by Atmel, inputs must be driven to the voltage levels specified in Figure 12. Outputs of the TS68020 are specified with minimum and/or maximum limits, as appropriate, and are measured as shown. Inputs to the TS68020 are specified with minimum and, as appropriate, maximum setup and hold times, and are measurement as shown. Finally, the measurements for signal-to-signal specification are also shown.

Note that the testing levels used to verify conformance of the TS68020 to the AC specifications does not affect the guaranteed DC operation of the device as specified in the DC electrical characteristics.

Figure 12. Drive Levels and Test Points for AC Specification



Legend:

A) Maximum Output Delay Specification

B) Minimum Output Hold Time

C) Minimum Input Setup Time Specification

D) Minimum Input Hold Time Specification

E) Signal Valid to Signal Valid Specification (Maximum or Minimum)

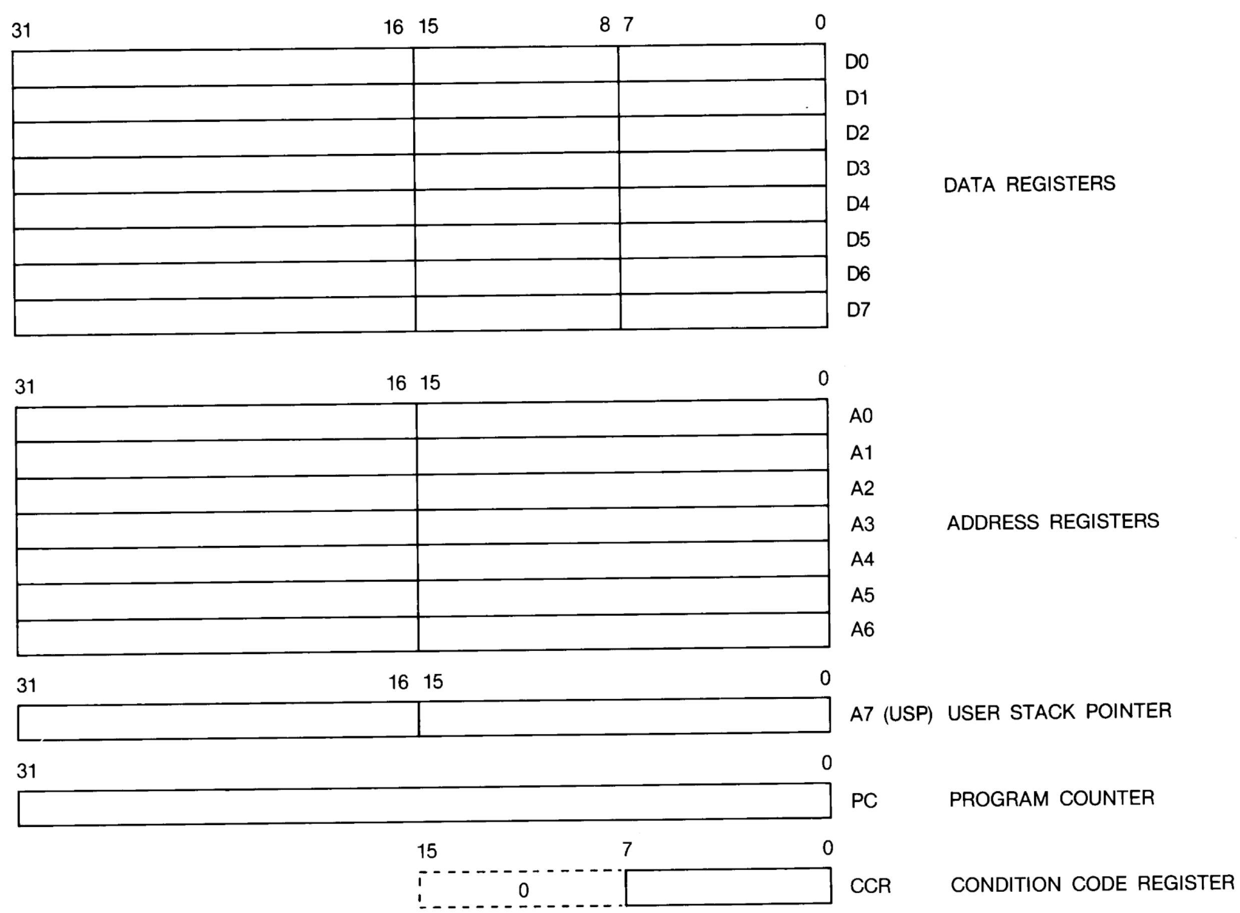
F) Signal Valid to Signal Invalid Specification (Maximum or Minimum)

Notes:
1. This output timing is applicable to all parameters specified relative to the rising edge of the clock.
2. This out put timing is applicable to all parameters specified relative to the falling edge of the clock.
3. This input timing is applicable to all parameters specified relative to the falling edge of the clock.
4. This input timing is applicable to all parameters specified relative to the falling edge of the clock.
5. This timing is applicable to all parameters specified relative to the assertion/negation of another signal.

The TS68000 Family processors distinguish address spaces as supervisor / used and program/data. These four combinations are specified by the function code pins (FC0/FC1/FC2) during bus cycles, indication the particular address space. Using the function codes, the memory sub-system can distinguish between authorized access (supervisor mode is privileged access) and unauthorized access (user mode may not have access to supervisor program or data areas). To support the full privileges of the supervisor, the alternate function code registers allow the supervisor to specify an access to user program or data areas by preloading the SFC/DFC registers appropriately.

The cache registers (control — CACR, address — CAAR) allow software manipulation of the on-chip instruction cache. Control and status accesses to the instruction cache are provided by the cache control register (CACR), while the cache address register (CAAR) holds the address for those cache control functions that require an address.

Figure 19. User Programming Model



The 18 addressing modes, shown in Table 8, include nine basic types:

- Register Direct
- Register Indirect
- Register Indirect with Index
- Memory Indirect
- Program Counter Indirect with Displacement
- Program Counter Indirect with Index
- Program Counter Memory Indirect
- Absolute
- Immediate

The register indirect addressing modes support postincrement, predecrement, offset, and indexing. Programmers find these capabilities particularly useful for handling advanced data structures common to sophisticated applications and high level languages. The program counter relative mode also has index and offset capabilities; programmers find that this addressing mode is required to support position-independent software. In addition to these addressing modes, the TS68020 provides data operand sizing and scaling; these features provide performance enhancements to the programmer.

Table 8. TS68020 Addressing Modes

Addressing Modes	Syntax
Register Direct	
Data Register Direct	Dn
Address Register Direct	An
Register Indirect	
Address Register Indirect	(An)
Address Register Indirect with Post Increment	(An) +
Address Register Indirect with Predecrement	– (An)
Address Register Indirect with Displacement	(d_{16}An)
Register Indirect with Index	
Address Register Indirect with Index (8-bit Displacement)	(d_8, An, Xn)
Address Register Indirect with Index (Base Displacement)	(bd, An, Xn)
Memory Indirect	
Memory Indirect Post-Indexed	([bd, An], Xn, od)
Memory Indirect Pre-Indexed	([bd, An, Xn], od)
Program Counter Indirect with Displacement	(d_{16}, PC)
Program Counter Indirect with Index	
PC Indirect with Index (8-bit Displacement)	(d_8, PC, Xn)
PC Indirect with Index (Base Displacement)	(bd, PC, Xn)
Program Counter Memory Indirect	
PC Memory Indirect Post-Indexed	([bd, PC], Xn, od)
PC Memory Indirect Pre-Indexed	([bd, PC, Xn]), od)

Instruction Set Overview

The TS68020 instruction set is shown in Table 9. Special emphasis has been given to the instruction set's support of structured high-level languages and sophisticated operating systems. Each instruction, with few exceptions, operates on bytes, words, and long words and most instructions can use any of the 18 addressing modes. Many instruction extensions have been made on the TS68020 to take advantage of the full 32-bit operation where, on the earlier 68000 Family members, only 8 and 16 bits values were used. The TS68020 is upward source- and object-level code compatible with the family because it supports all of the instructions that previous family members offer. Additional instructions are now provided by the TS68020 in support of its advanced features.

Table 9. Instruction Set

Mnemonic	Description
ABCD	Add Decimal with Extend
ADD	Add
ADDA	Add Address
ADDI	Add Immediate
ADDQ	Add Quick
ADDX	Add with Extend
AND	Logical AND
ANDI	Logical AND Immediate
ASL, ASR	Arithmetic Shift Left and Right
Bcc	Branch Conditionally
BCHG	Test Bit and Change
BCLR	Test Bit and Clear
BFCHG	Test Bit Field and Change
BFCLR	Test Bit Field and Clear
BFEXTS	Signed Bit Field Extract
BFEXTU	Unsigned Bit Field Extract
BFFFO	Bit Field Find First One
BFINS	Bit Field Insert
BFSET	Test Bit Field and Set
BFTST	Test Bit Field
BKPT	Breakpoint
BRA	Branch
BSET	Test Bit and Set
BSR	Branch to Subroutine
BTST	Test Bit

Table 9. Instruction Set (Continued)

Mnemonic	Description
OR	Logical Inclusive OR
ORI	Logical Inclusive OR Immediate
PACK	Pack BCD
PEA	Push Effective Address
RESET	Reset External Devices
ROL, ROR	Rotate Left and Right
ROXL, ROXR	Rotate with Extend Left and Right
RTD	Return and Deallocate
RTE	Return and Exception
RTM	Return from Module
RTR	Return and Restore Codes
RTS	Return from Subroutine
SBCD	Subtract Decimal with Extend
Scc	Set Conditionally
STOP	Stop
SUB	Subtract
SUBA	Subtract Address
SUBI	Subtract Immediate
SUBQ	Subtract Quick
SUBX	Subtract with Extend
SWAP	Swap Register Words
TAS	Test Operand and Set
TRAP	Trap
TRAPcc	Trap Conditionally
TRAPV	Trap on Overflow
TST	Test Operand
UNLK	Unlink
UNPK	Unpack BCD
Co-processor Instructions	
cpBCC	Branch Conditionally
cpDBcc	Test Co-processor Condition, Decrement and Branch
cpGEN	Co-processor General Instruction
cpRESTORE	Restore Internal State of Co-processor
cpSAVE	Save Internal State of Co-processor
cpScc	Set Conditionally
cpTRAPcc	Trap Conditionally

Multi-processing

To further support multi-processing with the TS68020, a compare and swap instruction, CAS, has been added. This instruction makes use of the read-modify-write cycle to compare two operands and swap a third operand pending the results of the compare. A variant of this instruction, CAS2, performs similarly comparing dual operand pairs, and updating two operands.

These multi-processing operations are useful when using common memory to share or pass data between multiple processing elements. The read-modify-write cycle is an indivisible operand that allows reading and updating a “lock” operand used to control access to the common memory elements. The CAS2 instruction is more powerful since dual operands allow the “lock” to the checked and two values (i.e., both pointers in a doubly-linked list) to be updated according to the lock’s status, all in a single operation.

Module Support

The TS68020 includes support for modules with the call module (CALLM) and return from module (RTM) instructions. The CALLM instruction references a module descriptor. This descriptor contains control information for entry into the associated module. The CALLM instruction creates a module stack frame and stores the module state in that frame. The RTM instruction recovers the previous module state from the stack frame and returns to the calling module.

The module interface also provides a mechanism for finer resolution of access control by external hardware. Although the TS68020 does not interrupt the access control information, it does communicate with external hardware when the access control is to be changed, and relies on the external hardware to verify that the changes are legal.

CALLM and RTM, when used as subroutine calls and returns with proper descriptor formats, cause the TS68020 to perform the necessary actions to verify legitimate access to modules.

Virtual Memory/Machine Concepts

The full addressing range of the TS68020 is 4-Gbyte (4, 294, 967, 296). However, most TS68020 systems implement a smaller physical memory. Nonetheless, by using virtual memory techniques, the system can be made to appear to have a full 4-Gbyte of physical memory available to each user program. These techniques have been used for many years in large mainframe computers and minicomputers. With the TS68020 (as with the TS68010 and TS68012), virtual memory can be fully supported in microprocessor-based systems.

In a virtual memory system, a user program can be written as though it has a large amount of memory available to it when actually only a smaller amount of memory is physically present in the system. In a similar fashion, a system provides user programs access to other devices that are not physically present in the system, such as tape drives, disk drives, printers, or terminals. With proper software emulation, a physical system can be made to appear to a user program as any other 68000 computer system and the program may be given full access to all of the resources of that emulated system. Such an emulator system is called a virtual machine.

Virtual Memory

The basic mechanism for supporting virtual memory is to provides a limited amount of high-speed physical memory that can be accessed directly by the processor while maintaining of a much larger “virtual” memory on secondary storage devices such as large capacity disk drives. When the processor attempts to access a location in the virtual memory map that is not resident in the physical memory (referred to as a page fault), the access to that location is temporarily suspended while the necessary data is fetched from secondary storage and placed in physical memory; the suspended access is then either restarted or continued.

The TS68020 will always transfer the maximum amount of data on all bus cycles; i.e., it always assumes the port is 32-bit wide when beginning the bus cycle. In addition, the TS68020 has no restrictions concerning alignment of operands in memory; long word operands need not be aligned on long word address boundaries. When misaligned data requires multiple bus cycles, the TS68020 aligned data requires multiple bus cycles, the TS68020 automatically runs the minimum number of bus cycles.

The Co-processor Concept

The co-processor interface is a mechanism for extending the instruction set of the TS68000 Family. Examples of these extensions are the addition of specialized data operands for the existing data types or, for the case of the floating point, the inclusion of new data types and operations for them as implemented by the TS68881 and TS68882 floating point co-processors.

The programmer's model for the TS68000 Family of microprocessors is based on sequential, non-concurrent instruction execution. This means each instruction is completely executed prior to the beginning of the next instruction. Hence, instructions do not operate concurrently in the programmer's model. Most microprocessors implement the sequential model which greatly simplifies the programmer responsibilities since sequencing control is automatic and discrete.

The TS68000 co-processor interface is designed to extend the programmer's model and it provides full support for the sequential, non-concurrent instruction execution model. Hence, instruction execution by the co-processor is assumed to not overlap with instruction execution with the main microprocessor. Yet, the TS68000 co-processor interface does allow concurrent operation when concurrency can be properly accommodated. For example, the TS68881 or TS68882 floating-point co-processor will allow the TS68020 to proceed executing instruction while the co-processor continues a floating-point operation, up to the point that the TS68020 sends another request to the co-processor. Adhering to the sequential execution model, the request to the co-processor continues a floating-point operation, up to the co-processor completes each TS68881 and TS68882 instruction before it starts the next, and the TS68020 is allowed to proceed as it can in a concurrent fashion.

co-processors are divided into two types by their bus utilization characteristics. A co-processor is a DMA co-processor if it can control the bus independent of the main processor. A co-processor is a non-DMA co-processor if it does not have the capability of controlling the bus. Both co-processor types utilize the same protocol and main processor resources. Implementation of a co-processor as a DMA or non-DMA type is based primarily on bus bandwidth of the co-processor, performance, and cost issues.

The communication protocol between the main processor and the co-processor necessary to execute a co-processor instruction is based on a group of co-processor interface registers (Table 10) which are defined for the TS68000 Family co-processor interface. The TS68020 hardware uses standard TS68000 asynchronous bus cycles to access the registers. Thus, the co-processor doesn't require a special bus hardware; the bus interface implemented by a co-processor for its interface register set must only satisfy the TS68020 address, data, and control signal timing to guarantee proper communication with the main processor. The TS68020 implements the communication protocol with all co-processors in hardware (and microcode) and handles all operations automatically so the programmer is only concerned with the instructions and data types provided by the co-processor as extensions to the TS68020 instruction set and data types.

Other microprocessors in the TS68000 Family can operate any TS68000 co-processor even though they may not have the hardware implementation of the co-processor interface as does the TS68020. Since the co-processor is operated through the co-processor interface registers which are accessed via normal asynchronous bus cycles, the co-processor may be used as a peripheral device. Software easily emulates the communication protocol by addressing the co-processor interface registers appropriately and passing the necessary commands and operands required by the co-processor.

The co-processor interface registers are implemented by the co-processor in addition to those registers implemented as extensions to the TS68020 programmer's model. For example, the TS68881 implements the co-processor interface registers shown in Table 10 and the registers in the programming model, including eight 80-bit floating-point data registers and three 32-bit control/status registers used by the TS68881 programmer.

Table 10. Co-processor Interface Registers

Register	Function	R/W
Response	Requests Action from CPU	R
Control	CPU	W
Save	Initiate Save of Internal State	R
Restore	Initiate Restore of Internal State	R/W
Operation Word	Current Co-processor Instruction	W
Command Word	Co-processor Specific Command	W
Condition Word	Condition to be Evaluated	W
Operand	32-bit Operand	R/W
Register Select	Specifies CPU Register or Mask	R
Instruction Address	Pointer to Co-processor Instruction	R/W
Operand Address	Pointer to Co-processor Operand	R/W

Table 11. Co-processor Primitives

Processor Synchronization Busy with Current Instruction Proceed with Next Instruction, If No Trace Service Interrupts and Re-query, If Trace Enable Proceed with Execution, Condition True/False
Instruction Manipulation Transfer Operation Word Transfer Words from Instruction Stream
Exception Handling Take Privilege Violation if S Bit Not Set Take Pre-Instruction Exception Take Mid-Instruction Exception Take Post-Instruction Exception

Package Mechanical Data

Figure 23. 114-lead - Ceramic Pin Grid Array

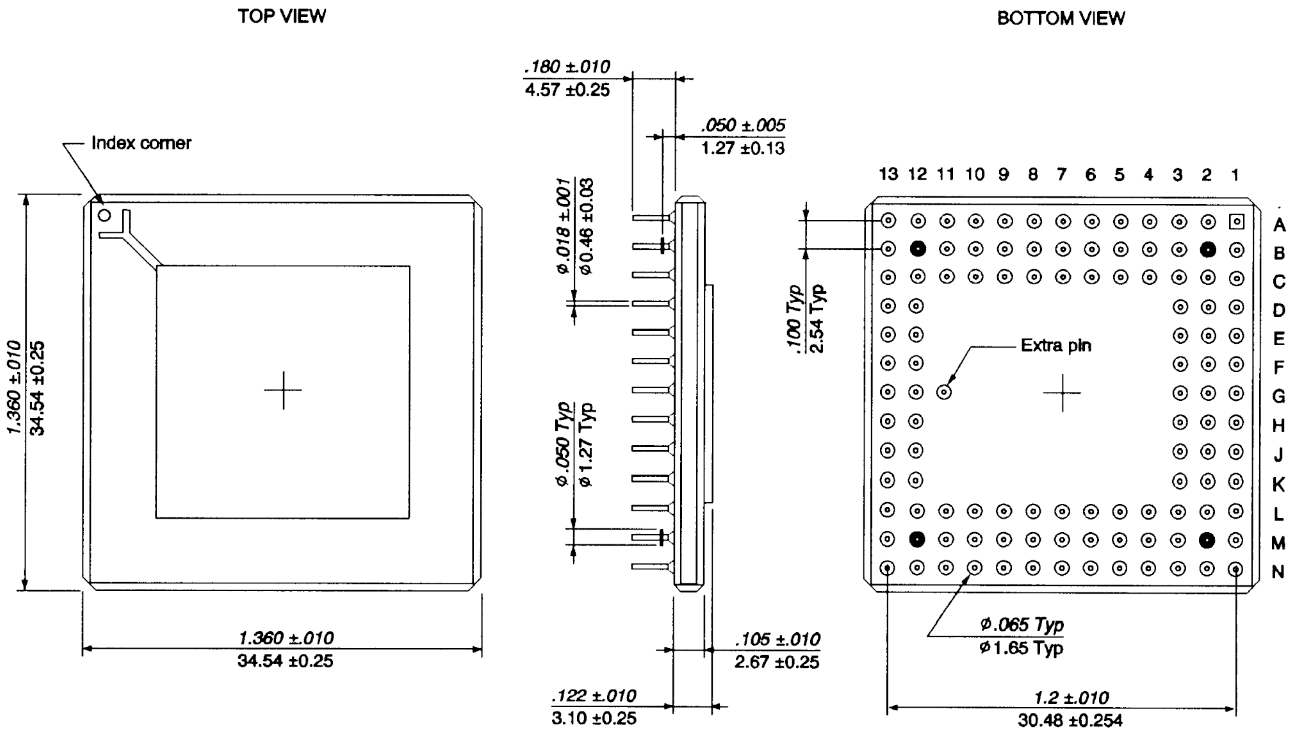
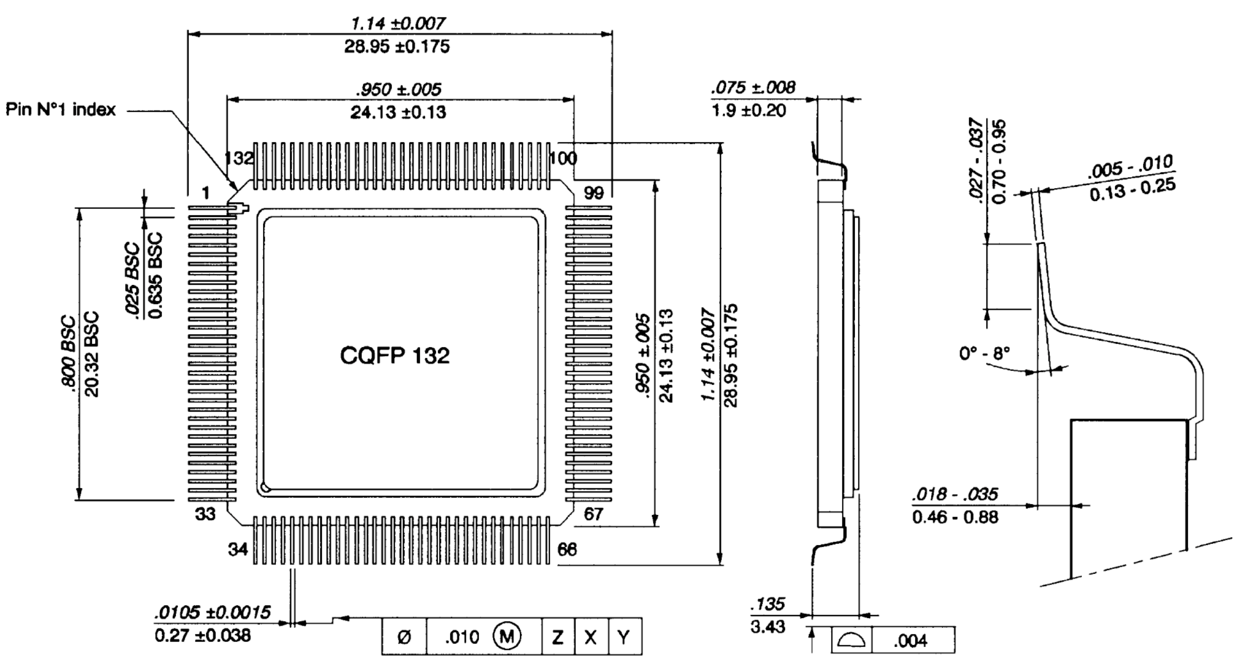


Figure 24. 132 Pins - Ceramic Quad Flat Pack



Mass

PGA 114 - 6 grams typically

CQFP 132 - 14 grams typically

Terminal Connections

114-lead - Ceramic Pin Grid Array

See Figure 2.

132-lead - Ceramic Quad Flat Pack

See Figure 3.

Ordering Information

Hi-REL Product

Commercial Atmel Part-Number	Norms	Package	Temperature Range T_c (°C)	Frequency (MHz)	Drawing Number
TS68020MRB/C16	MIL-STD-883	PGA 114	-55/+125	16.67	-
TS68020MR1B/C16	MIL-STD-883	PGA 114/tin	-55/+125	16.67	-
TS68020MRB/C20	MIL-STD-883	PGA 114	-55/+125	20	-
TS68020MR1B/C20	MIL-STD-883	PGA 114/tin	-55/+125	20	-
TS68020MRB/C25	MIL-STD-883	PGA 114	-55/+125	25	-
TS68020MR1B/C25	MIL-STD-883	PGA 114/tin	-55/+125	25	-
TS68020MFB/C16	MIL-STD-883	CQFP 132	-55/+125	16.67	-
TS68020MF1B/C16	MIL-STD-883	CQFP 132/tin	-55/+125	16.67	-
TS68020MFB/C20	MIL-STD-883	CQFP 132	-55/+125	20	-
TS68020MF1B/C20	MIL-STD-883	CQFP 132/tin	-55/+125	20	-
TS68020MFB/C25	MIL-STD-883	CQFP 132	-55/+125	25	-
TS68020MF1B/C25	MIL-STD-883	CQFP 132/tin	-55/+125	25	-
TS68020DESC02XA	DESC	PGA 114/tin	-55/+125	16.67	5962-8603202XA
TS68020DESC03XA	DESC	PGA 114/tin	-55/+125	20	5962-8603203XA
TS68020DESC04XA	DESC	PGA 114/tin	-55/+125	25	5962-8603204XA
TS68020DESC02XC	DESC	PGA 114	-55/+125	16.67	5962-8603202XC
TS68020DESC03XC	DESC	PGA 114	-55/+125	20	5962-8603203XC
TS68020DESC04XC	DESC	PGA 114	-55/+125	25	5962-8603204XC
TS68020DESC02YA	DESC	CQFP 132/tin	-55/+125	16.67	5962-8603202YA
TS68020DESC03YA	DESC	CQFP 132/tin	-55/+125	20	5962-8603203YA
TS68020DESC04YA	DESC	CQFP 132/tin	-55/+125	25	5962-8603204YA
TS68020DESC02YC	DESC	CQFP 132	-55/+125	16.67	5962-8603202YC
TS68020DESC03YC	DESC	CQFP 132	-55/+125	20	5962-8603203YC
TS68020DESC04YC	DESC	CQFP 132	-55/+125	25	5962-8603204YC

Standard Product

Commercial Atmel Part-Number	Norms	Package	Temperature Range T_c (°C)	Frequency (MHz)	Drawing Number
TS68020VR16	Internal Standard	PGA 114	-40/+85	16.67	Internal
TS68020VR20	Internal Standard	PGA 114	-40/+85	20	Internal
TS68020VR25	Internal Standard	PGA 114	-40/+85	25	Internal
TS68020MR16	Internal Standard	PGA 114	-55/+125	16.67	Internal
TS68020MR20	Internal Standard	PGA 114	-55/+125	20	Internal
TS68020MR25	Internal Standard	PGA 114	-55/+125	25	Internal

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