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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	68000
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	16.67MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 85°C (TC)
Security Features	-
Package / Case	114-BCPGA
Supplier Device Package	114-CPGA (34.54x34.54)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts68020vr16

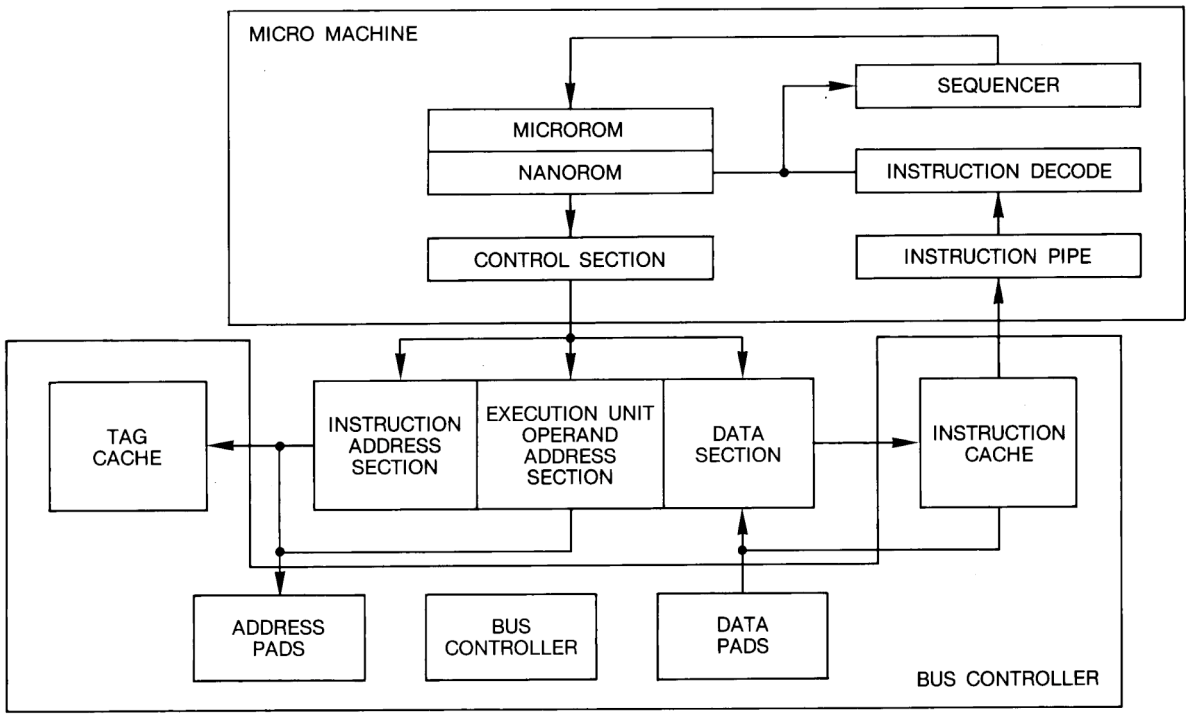
Introduction

The TS68020 is a high-performance 32-bit microprocessor. It is the first microprocessor to have evolved from a 16-bit machine to a full 32-bit machine that provides 32-bit address and data buses as well as 32-bit internal structures. Many techniques were utilized to improve performance and at the same time maintain compatibility with other processors of the TS68000 Family. Among the improvements are new addressing modes which better support high-level language structures, an expanded instruction set which provides 32-bit operations for the limited cases not supported by the TS68000 and several new instructions which support new data types. For special-purpose applications when a general-purpose processor alone is not adequate, a co-processor interface is provided.

The TS68020 is a high-performance microprocessor implemented in HCMOS, low power, small geometry process. This process allows CMOS and HMOS (high density NMOS) gates to be combined on the same device. CMOS structures are used where speed and low power is required, and HMOS structures are used where minimum silicon area is desired. This technology enables the TS68020 to be very fast while consuming less power (less than 1.5 watts) and still have a reasonably small die size. It utilizes about 190.000 transistors, 103.000 of which are actually implemented. The package is a pin-grid array (PGA) with 114 pins, arranged 13 pins on a side with a depopulated center and 132 pins ceramic quad flat pack.

Figure 1 is a block diagram of the TS68020. The processor can be divided into two main sections: the bus controller and the micromachine. This division reflects the autonomy with which the sections operate.

Figure 1. TS68020 Block Diagram



The bus controller consists of the address and data pads and multiplexers required to support dynamic bus sizing, a macro bus controller which schedules the bus cycles on the basis of priority with two state machines (one to control the bus cycles for operated accesses and the other to control the bus cycles for instruction accesses), and the instruction cache with its associated control.

Detailed Specifications

Scope

This drawing describes the specific requirements for the microprocessor 68020, 16.67 MHz, 20 MHz and 25 MHz, in compliance with the MIL-STD-883 class B.

Applicable Documents

MIL-STD-883

- MIL-STD-883: Test Methods and Procedures for Electronics
- MIL-PRF-38535 appendix A: General Specifications for Microcircuits
- Desc Drawing 5962 - 860320xxx

Requirements

General

The microcircuits are in accordance with the applicable document and as specified herein.

Design and Construction

Terminal Connections

Depending on the package, the terminal connections shall be as shown in Figure 2 and Figure 3.

Lead Material and Finish

Lead material and finish shall be any option of MIL-STD-1835.

Package

The macrocircuits are packages in hermetically sealed ceramic packages which are conform to case outlines of MIL-STD-1835 (when defined):

- 114-pin SQ.PGA UP PAE Outline
- 132-pin Ceramic Quad Flat Pack CQFP

The precise case outlines are described on Figure 23 and Figure 24.

Electrical Characteristics

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{CC}	Supply Voltage		-0.3	+7.0	V
V_I	Input Voltage		-0.5	+7.0	V
P_{dmax}	Max Power Dissipation	T_{case} = -55°C		2.0	W
		T_{case} = +125°C		1.9	W
T_{case}	Operating Temperature	M Suffix	-55	+125	°C
		V Suffix	-40	+85	°C
T_{stg}	Storage Temperature		-55	+150	°C
T_{leads}	Lead Temperature	Max 5 Sec. Soldering		+270	°C

Table 3. Recommended Condition of Use

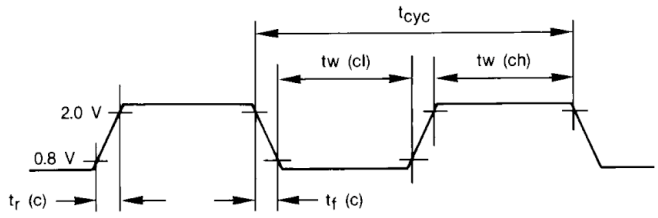
Unless otherwise stated, all voltages are referenced to the reference terminal (see Table 1).

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		4.5	5.5	V
V_{IL}	Low Level Input Voltage		-0.3	0.5	V
V_{IH}	High Level Input Voltage		2.4	5.25	V
T_{case}	Operating Temperature		-55	+125	°C
R_L	Value of Output Load Resistance		(1)		Ω
C_L	Output Loading Capacitance			(1)	pF
$t_r(c)$–$t_f(c)$	Clock Rise Time (See Figure 5)	68020-16		5	ns
		68020-20		5	
		68020-25		4	
f_c	Clock Frequency (See Figure 5)	68020-16	8	16.67	MHz
		68020-20	12.5	20	
		68020-25	12.5	25	
t_{cyc}	Cycle Time (see Figure 5)	68020-16	60	125	ns
		68020-20	50	80	
		68020-25	40	80	
$t_W(CL)$	Clock Pulse Width Low (See Figure 5)	68020-16	24	95	ns
		68020-20	20	54	
		68020-25	19	61	
$t_W(CH)$	Clock Pulse Width High (See Figure 5)	68020-16	24	95	ns
		68020-20	20	50	
		68020-25	19	61	

Note: 1. Load network number 1 to 4 as specified (Table 7) gives the maximum loading of the relevant output.

This device contains protective circuitry against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

Figure 5. Clock Input Timing Diagram



Note: Timing measurements are referenced to and from a low voltage of 0.8V and a high voltage of 2.0V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8V and 2.0V.

Table 4. Thermal Characteristics at 25°C

Package	Symbol	Parameter	Value	Unit
PGA 114	θ_{JA}	Thermal Resistance - Ceramic Junction to Ambient	26	°C/W
	θ_{JC}	Thermal Resistance - Ceramic Junction to Case	5	°C/W
CQFP 132	θ_{JA}	Thermal Resistance - Ceramic Junction to Ambient	34	°C/W
	θ_{JC}	Thermal Resistance - Ceramic Junction to Case	2	°C/W

Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \cdot V_{CC}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K + (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273) + \theta_{JA} \cdot P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part K can be determined from equation **(3)** by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations **(1)** and **(2)** iterativley for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation:

$$\theta_{JA} = \theta_{JC} = \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation **(1)** will result in a lower semiconductor junction temperature.

Mechanical and Environment

The microcircuits shall meet all mechanical environmental requirements of MIL-STD-883 for class B devices.

Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum:

- ATMEL Logo
- Manufacturer's Part Number
- Class B Identification
- Date-code of Inspection Lot
- ESD Identifier if Available
- Country of Manufacturing

Quality Conformance Inspection

DESC/MIL-STD-883

Is in accordance with MIL-M-38510 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspections are performed on a periodical basis.

Electrical Characteristics

General Requirements

All static and dynamic electrical characteristics specified and the relevant measurement conditions are given below.

(last issue on request to our marketing services).

Table 5: Static electrical characteristics for all electrical variants.

Table 6: Dynamic electrical characteristics for 68020-16 (16.67 MHz), 68020-20 (20 MHz) and 68020-25 (25 MHz).

For static characteristics, test methods refer to "Test Conditions Specific to the Device" on page 14 hereafter of this specification (Table 7).

For dynamic characteristics (Table 6), test methods refer to IEC 748-2 method, where existing.

Indication of “min.” or “max.” in the column “test temperature” means minimum or maximum operating temperature.

Table 5. Static Characteristics. V_{CC} = 5.0V_{DC} ± 10%; GND = 0V_{DC}; T_c = -55/+125°C or -40/+85°C (Figure 4 to Figure 8)

Symbol	Parameter	Condition	Min	Max	Units
I_{CC}	Maximum Supply Current	V_{CC} = 5.5V T_{case} -55°C to +25°C		333	mA
I_{CC}	Maximum Supply Current	V_{CC} = 5.5V T_{case} = 125°C		207	mA
V_{IH}	High Level Input Voltage	V_O = 0.5V or 2.5 V_{CC} = 4.5V to 5.5V	2.0	V_{CC}	V
V_{IL}	Low Level Input Voltage	V_O = 0.5V or 2.4V V_{CC} = 4.5V to 5.5V	-0.5	0.8	V
V_{OH}	High Level Output Voltage All Outputs	I_{OH} = 400 µA	2.4		V
V_{OL}	Low Level Output Voltage Outputs A0-A31, FC0-FC2, D0-D31, SIZ0-SIZ1, $\overline{BG}$	I_{OL} = 3.2 mA Load Circuit as Figure 8 R = 1.22 kΩ		0.5	V
V_{OL}	Low Level Output Voltage Outputs $\overline{AS}$, $\overline{DS}$, $\overline{RMC}$, R/$\overline{W}$, $\overline{DBEN}$, $\overline{IPEND}$	I_{OL} = 5.3 mA Load Circuit as Figure 8 R = 740Ω		0.5	V
V_{OL}	Low Level Output Voltage Outputs $\overline{ECS}$, $\overline{OCS}$	I_{OL} = 2.0 mA Load Circuit as Figure 8 R = 2 kΩ		0.5	V
V_{OL}	Low Level Output Voltage Outputs $\overline{HALT}$, $\overline{RESET}$	I_{OL} = 10.7 mA Load Circuit as Figure 6 and Figure 7		0.5	V
$\lvert I_{IN} \rvert$	Input Leakage Current (High and Low State)	-0.5V ≤ V_{IN} ≤ V_{CC} (Max)		2.5	µA
$\lvert I_{OHZ} \rvert$	High level leakage current at three-state outputs Outputs A0-A31, $\overline{AS}$, $\overline{DBEN}$, $\overline{DS}$, D0-D31, R/$\overline{W}$, FC0-FC2, $\overline{RMC}$, SIZ0-SIZ1	V_{OH} = 2.4V		2.5	µA
$\lvert I_{OLZ} \rvert$	Low Level Leakage Current at Three-state Outputs Outputs A0-A31, $\overline{AS}$, $\overline{DBEN}$, $\overline{DS}$, D0-D31 R/$\overline{W}$, FC0-FC2, $\overline{RMC}$, SIZ0-SIZ1	V_{OL} = 0.5V		2.5	µA
I_{OS}	Output Short-circuit Current (Any Output)	V_{CC} = 5.5V V_O = 0V (Pulsed. Duration 1 ms Duty Cycle 10:1)		200	mA

Dynamic (Switching) Characteristics

The limits and values given in this section apply over the full case temperature range -55°C to +125°C and V_{CC} in the range 4.5V to 5.5V V_{IL} = 0.5V and V_{IH} = 2.4V (See also note 12 and 13). The INTERVAL numbers refer to the timing diagrams. See Figure 5, Figure 9 and Figure 12.

Table 6. Dynamic Electrical Characteristics

Symbol	Parameter	Interval Number	68020-16		68020-20		68020-25		Unit	Notes
			Min	Max	Min	Max	Min	Max		
t_{CPW}	Clock Pulse Width	2 , 3	24	95	20	54	19	61	ns	
t_{CHAV}	Clock High to Address/FC/Size/$\overline{RMC}$ Valid	6	0	30	0	25	0	25	ns	
t_{CHEV}	Clock High to $\overline{ECS}$, $\overline{OCS}$ Asserted	6A	0	20	0	15	0	12	ns	
t_{CHAZX}	Clock High to Address/Data/FC/$\overline{RMC}$/ Size High Impedance	7	0	60	0	50	0	40	ns	(11)
t_{CHAZn}	Clock High to Address/FC/Size/$\overline{RMC}$ Invalid	8	0		0		0		ns	
t_{CLSA}	Clock Low to $\overline{AS}$, $\overline{DS}$ Asserted	9	3	30	3	25	3	18	ns	
t_{STSA}	$\overline{AS}$ to $\overline{DS}$ Assertion (Read)(Skew)	9A	-15	15	-10	10	-10	10	ns	(1)
t_{ECSA}	$\overline{ECS}$ Width Asserted	10	20		15		15		ns	
t_{OCSA}	$\overline{OCS}$ Width Asserted	10A	20		15		15		ns	
t_{EOCSN}	$\overline{ECS}$, $\overline{OCS}$ Width Negated	10B	15		10		5		ns	(11)
t_{AVSA}	Address/FC/Size/$\overline{RMC}$ Valid to $\overline{AS}$ Asserted (and $\overline{DS}$ Asserted, Read)	11	15		10		6		ns	(6)
t_{CLSN}	Clock Low to $\overline{AS}$, $\overline{DS}$ Negated	12	0	30	0	25	0	15	ns	
t_{CLEN}	Clock Low to $\overline{ECS}$/$\overline{OCS}$ Negated	12A	0	30	0	25	0	15	ns	
t_{SNAI}	$\overline{AS}$, $\overline{DS}$ Negated to Address/FC/ Size/$\overline{RMC}$ Invalid	13	15		10		10		ns	
t_{SWA}	$\overline{AS}$ (and $\overline{DS}$, Read) Width Asserted	14	100		85		70		ns	
t_{SWAW}	$\overline{DS}$ Width Asserted, Write	14A	40		38		30		ns	
t_{SN}	$\overline{AS}$, $\overline{DS}$ Width Negated	15	40		38		30		ns	(11)
t_{SNSA}	$\overline{DS}$ Negated to $\overline{AS}$ Asserted	15A	35		30		25		ns	(8)
t_{CSZ}	Clock High to $\overline{AS}$/$\overline{DS}$/R/$\overline{W}$/$\overline{DBEN}$ High Impedance	16		60		50		40	ns	(11)
t_{SNRN}	$\overline{AS}$, $\overline{DS}$ Negated to R/$\overline{W}$ High	17	15		10		10		ns	(6)
t_{CHRH}	Clock High to R/$\overline{W}$ High	18	0	30	0	25	0	20	ns	
t_{CHRL}	Clock High to R/$\overline{W}$ Low	20	0	30	0	25	0	20	ns	
t_{RAAA}	R/$\overline{W}$ High to $\overline{AS}$ Asserted	21	15		10		5		ns	(6)
t_{RASA}	R/$\overline{W}$ Low to $\overline{DS}$ Asserted (Write)	22	75		60		50		ns	(6)
t_{CHDO}	Clock High to Data Out Valid	23		30		25		25	ns	
t_{SNDI}	AS, DS Negated to Data Out Valid	25	15		10		5		ns	(6)
t_{DNDBN}	$\overline{DS}$ Negated to $\overline{DBEN}$ Negated (Write)	25A	15		10		5		ns	(9)

Test Conditions Specific to the Device

Loading Network

The applicable loading network shall be defined in column “Test conditions” of Table 6, referring to the loading network number as shown in Figure 6, Figure 7, Figure 8 below.

Figure 6. RESET Test Loads

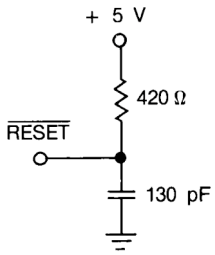


Figure 7. HALT Test Load

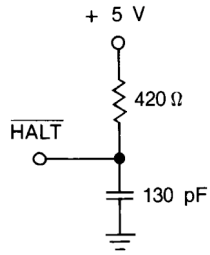


Figure 8. Test Load

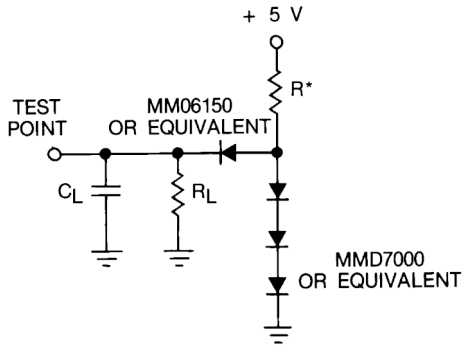
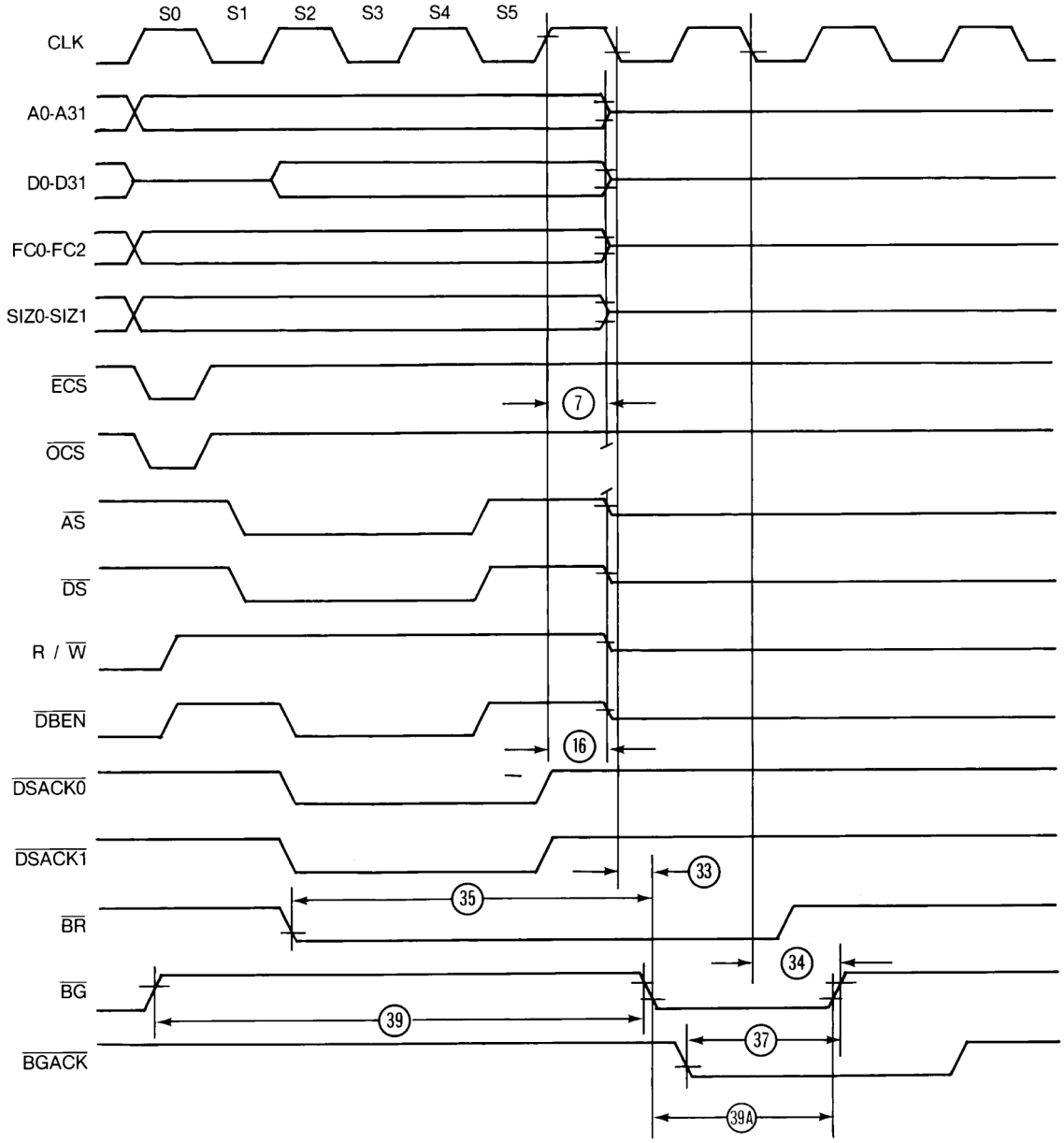


Table 7. Load Network

Load NBR	Figure	R	R_L	C_L	Output Application
1	7	2 k	6.0 k	50 pF	$\overline{OCS}$, $\overline{ECS}$
2	7	1.22 k	6.0 k	130 pF	A0-A31, D0-D31, $\overline{BG}$, FC0-FC2, SIZ0-SIZ1
3	7	0.74 k	6.0 k	130 pF	$\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, $\overline{RMC}$, $\overline{DBEN}$, $\overline{IPEND}$

Note: 1. Equivalent loading may be simulated by the tester.

Figure 11. Bus Arbitration Timing Diagram



Note: Timing measurements are referenced to and from a low voltage of 0.8V and a high voltage of 2.0V, unless otherwise noted. The voltage swing thorough this range should start outside and pass through the range such that the rise or fall will be linear between 0.8V and 2.0V.

Input and Output Signals for Dynamic Measurements

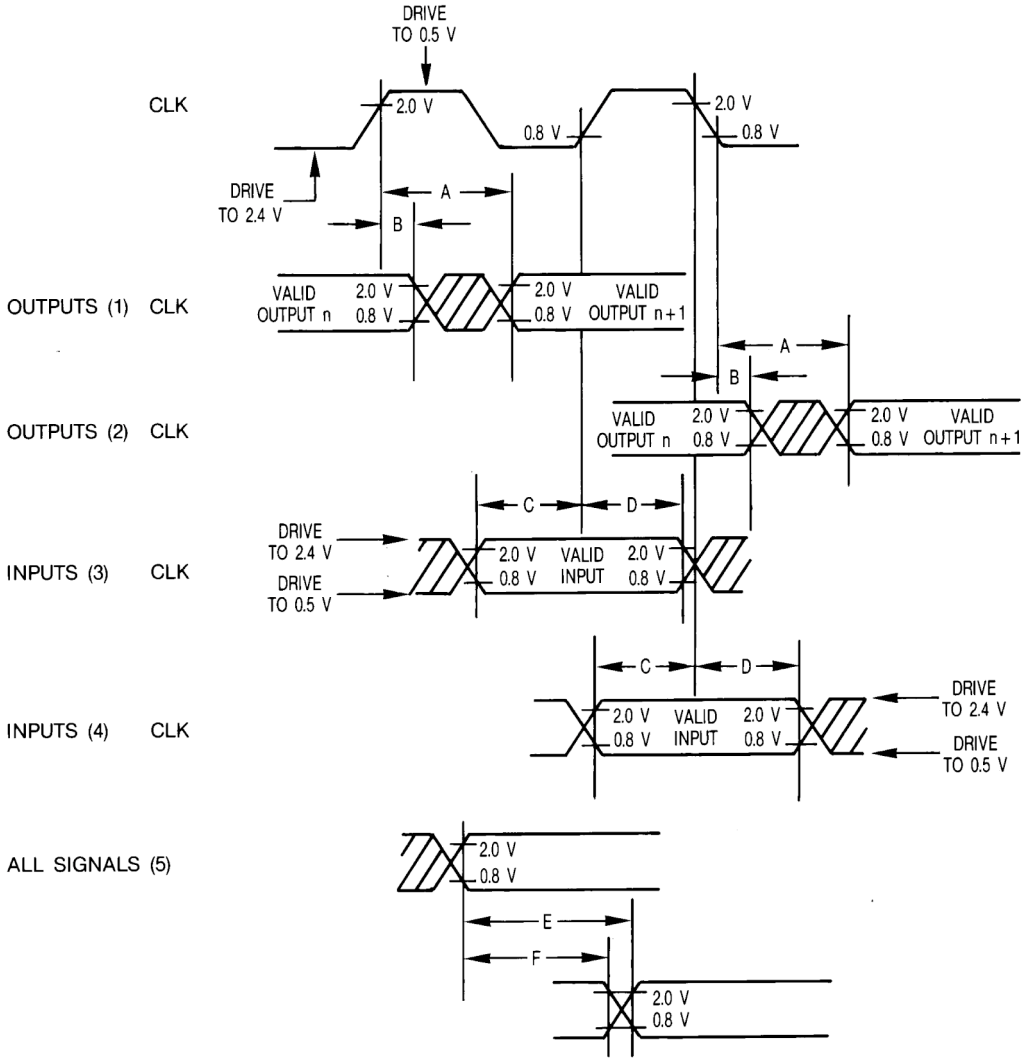
AC Electrical Specifications Definitions

The AC specifications presented consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of the TS68020 clock input and, possibly, relative to one or more other signals.

The measurement of the AC specifications is defined by the waveforms in Figure 12. In order to test the parameters guaranteed by Atmel, inputs must be driven to the voltage levels specified in Figure 12. Outputs of the TS68020 are specified with minimum and/or maximum limits, as appropriate, and are measured as shown. Inputs to the TS68020 are specified with minimum and, as appropriate, maximum setup and hold times, and are measurement as shown. Finally, the measurements for signal-to-signal specification are also shown.

Note that the testing levels used to verify conformance of the TS68020 to the AC specifications does not affect the guaranteed DC operation of the device as specified in the DC electrical characteristics.

Figure 12. Drive Levels and Test Points for AC Specification



Legend:

A) Maximum Output Delay Specification

B) Minimum Output Hold Time

C) Minimum Input Setup Time Specification

D) Minimum Input Hold Time Specification

E) Signal Valid to Signal Valid Specification (Maximum or Minimum)

F) Signal Valid to Signal Invalid Specification (Maximum or Minimum)

Notes:
1. This output timing is applicable to all parameters specified relative to the rising edge of the clock.
2. This out put timing is applicable to all parameters specified relative to the falling edge of the clock.
3. This input timing is applicable to all parameters specified relative to the falling edge of the clock.
4. This input timing is applicable to all parameters specified relative to the falling edge of the clock.
5. This timing is applicable to all parameters specified relative to the assertion/negation of another signal.

Additional Information

Additional information shall not be for any inspection purposes.

Power Consideration

See Table 4.

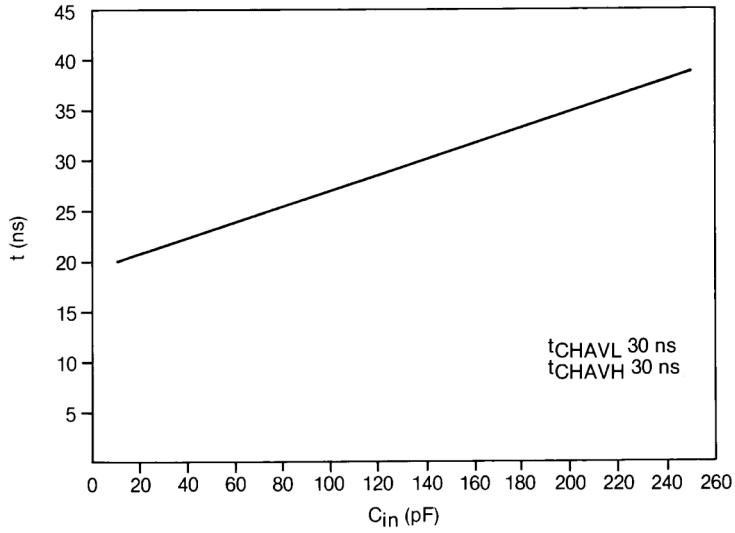
Capacitance (Not for Inspection Purposes

Symbol	Parameter	Test Conditions	Min	Unit
C_{in}	Input Capacitance	V_{in} = 0V T_{amb} = 25°C f = 1 MHz	20	pF

Capacitance Derating Curves

Figure 13 to Figure 18 inclusive show the typical derating conditions which apply. The capacitance includes any stray capacitance. The graphs may not be linear outside the range shown.

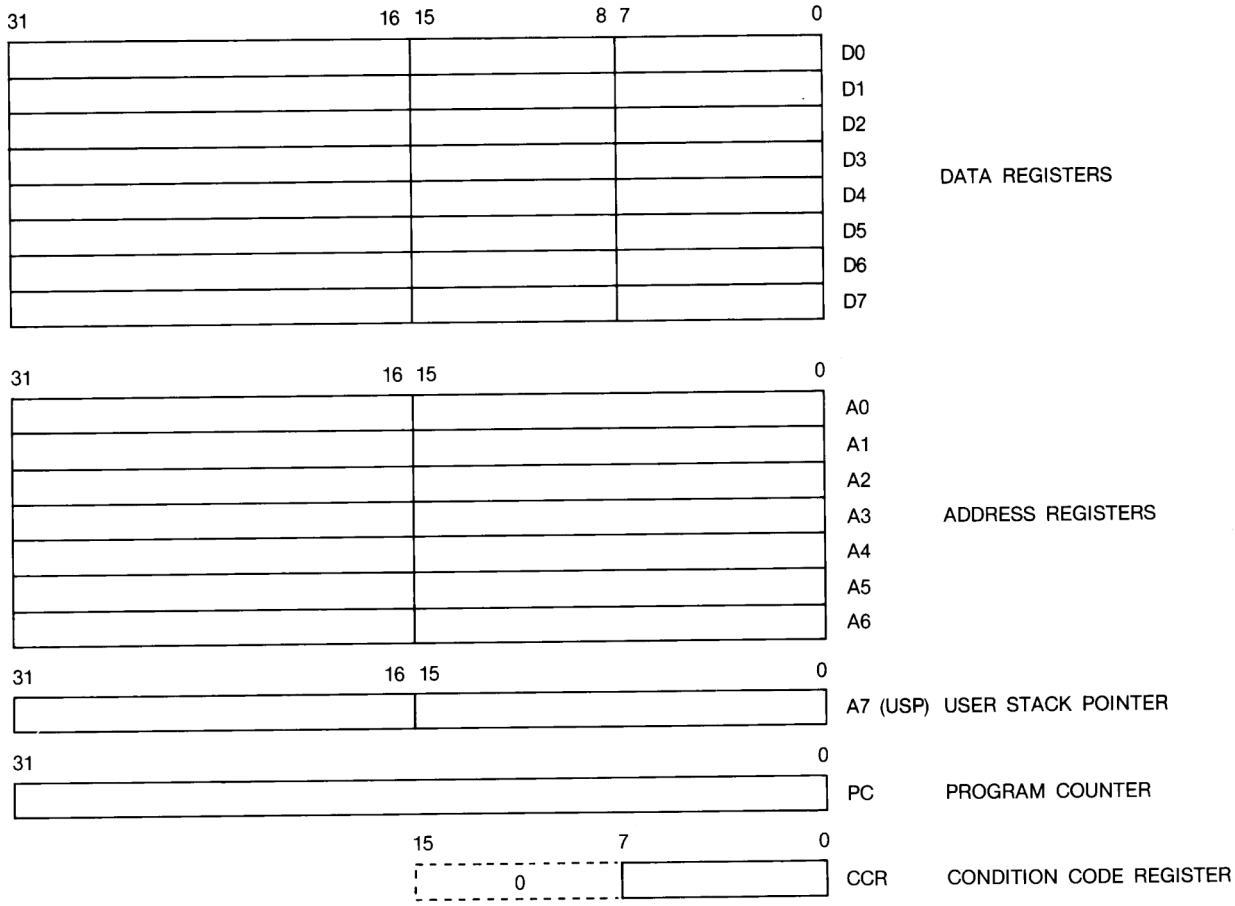
Figure 13. Address Capacitance Derating Curve



The TS68000 Family processors distinguish address spaces as supervisor / used and program/data. These four combinations are specified by the function code pins (FC0/FC1/FC2) during bus cycles, indication the particular address space. Using the function codes, the memory sub-system can distinguish between authorized access (supervisor mode is privileged access) and unauthorized access (user mode may not have access to supervisor program or data areas). To support the full privileges of the supervisor, the alternate function code registers allow the supervisor to specify an access to user program or data areas by preloading the SFC/DFC registers appropriately.

The cache registers (control — CACR, address — CAAR) allow software manipulation of the on-chip instruction cache. Control and status accesses to the instruction cache are provided by the cache control register (CACR), while the cache address register (CAAR) holds the address for those cache control functions that require an address.

Figure 19. User Programming Model



Bit Field Operation

The TS68020 supports variable length bit field operations up to 32-bit. A bit field may start in any bit position and span any address boundary for the full length of the bit field, up to the 32-bit maximum. The bit field insert (BFINS) inserts a value into a field. Bit field extract unsigned (BFEXTU) and bit field extract signed (BFEXTS) extract an unsigned or signed value from the field. BFFFO finds the first bit in a bit field that is set. To complement the TS68000 bit manipulation instruction, there are bit field change, clear, set and test instructions (BFCHG, BFCLR, BFSET, BFTST). Using the on-chip barrel shifter, the bit and bit field instructions are very fast and particularly useful in applications using packed bits and bit fields, such as graphics and communications.

Binary Coded Decimal (BCD) Support

The TS68000 Family supports BCD operations including add, subtract, and negation. The TS68020 adds the PACK and UNPACK operations for BCD conversions to and from binary form as well as other conversions, e.g., ASCII and EBCDIC. The PACK instruction reduces two bytes of data into a single byte while UNPACK reverses the operation.

Bounds Checking

Previous 68000 Family members offer variable bounds checking only on the upper limit of the bound. The underlying assumption is that the lower bound is zero. This is expanded on the TS68020 by providing two new instructions, CHK2 and CMP2. These instructions allow checking and comparing of both the upper and lower bounds. These instructions may be either signed or unsigned. The CMP2 instructions sets the condition codes upon completion while the CHK2 instruction, in addition to setting the condition codes, will take a system trap if either boundary condition is exceeded.

System Traps

Three additions have been made to the system trap capabilities of the TS68020. The current TRAPV (trap on overflow) instruction has been expanded to a TRAPcc format where any condition code is allowed to be the trapping condition. And, the TRAPcc instruction is expanded to optionally provide one or two additional words following the trap instruction so user-specified information may be presented to the trap handler. These additional words can be used when needed to provide simple error codes or debug information for interactive runtime debugging or post-mortem program dumps. Compilers may provide direction to run-time execution routines towards handling of specific conditions.

The breakpoint instruction, BKPT, is used to support the program breakpoint function for debug monitors and real-time in-circuit or hardware emulators, and the operation will be dependent on the actual system implementation. Execution of this instruction causes the TS68020 to run a breakpoint acknowledge bus cycle, with a 3-bit breakpoint identifier placed on address lines A2, A3, and A4. This 3-bit identifier permits up to eight breakpoints to be easily differentiated. The normal response to the TS68020 is an operation word (typically an instruction, originally replaced by the debugger with the breakpoint instruction) placed on the data lines by external debugger hardware and the breakpoint acknowledge cycle properly terminated. The TS68020 then executes this operation word in place of the breakpoint instruction. The debugger hardware can count the number of executions of each breakpoint and halt execution after a pre-determined number of cycles.

Multi-processing

To further support multi-processing with the TS68020, a compare and swap instruction, CAS, has been added. This instruction makes use of the read-modify-write cycle to compare two operands and swap a third operand pending the results of the compare. A variant of this instruction, CAS2, performs similarly comparing dual operand pairs, and updating two operands.

These multi-processing operations are useful when using common memory to share or pass data between multiple processing elements. The read-modify-write cycle is an indivisible operand that allows reading and updating a “lock” operand used to control access to the common memory elements. The CAS2 instruction is more powerful since dual operands allow the “lock” to the checked and two values (i.e., both pointers in a doubly-linked list) to be updated according to the lock’s status, all in a single operation.

Module Support

The TS68020 includes support for modules with the call module (CALLM) and return from module (RTM) instructions. The CALLM instruction references a module descriptor. This descriptor contains control information for entry into the associated module. The CALLM instruction creates a module stack frame and stores the module state in that frame. The RTM instruction recovers the previous module state from the stack frame and returns to the calling module.

The module interface also provides a mechanism for finer resolution of access control by external hardware. Although the TS68020 does not interrupt the access control information, it does communicate with external hardware when the access control is to be changed, and relies on the external hardware to verify that the changes are legal.

CALLM and RTM, when used as subroutine calls and returns with proper descriptor formats, cause the TS68020 to perform the necessary actions to verify legitimate access to modules.

Virtual Memory/Machine Concepts

The full addressing range of the TS68020 is 4-Gbyte (4, 294, 967, 296). However, most TS68020 systems implement a smaller physical memory. Nonetheless, by using virtual memory techniques, the system can be made to appear to have a full 4-Gbyte of physical memory available to each user program. These techniques have been used for many years in large mainframe computers and minicomputers. With the TS68020 (as with the TS68010 and TS68012), virtual memory can be fully supported in microprocessor-based systems.

In a virtual memory system, a user program can be written as though it has a large amount of memory available to it when actually only a smaller amount of memory is physically present in the system. In a similar fashion, a system provides user programs access to other devices that are not physically present in the system, such as tape drives, disk drives, printers, or terminals. With proper software emulation, a physical system can be made to appear to a user program as any other 68000 computer system and the program may be given full access to all of the resources of that emulated system. Such an emulator system is called a virtual machine.

Virtual Memory

The basic mechanism for supporting virtual memory is to provides a limited amount of high-speed physical memory that can be accessed directly by the processor while maintaining of a much larger “virtual” memory on secondary storage devices such as large capacity disk drives. When the processor attempts to access a location in the virtual memory map that is not resident in the physical memory (referred to as a page fault), the access to that location is temporarily suspended while the necessary data is fetched from secondary storage and placed in physical memory; the suspended access is then either restarted or continued.

The TS68020 will always transfer the maximum amount of data on all bus cycles; i.e., it always assumes the port is 32-bit wide when beginning the bus cycle. In addition, the TS68020 has no restrictions concerning alignment of operands in memory; long word operands need not be aligned on long word address boundaries. When misaligned data requires multiple bus cycles, the TS68020 aligned data requires multiple bus cycles, the TS68020 automatically runs the minimum number of bus cycles.

The Co-processor Concept

The co-processor interface is a mechanism for extending the instruction set of the TS68000 Family. Examples of these extensions are the addition of specialized data operands for the existing data types or, for the case of the floating point, the inclusion of new data types and operations for them as implemented by the TS68881 and TS68882 floating point co-processors.

The programmer's model for the TS68000 Family of microprocessors is based on sequential, non-concurrent instruction execution. This means each instruction is completely executed prior to the beginning of the next instruction. Hence, instructions do not operate concurrently in the programmer's model. Most microprocessors implement the sequential model which greatly simplifies the programmer responsibilities since sequencing control is automatic and discrete.

The TS68000 co-processor interface is designed to extend the programmer's model and it provides full support for the sequential, non-concurrent instruction execution model. Hence, instruction execution by the co-processor is assumed to not overlap with instruction execution with the main microprocessor. Yet, the TS68000 co-processor interface does allow concurrent operation when concurrency can be properly accommodated. For example, the TS68881 or TS68882 floating-point co-processor will allow the TS68020 to proceed executing instruction while the co-processor continues a floating-point operation, up to the point that the TS68020 sends another request to the co-processor. Adhering to the sequential execution model, the request to the co-processor continues a floating-point operation, up to the co-processor completes each TS68881 and TS68882 instruction before it starts the next, and the TS68020 is allowed to proceed as it can in a concurrent fashion.

co-processors are divided into two types by their bus utilization characteristics. A co-processor is a DMA co-processor if it can control the bus independent of the main processor. A co-processor is a non-DMA co-processor if it does not have the capability of controlling the bus. Both co-processor types utilize the same protocol and main processor resources. Implementation of a co-processor as a DMA or non-DMA type is based primarily on bus bandwidth of the co-processor, performance, and cost issues.

The communication protocol between the main processor and the co-processor necessary to execute a co-processor instruction is based on a group of co-processor interface registers (Table 10) which are defined for the TS68000 Family co-processor interface. The TS68020 hardware uses standard TS68000 asynchronous bus cycles to access the registers. Thus, the co-processor doesn't require a special bus hardware; the bus interface implemented by a co-processor for its interface register set must only satisfy the TS68020 address, data, and control signal timing to guarantee proper communication with the main processor. The TS68020 implements the communication protocol with all co-processors in hardware (and microcode) and handles all operations automatically so the programmer is only concerned with the instructions and data types provided by the co-processor as extensions to the TS68020 instruction set and data types.

Other microprocessors in the TS68000 Family can operate any TS68000 co-processor even though they may not have the hardware implementation of the co-processor interface as does the TS68020. Since the co-processor is operated through the co-processor interface registers which are accessed via normal asynchronous bus cycles, the co-processor may be used as a peripheral device. Software easily emulates the communication protocol by addressing the co-processor interface registers appropriately and passing the necessary commands and operands required by the co-processor.

The co-processor interface registers are implemented by the co-processor in addition to those registers implemented as extensions to the TS68020 programmer's model. For example, the TS68881 implements the co-processor interface registers shown in Table 10 and the registers in the programming model, including eight 80-bit floating-point data registers and three 32-bit control/status registers used by the TS68881 programmer.

Table 10. Co-processor Interface Registers

Register	Function	R/W
Response	Requests Action from CPU	R
Control	CPU	W
Save	Initiate Save of Internal State	R
Restore	Initiate Restore of Internal State	R/W
Operation Word	Current Co-processor Instruction	W
Command Word	Co-processor Specific Command	W
Condition Word	Condition to be Evaluated	W
Operand	32-bit Operand	R/W
Register Select	Specifies CPU Register or Mask	R
Instruction Address	Pointer to Co-processor Instruction	R/W
Operand Address	Pointer to Co-processor Operand	R/W

Table 11. Co-processor Primitives

Processor Synchronization Busy with Current Instruction Proceed with Next Instruction, If No Trace Service Interrupts and Re-query, If Trace Enable Proceed with Execution, Condition True/False
Instruction Manipulation Transfer Operation Word Transfer Words from Instruction Stream
Exception Handling Take Privilege Violation if S Bit Not Set Take Pre-Instruction Exception Take Mid-Instruction Exception Take Post-Instruction Exception

Table 11. Co-processor Primitives (Continued)

General Operand Transfer
Evaluate and Pass (Ea.)
Evaluate (Ea.) and Transfer Data
Write to Previously Evaluated (Ea.)
Take Address and Transfer Data
Transfer to/from Top of Stack
Register Transfer
Transfer CPU Register
Transfer CPU Control Register
Transfer Multiple CPU Registers
Transfer Multiple Co-processor Registers
Transfer CPU SR and/or ScanPC

Up to eight processors are supported in a single system with a system-unique co-processor identifier encoded in the co-processor instruction. When accessing a co-processor, the TS68020 executes standard read and write bus cycle in CPU address space, as encoded by the function codes, and places the co-processor identifier on the address bus to be used by chip-select logic to select the particular co-processor. Since standard bus cycle are used to access the co-processor, the co-processor may be located according to system design requirements, whether it be located on the micro-processor local bus, on another board on the system bus, or any other place where the chip-select and co-processor protocol using standard TS68000 bus cycles can be supported.

Co-processor Protocol

Interprocessor transfers are all initiated by the main processor during co-processor instruction execution. During the processing of a co-processor instruction, the main processor transfers instruction information and data to the associated co-processor, and receives data, requests, and status information from the co-processor. These transfers are all based on the TS68000 bus cycles.

The typical co-processor protocol which the main processor follows is:

a) The main processor initiates the communications by writing command information to a location in the co-processor interface.

b) The main processor reads the co-processor response to that information.

1) The response may indicate that the co-processor is busy, and the main processor should again query the co-processor. This allows the main processor and co-processor to synchronize their concurrent operations.

2) The response may indicate some exception condition; the main processor acknowledges the exception and begins exception processing.

3) The response may indicate that the co-processor needs the main processor to perform some service such as transferring data to or from the co-processor. The co-processor may also request that the main processor query the co-processor again after the service is complete.

4) The response may indicate that the main processor is not needed for further processing of the instruction. The communication is terminated, and the main processor is free to begin execution of the next instruction. At this point in the co-processor protocol, as the main processor continues to execute the instruction stream, the main processor may operate concurrently with the co-processor.

Preparation for Delivery

Certificate of Compliance

Atmel offers a certificate of compliance with each shipment of parts, affirming the products are in compliance with MIL-STD-883 and guaranteeing the parameters are tested at extreme temperatures for the entire temperature range.

Handling

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

a) Device should be handled on benches with conductive and grounded surface.

b) Ground test equipment, tools and operator

c) Do not handle devices by the leads.

d) Store devices in conductive foam or carriers.

e) Avoid use of plastic, rubber, or silk in MOS areas.

f) Maintain relative humidity above 50%, if practical.

Package Mechanical Data

Figure 23. 114-lead - Ceramic Pin Grid Array

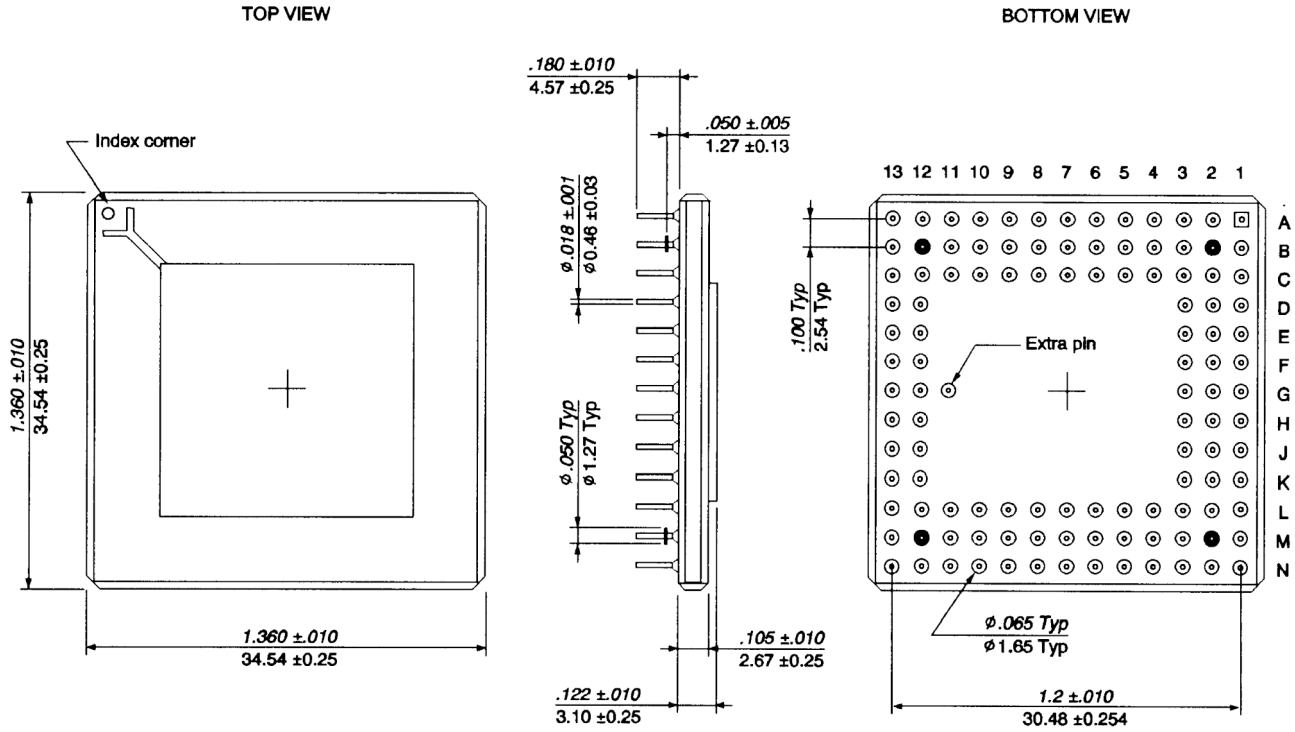


Figure 24. 132 Pins - Ceramic Quad Flat Pack