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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f51101adfl-30

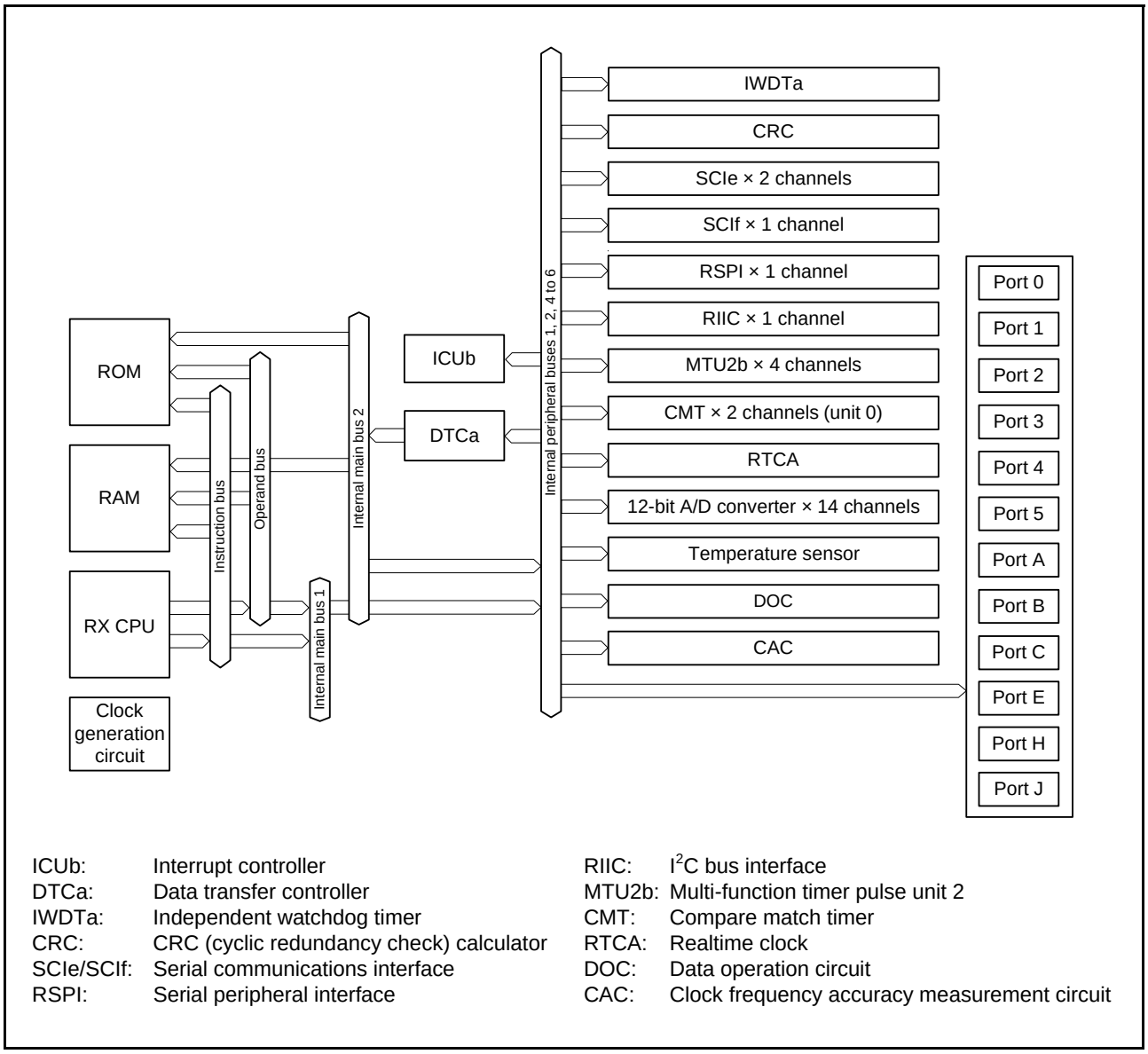
Table 1.3 List of Products (2/2)

Group	Part No.	Orderable Part No.	Package	ROM Capacity	RAM Capacity	Maximum Operating Frequency	Operating Temperature
RX110	R5F51105ADFM	R5F51105ADFM#30	PLQP0064KB-A	128 Kbytes	16 Kbytes	32MHz	–40 to +85°C
	R5F51105ADFK	R5F51105ADFK#30	PLQP0064GA-A				
	R5F51105ADLF	R5F51105ADLF#U0	PWLG0064KA-A				
	R5F51105ADFL	R5F51105ADFL#30	PLQP0048KB-A				
	R5F51105ADNE	R5F51105ADNE#U0	PWQN0048KB-A				
	R5F51104ADFM	R5F51104ADFM#30	PLQP0064KB-A	96 Kbytes			
	R5F51104ADFK	R5F51104ADFK#30	PLQP0064GA-A				
	R5F51104ADLF	R5F51104ADLF#U0	PWLG0064KA-A				
	R5F51104ADFL	R5F51104ADFL#30	PLQP0048KB-A				
	R5F51104ADNE	R5F51104ADNE#U0	PWQN0048KB-A				
	R5F51103ADFM	R5F51103ADFM#30	PLQP0064KB-A	64 Kbytes	10 Kbytes		
	R5F51103ADFK	R5F51103ADFK#30	PLQP0064GA-A				
	R5F51103ADLF	R5F51103ADLF#U0	PWLG0064KA-A				
	R5F51103ADFL	R5F51103ADFL#30	PLQP0048KB-A				
	R5F51103ADNE	R5F51103ADNE#U0	PWQN0048KB-A				
	R5F51103ADLM	R5F51103ADLM#U0	PWLG0036KA-A				
	R5F51103ADNF	R5F51103ADNF#U0	PWQN0040KC-A				
	R5F51101ADFM	R5F51101ADFM#30	PLQP0064KB-A	32 Kbytes			
	R5F51101ADFK	R5F51101ADFK#30	PLQP0064GA-A				
	R5F51101ADLF	R5F51101ADLF#U0	PWLG0064KA-A				
	R5F51101ADFL	R5F51101ADFL#30	PLQP0048KB-A				
	R5F51101ADNE	R5F51101ADNE#U0	PWQN0048KB-A				
	R5F51101ADLM	R5F51101ADLM#U0	PWLG0036KA-A				
	R5F51101ADNF	R5F51101ADNF#U0	PWQN0040KC-A				
	R5F5110JADFM	R5F5110JADFM#30	PLQP0064KB-A	16 Kbytes	8 Kbytes		
	R5F5110JADFK	R5F5110JADFK#30	PLQP0064GA-A				
	R5F5110JADLF	R5F5110JADLF#U0	PWLG0064KA-A				
	R5F5110JADFL	R5F5110JADFL#30	PLQP0048KB-A				
	R5F5110JADNE	R5F5110JADNE#U0	PWQN0048KB-A				
	R5F5110JADLM	R5F5110JADLM#U0	PWLG0036KA-A				
	R5F5110JADNF	R5F5110JADNF#U0	PWQN0040KC-A				
	R5F5110HADLM	R5F5110HADLM#U0	PWLG0036KA-A	8 Kbytes			
	R5F5110HADNF	R5F5110HADNF#U0	PWQN0040KC-A				

Note: Orderable part numbers are current as of when this manual was published. Please make sure to refer to the relevant product page on the Renesas website for the latest part numbers.

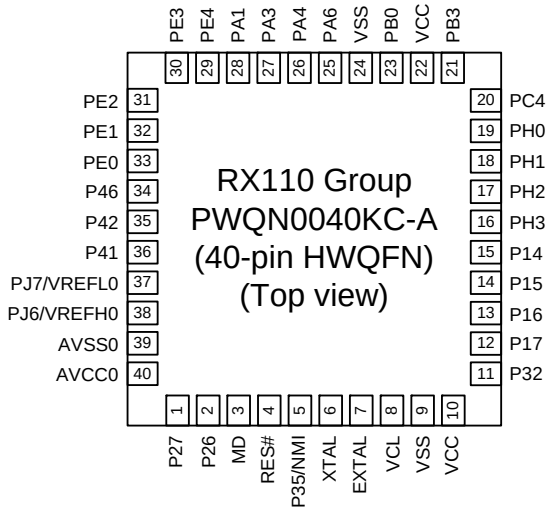
1.3 Block Diagram

Figure 1.2 shows a block diagram.



ICUb:	Interrupt controller	RIIC:	I^2C bus interface
DTCa:	Data transfer controller	MTU2b:	Multi-function timer pulse unit 2
IWDTa:	Independent watchdog timer	CMT:	Compare match timer
CRC:	CRC (cyclic redundancy check) calculator	RTCA:	Realtime clock
SCIe/SCIf:	Serial communications interface	DOC:	Data operation circuit
RSPI:	Serial peripheral interface	CAC:	Clock frequency accuracy measurement circuit

Figure 1.2 Block Diagram



Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, see the table “List of Pins and Pin Functions (40-Pin HWQFN)”.
Note: It is recommended that the exposed die pad of HWQFN should be connected to VSS.

Figure 1.6 Pin Assignments of the 40-Pin HWQFN

Table 1.5 List of Pins and Pin Functions (64-Pin LFQFP/LQFP) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, RTC)	Communication (SCIe, SCIf, RSPI, RIIC)	Others
1		P03			
2		P27	MTIOC2B	SCK1/SCK12	IRQ3/CMPA2/ CACREF/ADTRG0#
3		P26	MTIOC2A	TXD1/SMOSI1/SSDA1	
4		P30		RXD1/SMISO1/SSCL1	IRQ0
5		P31		CTS1#/RTS1#/SS1#	IRQ1
6	MD				FINED
7	RES#				
8	XCOUT				
9	XCIN	PH7			
10		P35			NMI
11	XTAL				
12	EXTAL				
13	VCL				
14	VSS				
15	VCC				
16		P32	MTIOC0C/RTCOUT		IRQ2
17		P17	MTIOC0C	SCK1/MISOA/SDA0/RXD12/RXDX12/ SMISO12/SSCL12	IRQ7
18		P16	RTCOUT	TXD1/SMOSI1/SSDA1/MOSIA/SCL0	IRQ6/ADTRG0#
19		P15	MTIOC0B/MTCLKB	RXD1/SMISO1/SSCL1/RSPCKA	IRQ5/CLKOUT
20		P14	MTIOC0A/MTCLKA	CTS1#/RTS1#/SS1#/SSLA0/TXD12/ TXDX12/SIOX12/SMOSI12/SSDA12	IRQ4
21		PH3	MTIOC1A		
22		PH2			IRQ1
23		PH1			IRQ0
24		PH0	MTIOC1B		CACREF
25		P55			
26		P54			
27		PC7	MTCLKB	TXD1/SMOSI1/SSDA1/MISOA	CACREF
28		PC6	MTCLKA	RXD1/SMISO1/SSCL1/MOSIA	
29		PC5	MTCLKD	SCK1/RSPCKA	
30		PC4	MTCLKC	SCK5/SSLA0	IRQ2/CLKOUT
31		PC3		TXD5/SMOSI5/SSDA5	
32		PC2		RXD5/SMISO5/SSCL5/SSLA3	
33		PB7/PC1			
34		PB6/PC0			
35		PB5	MTIOC2A/MTIOC1B		
36		PB3	MTIOC0A		
37		PB1	MTIOC0C		IRQ4
38	VCC				
39		PB0	MTIC5W/MTIOC0C/ RTCOUT	SCL0/RSPCKA	IRQ2/ADTRG0#
40	VSS				
41		PA6	MTIC5V/MTCLKB/MTIOC2A	CTS5#/RTS5#/SS5#/SDA0/MOSIA	IRQ3
42		PA4	MTIC5U/MTCLKA/MTIOC2B	TXD5/SMOSI5/SSDA5/SSLA0	IRQ5
43		PA3	MTIOC0D/MTCLKD/ MTIOC1B	RXD5/SMISO5/SSCL5/MISOA	IRQ6
44		PA1	MTIOC0B/MTCLKC/ RTCOUT	SCK5/SSLA2	

Table 1.7 List of Pins and Pin Functions (48-Pin LFQFP/HWQFN) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, RTC)	Communication (SCIe, SCIf, RSPI, RIIC)	Others
1		P27	MTIOC2B	SCK1/SCK12	IRQ3/CMPA2/ CACREF/ADTRG0#
2		P26	MTIOC2A	TXD1/SMOSI1/SSDA1	
3	MD				FINED
4	RES#				
5	XCOUT				
6	XCIN	PH7			
7		P35			NMI
8	XTAL				
9	EXTAL				
10	VCL				
11	VSS				
12	VCC				
13		P17	MTIOC0C	SCK1/MISOA/SDA0/RXD12/RXDX12/ SMISO12/SSCL12	IRQ7
14		P16	RTCOUT	TXD1/SMOSI1/SSDA1/MOSIA/SCL0	IRQ6/ADTRG0#
15		P15	MTIOC0B/MTCLKB	RXD1/SMISO1/SSCL1/RSPCKA	IRQ5/CLKOUT
16		P14	MTIOC0A/MTCLKA	CTS1#/RTS1#/SS1#/SSLA0/TXD12/ TXDX12/SIOX12/SMOSI12/SSDA12	IRQ4
17		PH3	MTIOC1A		
18		PH2			IRQ1
19		PH1			IRQ0
20		PH0	MTIOC1B		CACREF
21		PC7	MTCLKB	TXD1/SMOSI1/SSDA1/MISOA	CACREF
22		PC6	MTCLKA	RXD1/SMISO1/SSCL1/MOSIA	
23		PC5	MTCLKD	SCK1/RSPCKA	
24		PC4	MTCLKC	SCK5/SSLA0	IRQ2/CLKOUT
25		PB5/PC3	MTIOC2A/MTIOC1B		
26		PB3/PC2	MTIOC0A		
27		PB1/PC1	MTIOC0C		IRQ4
28	VCC				
29		PB0/PC0	MTIC5W/MTIOC0C/ RTCOUT	SCL0/RSPCKA	IRQ2/ADTRG0#
30	VSS				
31		PA6	MTIC5V/MTCLKB/MTIOC2A	CTS5#/RTS5#/SS5#/SDA0/MOSIA	IRQ3
32		PA4	MTIC5U/MTCLKA/MTIOC2B	TXD5/SMOSI5/SSDA5/SSLA0	IRQ5
33		PA3	MTIOC0D/MTCLKD/ MTIOC1B	RXD5/SMISO5/SSCL5/MISOA	IRQ6
34		PA1	MTIOC0B/MTCLKC/ RTCOUT	SCK5/SSLA2	
35		PE4	MTIOC1A	MOSIA	IRQ4/AN012
36		PE3	MTIOC0A/MTIOC1B	CTS12#/RTS12#/SS12#/RSPCKA	IRQ3/AN011
37		PE2		RXD12/RXDX12/SMISO12/SSCL12	IRQ7/AN010
38		PE1		TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12	IRQ1/AN009
39		PE0	MTIOC2A	SCK12	IRQ0/AN008
40		PE7			IRQ7/AN015
41		P46*1			AN006
42		P42*1			AN002
43		P41*1			AN001
44	VREFL0	PJ7*1			

Table 1.8 List of Pins and Pin Functions (40-Pin HWQFN)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, RTC)	Communication (SCIe, SCIf, RSPI, RIIC)	Others
1		P27	MTIOC2B	SCK1/SCK12	IRQ3/CMPA2/ CACREF/ADTRG0#
2		P26	MTIOC2A	TXD1/SMOSI1/SSDA1	
3	MD				FINED
4	RES#				
5		P35			NMI
6	XTAL				
7	EXTAL				
8	VCL				
9	VSS				
10	VCC				
11		P32	MTIOC0C		IRQ2
12		P17	MTIOC0C	SCK1/MISOA/SDA0/RXD12/RXDX12/ SMISO12/SSCL12	IRQ7
13		P16		TXD1/SMOSI1/SSDA1/SCL0/MOSIA	IRQ6/ADTRG0#
14		P15	MTIOC0B/MTCLKB	RXD1/SMISO1/SSCL1/RSPCKA	IRQ5/CLKOUT
15		P14	MTIOC0A/MTCLKA	CTS1#/RTS1#/SS1#/SSLA0/TXD12/ TXDX12/SIOX12/SMOSI12/SSDA12	IRQ4
16		PH3	MTIOC1A		
17		PH2			IRQ1
18		PH1			IRQ0
19		PH0	MTIOC1B		CACREF
20		PC4	MTCLKC	SCK5/SSLA0	IRQ2/CLKOUT
21		PB3	MTIOC0A		
22	VCC				
23		PB0	MTIOC0C/MTIC5W	SCL0/RSPCKA	IRQ2/ADTRG0#
24	VSS				
25		PA6	MTIOC2A/MTIC5V/MTCLKB	CTS5#/RTS5#/SS5#/SDA0/MOSIA	IRQ3
26		PA4	MTIOC2B/MTIC5U/MTCLKA	TXD5/SMOSI5/SSDA5/SSLA0	IRQ5
27		PA3	MTIOC0D/MTIOC1B/ MTCLKD	RXD5/SMISO5/SSCL5/MISOA	IRQ6
28		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	
29		PE4	MTIOC1A	MOSIA	IRQ4/AN012
30		PE3	MTIOC0A/MTIOC1B	CTS12#/RTS12#/SS12#/RSPCKA	IRQ3/AN011
31		PE2		RXD12/RXDX12/SMISO12/SSCL12	IRQ7/AN010
32		PE1		TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12	IRQ1/AN009
33		PE0	MTIOC2A	SCK12	IRQ0/AN008
34		P46*1			AN006
35		P42*1			AN002
36		P41*1			AN001
37	VREFL0	PJ7*1			
38	VREFH0	PJ6*1			
39	AVSS0				
40	AVCC0				

Note 1. The power source of the I/O buffer for these pins is AVCC0.

3. Address Space

3.1 Address Space

This MCU has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains program area.
Figure 3.1 shows the memory map.

Table 4.1 List of I/O Registers (Address Order) (11/13)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 C0C3h	PORT3	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C5h	PORT5	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CAh	PORTA	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CBh	PORTB	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CCh	PORTC	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CEh	PORTE	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0D1h	PORTH	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C11Fh	MPC	Write-Protect Register	PWPR	8	8	2 or 3 PCLKB
0008 C120h	PORT	Port Switching Register B	PSRB	8	8	2 or 3 PCLKB
0008 C121h	PORT	Port Switching Register A	PSRA	8	8	2 or 3 PCLKB
0008 C14Ch	MPC	P14 Pin Function Control Register	P14PFS	8	8	2 or 3 PCLKB
0008 C14Dh	MPC	P15 Pin Function Control Register	P15PFS	8	8	2 or 3 PCLKB
0008 C14Eh	MPC	P16 Pin Function Control Register	P16PFS	8	8	2 or 3 PCLKB
0008 C14Fh	MPC	P17 Pin Function Control Register	P17PFS	8	8	2 or 3 PCLKB
0008 C156h	MPC	P26 Pin Function Control Register	P26PFS	8	8	2 or 3 PCLKB
0008 C157h	MPC	P27 Pin Function Control Register	P27PFS	8	8	2 or 3 PCLKB
0008 C158h	MPC	P30 Pin Function Control Register	P30PFS	8	8	2 or 3 PCLKB
0008 C159h	MPC	P31 Pin Function Control Register	P31PFS	8	8	2 or 3 PCLKB
0008 C15Ah	MPC	P32 Pin Function Control Register	P32PFS	8	8	2 or 3 PCLKB
0008 C160h	MPC	P40 Pin Function Control Register	P40PFS	8	8	2 or 3 PCLKB
0008 C161h	MPC	P41 Pin Function Control Register	P41PFS	8	8	2 or 3 PCLKB
0008 C162h	MPC	P42 Pin Function Control Register	P42PFS	8	8	2 or 3 PCLKB
0008 C163h	MPC	P43 Pin Function Control Register	P43PFS	8	8	2 or 3 PCLKB
0008 C164h	MPC	P44 Pin Function Control Register	P44PFS	8	8	2 or 3 PCLKB
0008 C166h	MPC	P46 Pin Function Control Register	P46PFS	8	8	2 or 3 PCLKB
0008 C190h	MPC	PA0 Pin Function Control Register	PA0PFS	8	8	2 or 3 PCLKB
0008 C191h	MPC	PA1 Pin Function Control Register	PA1PFS	8	8	2 or 3 PCLKB
0008 C193h	MPC	PA3 Pin Function Control Register	PA3PFS	8	8	2 or 3 PCLKB
0008 C194h	MPC	PA4 Pin Function Control Register	PA4PFS	8	8	2 or 3 PCLKB
0008 C196h	MPC	PA6 Pin Function Control Register	PA6PFS	8	8	2 or 3 PCLKB
0008 C198h	MPC	PB0 Pin Function Control Register	PB0PFS	8	8	2 or 3 PCLKB
0008 C199h	MPC	PB1 Pin Function Control Register	PB1PFS	8	8	2 or 3 PCLKB
0008 C19Bh	MPC	PB3 Pin Function Control Register	PB3PFS	8	8	2 or 3 PCLKB
0008 C19Dh	MPC	PB5 Pin Function Control Register	PB5PFS	8	8	2 or 3 PCLKB
0008 C19Eh	MPC	PB6 Pin Function Control Register	PB6PFS	8	8	2 or 3 PCLKB
0008 C19Fh	MPC	PB7 Pin Function Control Register	PB7PFS	8	8	2 or 3 PCLKB
0008 C1A2h	MPC	PC2 Pin Function Control Register	PC2PFS	8	8	2 or 3 PCLKB
0008 C1A3h	MPC	PC3 Pin Function Control Register	PC3PFS	8	8	2 or 3 PCLKB
0008 C1A4h	MPC	PC4 Pin Function Control Register	PC4PFS	8	8	2 or 3 PCLKB
0008 C1A5h	MPC	PC5 Pin Function Control Register	PC5PFS	8	8	2 or 3 PCLKB
0008 C1A6h	MPC	PC6 Pin Function Control Register	PC6PFS	8	8	2 or 3 PCLKB
0008 C1A7h	MPC	PC7 Pin Function Control Register	PC7PFS	8	8	2 or 3 PCLKB
0008 C1B0h	MPC	PE0 Pin Function Control Register	PE0PFS	8	8	2 or 3 PCLKB
0008 C1B1h	MPC	PE1 Pin Function Control Register	PE1PFS	8	8	2 or 3 PCLKB
0008 C1B2h	MPC	PE2 Pin Function Control Register	PE2PFS	8	8	2 or 3 PCLKB
0008 C1B3h	MPC	PE3 Pin Function Control Register	PE3PFS	8	8	2 or 3 PCLKB
0008 C1B4h	MPC	PE4 Pin Function Control Register	PE4PFS	8	8	2 or 3 PCLKB
0008 C1B5h	MPC	PE5 Pin Function Control Register	PE5PFS	8	8	2 or 3 PCLKB
0008 C1B6h	MPC	PE6 Pin Function Control Register	PE6PFS	8	8	2 or 3 PCLKB
0008 C1B7h	MPC	PE7 Pin Function Control Register	PE7PFS	8	8	2 or 3 PCLKB
0008 C1C8h	MPC	PH0 Pin Function Control Register	PH0PFS	8	8	2 or 3 PCLKB
0008 C1C9h	MPC	PH1 Pin Function Control Register	PH1PFS	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (12/13)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 C1CAh	MPC	PH2 Pin Function Control Register	PH2PFS	8	8	2 or 3 PCLKB
0008 C1CBh	MPC	PH3 Pin Function Control Register	PH3PFS	8	8	2 or 3 PCLKB
0008 C1D6h	MPC	PJ6 Pin Function Control Register	PJ6PFS	8	8	2 or 3 PCLKB
0008 C1D7h	MPC	PJ7 Pin Function Control Register	PJ7PFS	8	8	2 or 3 PCLKB
0008 C290h	SYSTEM	Reset Status Register 0	RSTSR0	8	8	4 or 5 PCLKB
0008 C291h	SYSTEM	Reset Status Register 1	RSTSR1	8	8	4 or 5 PCLKB
0008 C293h	SYSTEM	Main Clock Oscillator Forced Oscillation Control Register	MOFCR	8	8	4 or 5 PCLKB
0008 C297h	SYSTEM	Voltage Monitoring Circuit Control Register	LVCMPCR	8	8	4 or 5 PCLKB
0008 C298h	SYSTEM	Voltage Detection Level Select Register	LVDLVLR	8	8	4 or 5 PCLKB
0008 C29Ah	SYSTEM	Voltage Monitoring 1 Circuit Control Register 0	LVD1CR0	8	8	4 or 5 PCLKB
0008 C29Bh	SYSTEM	Voltage Monitoring 2 Circuit Control Register 0	LVD2CR0	8	8	4 or 5 PCLKB
0008 C400h	RTC	64-Hz Counter	R64CNT	8	8	2 or 3 PCLKB
0008 C402h	RTC	Second Counter	RSECCNT	8	8	2 or 3 PCLKB
0008 C402h	RTC	Binary Counter 0	BCNT0	8	8	2 or 3 PCLKB
0008 C404h	RTC	Minute Counter	RMINCNT	8	8	2 or 3 PCLKB
0008 C404h	RTC	Binary Counter 1	BCNT1	8	8	2 or 3 PCLKB
0008 C406h	RTC	Hour Counter	RHRCNT	8	8	2 or 3 PCLKB
0008 C406h	RTC	Binary Counter 2	BCNT2	8	8	2 or 3 PCLKB
0008 C408h	RTC	Day-Of-Week Counter	RWKCNT	8	8	2 or 3 PCLKB
0008 C408h	RTC	Binary Counter 3	BCNT3	8	8	2 or 3 PCLKB
0008 C40Ah	RTC	Date Counter	RDAYCNT	8	8	2 or 3 PCLKB
0008 C40Ch	RTC	Month Counter	RMONCNT	8	8	2 or 3 PCLKB
0008 C40Eh	RTC	Year Counter	RYRCNT	16	16	2 or 3 PCLKB
0008 C410h	RTC	Second Alarm Register	RSECAR	8	8	2 or 3 PCLKB
0008 C410h	RTC	Binary Counter 0 Alarm Register	BCNT0AR	8	8	2 or 3 PCLKB
0008 C412h	RTC	Minute Alarm Register	RMINAR	8	8	2 or 3 PCLKB
0008 C412h	RTC	Binary Counter 1 Alarm Register	BCNT1AR	8	8	2 or 3 PCLKB
0008 C414h	RTC	Hour Alarm Register	RHRAR	8	8	2 or 3 PCLKB
0008 C414h	RTC	Binary Counter 2 Alarm Register	BCNT2AR	8	8	2 or 3 PCLKB
0008 C416h	RTC	Day-of-Week Alarm Register	RWKAR	8	8	2 or 3 PCLKB
0008 C416h	RTC	Binary Counter 3 Alarm Register	BCNT3AR	8	8	2 or 3 PCLKB
0008 C418h	RTC	Date Alarm Register	RDAYAR	8	8	2 or 3 PCLKB
0008 C418h	RTC	Binary Counter 0 Alarm Enable Register	BCNT0AER	8	8	2 or 3 PCLKB
0008 C41Ah	RTC	Month Alarm Register	RMONAR	8	8	2 or 3 PCLKB
0008 C41Ah	RTC	Binary Counter 1 Alarm Enable Register	BCNT1AER	8	8	2 or 3 PCLKB
0008 C41Ch	RTC	Year Alarm Register	RYRAR	16	16	2 or 3 PCLKB
0008 C41Ch	RTC	Binary Counter 2 Alarm Enable Register	BCNT2AER	16	16	2 or 3 PCLKB
0008 C41Eh	RTC	Year Alarm Enable Register	RYRAREN	8	8	2 or 3 PCLKB
0008 C41Eh	RTC	Binary Counter 3 Alarm Enable Register	BCNT3AER	8	8	2 or 3 PCLKB
0008 C422h	RTC	RTC Control Register 1	RCR1	8	8	2 or 3 PCLKB
0008 C424h	RTC	RTC Control Register 2	RCR2	8	8	2 or 3 PCLKB
0008 C426h	RTC	RTC Control Register 3	RCR3	8	8	2 or 3 PCLKB
0008 C42Eh	RTC	Time Error Adjustment Register	RADJ	8	8	2 or 3 PCLKB
007F C0ACh	TEMPS	Temperature Sensor Calibration Data Register	TSCDRL	8	8	1 or 2 PCLKB
007F C0ADh	TEMPS	Temperature Sensor Calibration Data Register	TSCDRH	8	8	1 or 2 PCLKB
007F C0B0h	FLASH	Flash Start-Up Setting Monitor Register	FSCMR	16	16	2 or 3 FCLK
007F C0B2h	FLASH	Flash Access Window Start Address Monitor	FAWSMR	16	16	2 or 3 FCLK
007F C0B4h	FLASH	Flash Access Window End Address Monitor Register	FAWEMR	16	16	2 or 3 FCLK
007F C0B6h	FLASH	Flash Initial Setting Register	FISR	8	8	2 or 3 FCLK
007F C0B7h	FLASH	Flash Extra Area Control Register	FEXCR	8	8	2 or 3 FCLK
007F C0B8h	FLASH	Flash Error Address Monitor Register L	FEAML	16	16	2 or 3 FCLK
007F C0BAh	FLASH	Flash Error Address Monitor Register H	FEAMH	8	8	2 or 3 FCLK

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = VREFL0 = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC	–0.3 to +4.6	V
Input voltage	Ports for 5 V tolerant*1	V_{in}	–0.3 to +6.5	V
	Ports P40 to P44, P46, ports PJ6, PJ7	V_{in}	–0.3 to AVCC0 +0.3	V
	Ports other than above	V_{in}	–0.3 to VCC +0.3	V
Reference power supply voltage		VREFH0	–0.3 to AVCC0 +0.3	V
Analog power supply voltage		AVCC0	–0.3 to +4.6	V
Analog input voltage		V_{AN}	–0.3 to AVCC0 + 0.3 (when AN000 to AN004 and AN006 used) –0.3 to VCC + 0.3 (when AN008 to AN015 used)	V
Operating temperature*2		T_{opr}	–40 to +85 –40 to +105	°C
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.
To preclude any malfunctions due to noise interference, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, and between the VREFH0 and VREFL0 pins. Place capacitors of about 0.1 µF as close as possible to every power supply pin and use the shortest and heaviest possible traces. Also, connect capacitors as stabilization capacitance.

Connect the VCL pin to a VSS pin via a 4.7 µF capacitor. The capacitor must be placed close to the pin, refer to section 5.9.1, Connecting VCL Capacitor and Bypass Capacitors.

Do not input signals or an I/O pull-up power supply to ports other than 5-V tolerant ports while the device is not powered. The current injection that results from input of such a signal or I/O pull-up may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.
If input voltage (within the specified range from -0.3 to + 6.5V) is applied to 5-V tolerant ports, it will not cause problems such as damage to the MCU.

Note 1. Ports P16, P17, PA6, and PB0 are 5 V tolerant.
Note 2. The upper limit of operating temperature is 85°C or 105°C, depending on the product. For details, refer to 1.2 List of Products.

Table 5.2 Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Power supply voltages	VCC*1	1.8	—	3.6	V
	VSS	—	0	—	V
Analog power supply voltages	AVCC0*1, *2	1.8	—	3.6	V
	AVSS0	—	0	—	V
	VREFH0	1.8	—	AVCC0	V
	VREFL0	—	0	—	V

Note 1. Supply AVCC0 simultaneously with or after supplying VCC.
Note 2. Refer to section 27.6.10, Voltage Range of Analog Power Supply Pins in the User's Manual: Hardware to determine the AVCC0 voltage.

5.2 DC Characteristics

Table 5.3 DC Characteristics (1)

Conditions: 2.7 V ≤ VCC ≤ 3.6 V, 2.7 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pin (except for SMBus, 5 V tolerant)	V_{IH}	VCC × 0.7	—	5.8	V	
	Ports P16, P17, port PA6, port PB0 (5 V tolerant)		VCC × 0.8	—	5.8		
	Ports P03, P05, ports P14, P15, ports P26, P27, ports P30 to P32, P35, ports P54, P55, ports PA0, PA1, PA3, PA4, ports PB1, PB3, PB5 to PB7, ports PC0 to PC7, ports PE0 to PE7, ports PH0 to PH3, PH7, RES#		VCC × 0.8	—	VCC + 0.3		
	RIIC input pin (except for SMBus)	V_{IL}	–0.3	—	VCC × 0.3		
	Other than RIIC input pin		–0.3	—	VCC × 0.2		
	RIIC input pin (except for SMBus)	ΔV_T	VCC × 0.05	—	—		
	Other than RIIC input pin		VCC × 0.1	—	—		
Input voltage (except for Schmitt trigger input pins)	MD	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	XTAL (external clock input)		VCC × 0.8	—	VCC + 0.3		
	Ports P40 to P44, P46, ports PJ6, PJ7		AVCC0 × 0.7	—	AVCC0 + 0.3		
	RIIC input pin (SMBus)		2.1	—	VCC + 0.3		
	MD	V_{IL}	–0.3	—	VCC × 0.1		
	XTAL (external clock input)		–0.3	—	VCC × 0.2		
	Ports P40 to P44, P46, ports PJ6, PJ7		–0.3	—	AVCC0 × 0.3		
	RIIC input pin (SMBus)		–0.3	—	0.8		

Table 5.7 DC Characteristics (5) (1/2)

Conditions: 1.8 V ≤ VCC ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

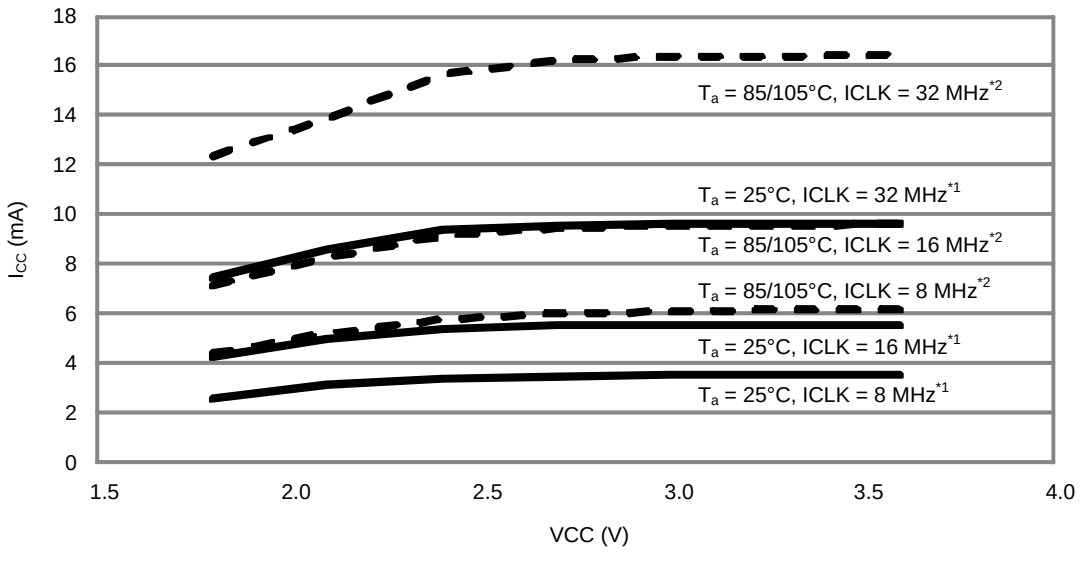
Item					Symbol	Typ *4	Max	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 32 MHz	I_{CC}	3.2	—	mA	
				ICLK = 16 MHz		2.1	—		
				ICLK = 8 MHz		1.5	—		
			All peripheral operation: Normal*3	ICLK = 32 MHz		9.6	—		
				ICLK = 16 MHz		5.6	—		
				ICLK = 8 MHz		3.5	—		
			All peripheral operation: Max.*3	ICLK = 32 MHz		—	21.6		
		Sleep mode	No peripheral operation*2	ICLK = 32 MHz		1.5	—		
				ICLK = 16 MHz		1.2	—		
				ICLK = 8 MHz		1.0	—		
			All peripheral operation: Normal*3	ICLK = 32 MHz		5.1	—		
				ICLK = 16 MHz		3.1	—		
				ICLK = 8 MHz		2.0	—		
		Deep sleep mode	No peripheral operation*2	ICLK = 32 MHz		1.0	—		
				ICLK = 16 MHz		0.80	—		
				ICLK = 8 MHz		0.70	—		
			All peripheral operation: Normal*3	ICLK = 32 MHz		3.4	—		
				ICLK = 16 MHz		2.2	—		
				ICLK = 8 MHz		1.5	—		
	Middle-speed operating modes	Normal operating mode	No peripheral operation*5	ICLK = 12 MHz	I_{CC}	1.7	—	mA	
				ICLK = 8 MHz		1.3	—		
				ICLK = 1 MHz		0.72	—		
			All peripheral operation: Normal*6	ICLK = 12 MHz		4.2	—		
				ICLK = 8 MHz		3.3	—		
				ICLK = 1 MHz		1.2	—		
			All peripheral operation: Max.*6	ICLK = 12 MHz		—	10		
		Sleep mode	No peripheral operation*5	ICLK = 12 MHz		1.0	—		
				ICLK = 8 MHz		0.82	—		
				ICLK = 1 MHz		0.65	—		
			All peripheral operation: Normal*6	ICLK = 12 MHz		2.3	—		
				ICLK = 8 MHz		1.9	—		
				ICLK = 1 MHz		1.0	—		
		Deep sleep mode	No peripheral operation*5	ICLK = 12 MHz		0.8	—		
				ICLK = 8 MHz		0.66	—		
				ICLK = 1 MHz		0.58	—		
			All peripheral operation: Normal*6	ICLK = 12 MHz		1.6	—		
				ICLK = 8 MHz		1.5	—		
				ICLK = 1 MHz		0.87	—		

Table 5.7 DC Characteristics (5) (2/2)

Conditions: 1.8 V ≤ VCC ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

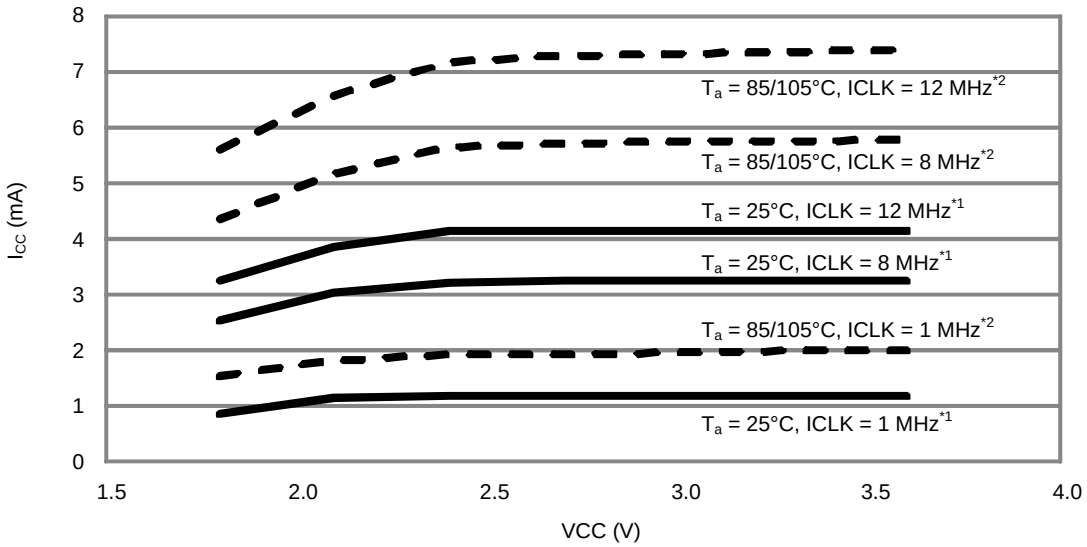
Item					Symbol	Typ *4	Max	Unit	Test Conditions
Supply current*1	Low-speed operating mode	Normal operating mode	No peripheral operation*7	ICLK = 32.768 kHz	I_{CC}	3.9	—	µA	
			All peripheral operation: Normal*8, *9	ICLK = 32.768 kHz		10.4	—		
			All peripheral operation: Max.*8, *9	ICLK = 32.768 kHz		—	36		
		Sleep mode	No peripheral operation*7	ICLK = 32.768 kHz		2.1	—		
			All peripheral operation: Normal*8	ICLK = 32.768 kHz		5.6	—		
		Deep sleep mode	No peripheral operation*7	ICLK = 32.768 kHz		1.7	—		
			All peripheral operation: Normal*8	ICLK = 32.768 kHz		3.9	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. Clock supply to the peripheral functions is stopped. The clock source is HOCO. FCLK and PCLK are set to divided by 64.
Note 3. Clocks are supplied to the peripheral functions. The clock source is HOCO. FCLK and PCLK are set to the same frequency as ICLK.
Note 4. Values when VCC = 3.3 V.
Note 5. Clock supply to the peripheral functions is stopped. The clock source is the main oscillation circuit when ICLK = 12 MHz and HOCO when ICLK = 8 or 1 MHz. FCLK and PCLK are set to divided by 64.
Note 6. Clocks are supplied to the peripheral functions. The clock source is the main oscillation circuit when ICLK = 12 MHz and HOCO when ICLK = 8 or 1 MHz. FCLK and PCLK are set to the same frequency as ICLK.
Note 7. Clock supply to the peripheral functions is stopped. The clock source is the sub-clock oscillator. FCLK and PCLK are set to divided by 64.
Note 8. Clocks are supplied to the peripheral functions. The clock source is the sub-clock oscillator. FCLK and PCLK are set to the same frequency as ICLK.
Note 9. Values when the MSTPCRA.MSTPA17 bit (12-bit A/D converter module stop bit) is set to “transition to the module stop state is made”.



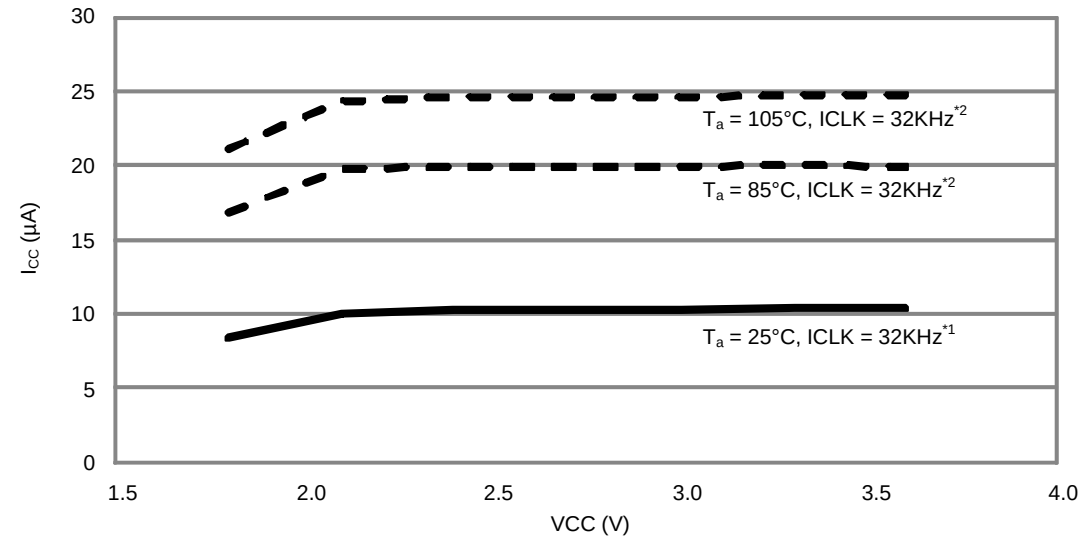
Note 1. All peripheral operation is normal. Average value of the tested middle samples during product evaluation
Note 2. All peripheral operation is maximum. Average value of the tested upper-limit samples during product evaluation.

Figure 5.1 Voltage Dependency in High-Speed Operating Mode (Reference Data)



Note 1. All peripheral operation is normal. Average value of the tested middle samples during product evaluation
Note 2. All peripheral operation is maximum. Average value of the tested upper-limit samples during product evaluation.

Figure 5.2 Voltage Dependency in Middle-Speed Operating Mode (Reference Data)



Note 1. All peripheral operation is normal. Average value of the tested middle samples during product evaluation
Note 2. All peripheral operation is maximum. Average value of the tested upper-limit samples during product evaluation.

Figure 5.3 Voltage Dependency in Low-Speed Operating Mode (Reference Data)

5.3.2 Reset Timing

Table 5.23 Reset Timing

Conditions: 1.8 V ≤ VCC ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	At power-on	t_{RESWP}	3	—	—	ms	Figure 5.25
	Other than above	t_{RESW}	30	—	—	μs	Figure 5.26
Wait time after RES# cancellation (at power-on)	At normal startup*1	t_{RESWT}	—	8.5	—	ms	Figure 5.25
	During fast startup time*2	t_{RESWT}	—	560	—	μs	
Wait time after RES# cancellation (during powered-on state)		t_{RESWT}	—	114	—	μs	Figure 5.26
Independent watchdog timer reset period		t_{RESWIW}	—	1	—	IWDT clock cycle	Figure 5.27
Software reset period		t_{RESWSW}	—	1	—	ICLK cycle	
Wait time after independent watchdog timer reset cancellation*3		t_{RESW2}	—	300	—	μs	
Wait time after software reset cancellation		t_{RESW2}	—	168	—	μs	

Note 1. When OFS1.(STUPLVD1REN, FASTSTUP) = 11b.
Note 2. When OFS1.(STUPLVD1REN, FASTSTUP) ≠ 11b.
Note 3. When IWDTCR.CKS[3:0] = 0000b.

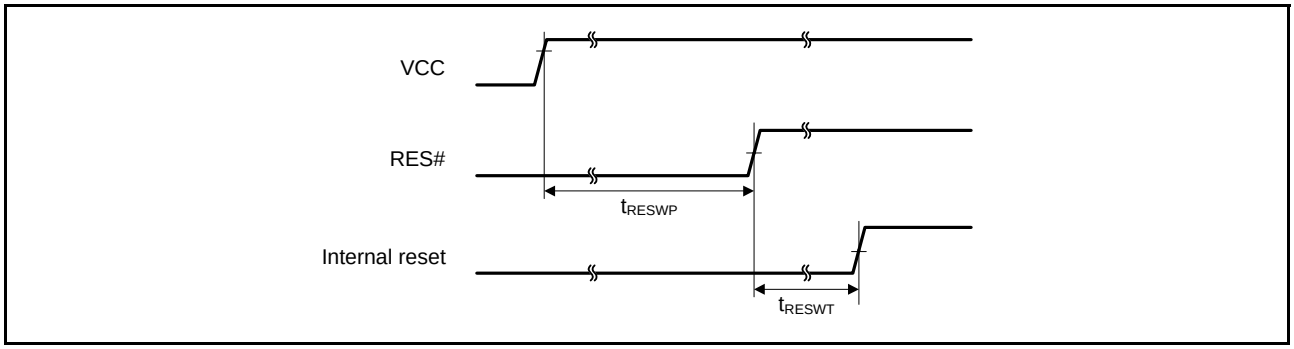


Figure 5.25 Reset Input Timing at Power-On

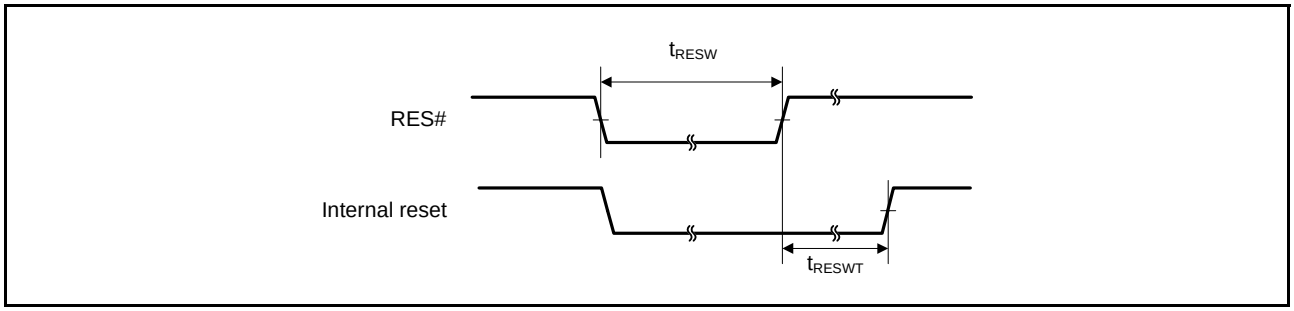


Figure 5.26 Reset Input Timing (1)

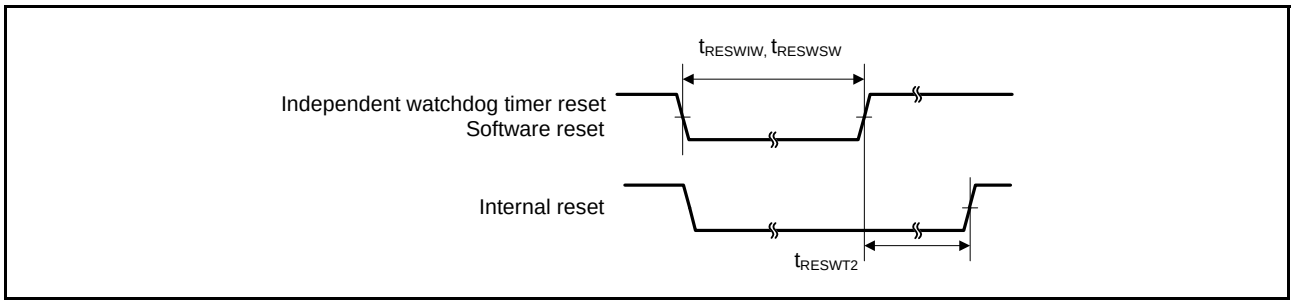


Figure 5.27 Reset Input Timing (2)

Table 5.31 Timing of On-Chip Peripheral Modules (2)

Conditions: 1.8 V ≤ VCC ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C, C = 30 pF

Item				Symbol	Min.	Max.	Unit	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc} *1	Figure 5.39
		Slave			8	4096		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time	Output	2.7 V or above	t_{SPCKr}, t_{SPCKf}	—	10	ns	
			1.8 V or above		—	15		
		Input			—	1	µs	
	Data input setup time	Master	2.7 V or above	t_{SU}	10	—	ns	Figure 5.40 to Figure 5.45
			1.8 V or above		30	—		
		Slave			$25 - t_{Pcyc}$	—		
	Data input hold time	Master	RSPCK set to a division ratio other than PCLKB divided by 2	t_H	t_{Pcyc}	—	ns	
			RSPCK set to PCLKB divided by 2	t_{HF}	0	—		
		Slave		t_H	$20 + 2 \times t_{Pcyc}$	—		
	SSL setup time	Master		t_{LEAD}	$–30 + N^{*2} \times t_{SPcyc}$	—	ns	
		Slave			2	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	$–30 + N^{*3} \times t_{SPcyc}$	—	ns	
		Slave			2	—	t_{Pcyc}	
	Data output delay time	Master	2.7 V or above	t_{OD}	—	14	ns	
			1.8 V or above		—	30		
		Slave	2.7 V or above		—	$3 \times t_{Pcyc} + 65$		
			1.8 V or above		—	$3 \times t_{Pcyc} + 105$		
	Data output hold time	Master	2.7 V or above	t_{OH}	0	—	ns	
			1.8 V or above		–20	—		
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$4 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output	2.7 V or above	t_{Dr}, t_{Df}	—	10	ns	
			1.8 V or above		—	20		
		Input			—	1	µs	
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	20	ns	
		Input			—	1	µs	
	Slave access time		2.7 V or above	t_{SA}	—	6	t_{Pcyc}	Figure 5.44, Figure 5.45
			1.8 V or above		—	7		
	Slave output release time		2.7 V or above	t_{REL}	—	5	t_{Pcyc}	
			1.8 V or above		—	6		

Note 1. t_{Pcyc}: PCLK cycle
Note 2. N: An integer from 1 to 8 that can be set by the RSPI clock delay register (SPCKD)
Note 3. N: An integer from 1 to 8 that can be set by the RSPI slave select negation delay register (SSLND)

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actually output code.

Offset error

Offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

5.5 Temperature Sensor Characteristics

Table 5.40 Temperature Sensor Characteristics

Conditions: 2.0 V ≤ VCC ≤ 3.6 V, 2.0 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	—	±1.5	—	°C	2.4 V or above
		—	±2.0	—		Below 2.4 V
Temperature slope	—	—	–3.65	—	mV/°C	
Output voltage (at 25°C)	—	—	1.05	—	V	VCC = 3.3 V
Temperature sensor start time	t_{START}	—	—	5	µs	
Sampling time	—	5	—	—	µs	

5.6 Power-On Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.41 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (1)

Conditions: 1.8 V ≤ VCC ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	1.35	1.50	1.65	V	Figure 5.49, Figure 5.50
	Voltage detection circuit (LVD1)*1	V_{det1_4}	3.00	3.10	3.20	V	Figure 5.51 At falling edge VCC
		V_{det1_5}	2.91	3.00	3.09		
		V_{det1_6}	2.81	2.90	2.99		
		V_{det1_7}	2.70	2.79	2.88		
		V_{det1_8}	2.60	2.68	2.76		
		V_{det1_9}	2.50	2.58	2.66		
		V_{det1_A}	2.40	2.48	2.56		
		V_{det1_B}	1.99	2.06	2.13		
		V_{det1_C}	1.90	1.96	2.02		
		V_{det1_D}	1.80	1.86	1.92		

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD2), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. n in the symbol Vdet1_n denotes the value of the LVDLVLR.LVD1LVL[3:0] bits.

Table 5.42 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (2)

Conditions: 1.8 V ≤ VCC ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Voltage detection circuit (LVD2)*1	V_{det2_0}	2.71	2.90	3.09	V	Figure 5.52 At falling edge VCC
		V_{det2_1}	2.43	2.60	2.77		
		V_{det2_2}	1.87	2.00	2.13		
		V_{det2_3}*2	1.69	1.80	1.91		
Wait time after power-on reset cancellation	At normal startup*3	t_{POR}	—	9.1	—	ms	Figure 5.50
	During fast startup time*4	t_{POR}	—	1.6	—		
Wait time after voltage monitoring 1 reset cancellation	Power-on voltage monitoring 1 reset disabled*3	t_{LVD1}	—	568	—	µs	Figure 5.51
	Power-on voltage monitoring 1 reset enabled*4		—	100	—		
Wait time after voltage monitoring 2 reset cancellation		t_{LVD2}	—	100	—	µs	Figure 5.52
Response delay time		t_{det}	—	—	350	µs	Figure 5.49
Minimum VCC down time*5		t_{VOFF}	350	—	—	µs	Figure 5.49, VCC = 1.0 V or above
Power-on reset enable time		$t_{W(POR)}$	1	—	—	ms	Figure 5.50, VCC = below 1.0 V
LVD operation stabilization time (after LVD is enabled)		$Td_{(E-A)}$	—	—	300	µs	Figure 5.51, Figure 5.52
Hysteresis width (LVD1 and LVD2)		V_{LVH}	—	70	—	mV	Vdet1_4 selected
			—	60	—		Vdet1_5 to 9, LVD2 selected
			—	50	—		When selection is from among Vdet1_A to B.
			—	40	—		When selection is from among Vdet1_C to D.

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD1), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. n in the symbol Vdet2_n denotes the value of the LVDLVLR.LVD2LVL[3:0] bits.

Note 2. Vdet2_3 selection can be used only when the CMPA2 pin input voltage is selected and cannot be used when the power supply voltage (VCC) is selected.

Note 3. When OFS1.(STUPLVD1REN, FASTSTUP) = 11b.

Note 4. When OFS1.(STUPLVD1REN, FASTSTUP) ≠ 11b.

Note 5. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/LVD.

5.7 Oscillation Stop Detection Timing

Table 5.43 Oscillation Stop Detection Circuit Characteristics

Conditions: 1.8 V ≤ VCC ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 5.53

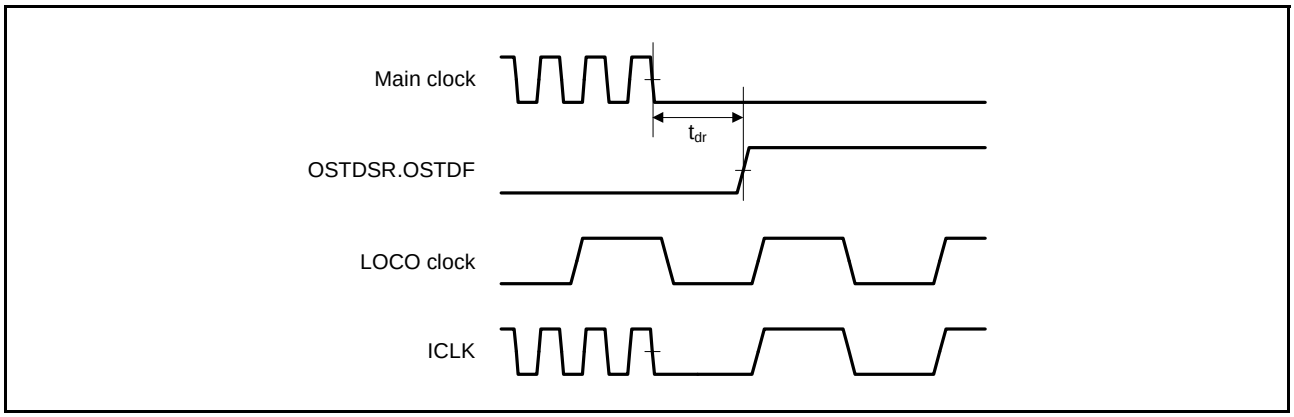


Figure 5.53 Oscillation Stop Detection Timing

5.8 ROM (Flash Memory for Code Storage) Characteristics

Table 5.44 ROM (Flash Memory for Code Storage) Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Reprogramming/erasure cycle*1		N_{PEC}	1000	—	—	Times	
Data hold time	After 1000 times of N_{PEC}	t_{DRP}	20*2, *3	—	—	Year	T_a = +85°C

Note 1. Definition of reprogram/erase cycle: The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 256 times for different addresses in 1-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. Characteristic when using the flash memory programmer and the self-programming library provided from Renesas Electronics.
Note 3. This result is obtained from reliability testing.

Table 5.45 ROM (Flash Memory for Code Storage) Characteristics (2)

High-speed operating mode Conditions: 2.7 V ≤ VCC ≤ 3.6 V, 2.7 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	4-byte	t_{P4}	—	103	931	—	52	489	µs
Erasure time	1-Kbyte	t_{E1K}	—	8.23	267	—	5.48	214	ms
	128-Kbyte	t_{E128K}	—	203	463	—	20	228	ms
Blank check time	4-byte	t_{BC4}	—	—	48	—	—	15.9	µs
	1-Kbyte	t_{BC1K}	—	—	1.58	—	—	0.127	ms
Erase operation forcible stop time		t_{SED}	—	—	21.6	—	—	12.8	µs
Start-up area switching setting time		t_{SAS}	—	12.6	543	—	6.16	432	ms
Access window time		t_{AWS}	—	12.6	543	—	6.16	432	ms
ROM mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	µs
ROM mode transition wait time 2		t_{MS}	5	—	—	5	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%. Confirm the frequency accuracy of the clock source.