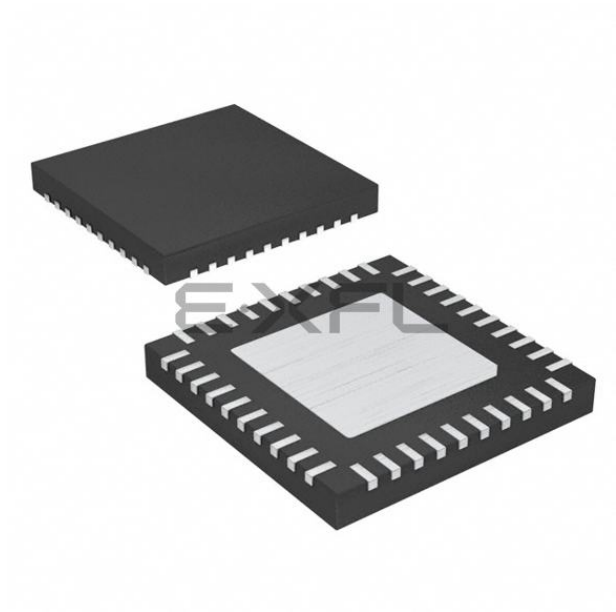
# Renesas Electronics America Inc - R5F51103ADNF#U0 Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | RX |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, SCI, SPI |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 28 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 10K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 8x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 40-WFQFN Exposed Pad |
| Supplier Device Package | 40-HWQFN (6x6) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f51103adnf-u0 |

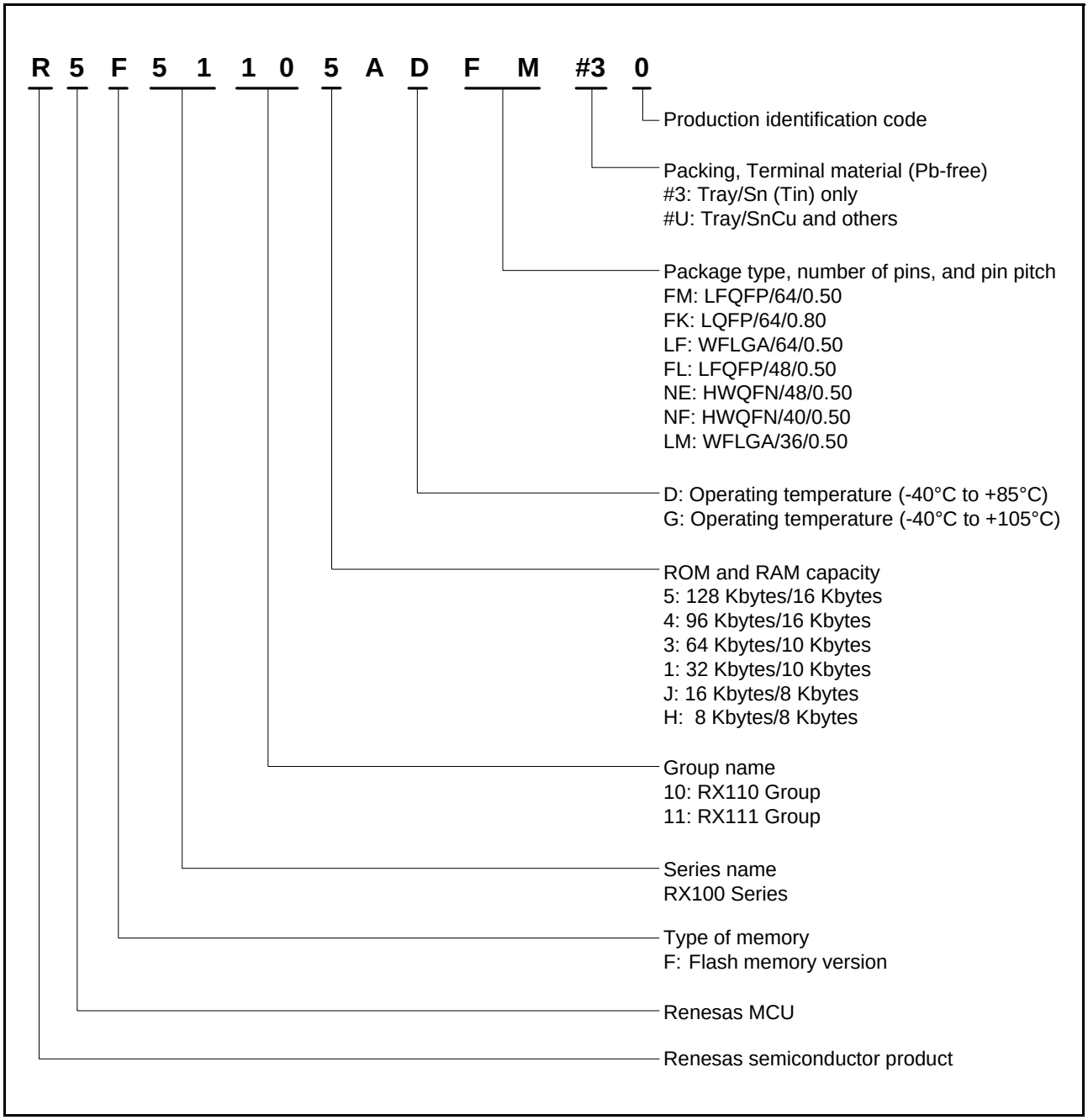



**Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type**

**Table 1.4 Pin Functions (2/3)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Serial communications interface (SCIe) | • Simple I2C mode | | |
| | SSCL1, SSCL5 | I/O | Input/output pins for the I2C clock. |
| | SSDA1, SSDA5 | I/O | Input/output pins for the I2C data. |
| | • Simple SPI mode | | |
| | SCK1, SCK5 | I/O | Input/output pins for the clock. |
| | SMISO1, SMISO5 | I/O | Input/output pins for slave transmit data. |
| | SMOSI1, SMOSI5 | I/O | Input/output pins for master transmit data. |
| | SS1#, SS5# | Input | Chip-select input pins. |
| Serial communications interface (SCIf) | • Asynchronous mode/clock synchronous mode | | |
| | SCK12 | I/O | Input/output pin for the clock. |
| | RXD12 | Input | Input pin for receiving data. |
| | TXD12 | Output | Output pin for transmitting data. |
| | CTS12# | Input | Input pin for controlling the start of transmission and reception. |
| | RTS12# | Output | Output pin for controlling the start of transmission and reception. |
| | • Simple I2C mode | | |
| | SSCL12 | I/O | Input/output pin for the I2C clock. |
| | SSDA12 | I/O | Input/output pin for the I2C data. |
| | • Simple SPI mode | | |
| | SCK12 | I/O | Input/output pin for the clock. |
| | SMISO12 | I/O | Input/output pin for slave transmit data. |
| | SMOSI12 | I/O | Input/output pin for master transmit data. |
| | SS12# | Input | Chip-select input pin. |
| | • Extended serial mode | | |
| | RXDX12 | Input | Input pin for data reception by SCIf. |
| | TXDX12 | Output | Output pin for data transmission by SCIf. |
| | SIOX12 | I/O | Input/output pin for data reception or transmission by SCIf. |
| I2C bus interface | SCL0 | I/O | Input/output pin for I2C bus interface clocks. Bus can be directly driven by the N-channel open drain output. |
| | SDA0 | I/O | Input/output pin for I2C bus interface data. Bus can be directly driven by the N-channel open drain output. |
| Serial peripheral interface | RSPCKA | I/O | Input/output pin for the RSPI clock. |
| | MOSIA | I/O | Input/output pin for transmitting data from the RSPI master. |
| | MISOA | I/O | Input/output pin for transmitting data from the RSPI slave. |
| | SSLA0 | I/O | Input/output pin to select the slave for the RSPI. |
| | SSLA1 to SSLA3 | Output | Output pins to select the slave for the RSPI. |
| 12-bit A/D converter | AN000 to AN004, AN006, AN008 to AN015 | Input | Input pins for the analog signals to be processed by the A/D converter. |
| | ADTRG0# | Input | Input pin for the external trigger signals that start the A/D conversion. |
| I/O ports | P03, P05 | I/O | 2-bit input/output pins. |
| | P14 to P17 | I/O | 4-bit input/output pins. |
| | P26, P27 | I/O | 2-bit input/output pins. |
| | P30 to P32, P35 | I/O | 4-bit input/output pins (P35 input pin). |
| | P40 to P44, P46 | I/O | 6-bit input/output pins. |
| | P54, P55 | I/O | 2-bit input/output pins. |
| | PA0, PA1, PA3, PA4, PA6 | I/O | 5-bit input/output pins. |
| | PB0, PB1, PB3, PB5 to PB7 | I/O | 6-bit input/output pins. |

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

When executing an instruction after writing to multiple registers, only read the last I/O register written to and execute the instruction using that value; it is not necessary to execute the instruction using the values written to all the registers.

### (3) Number of cycles necessary for accessing I/O registers

See Table 4.1 for details on the number of clock cycles necessary for accessing I/O registers.
The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided clock synchronization cycles +
Number of bus cycles for internal peripheral buses 1, 2, and 4 to 6

The number of bus cycles of internal peripheral buses 1, 2, and 4 to 6 differs according to the register to be accessed. When peripheral functions connected to internal peripheral buses 2, and 4 to 6 or registers for the external bus control unit (except for bus error related registers) are accessed, the number of divided clock synchronization cycles is added. The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK) or bus access timing.
In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access cycles shown in Table 4.1.
When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the bus access from the different bus master (DTC).

### (4) Notes on sleep mode and mode transitions

During sleep mode or mode transitions, do not write to the system control related registers (indicated by ‘SYSTEM’ in the Module Symbol column in Table 4.1, List of I/O Registers (Address Order)).

**Table 4.1 List of I/O Registers (Address Order) (3/13)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States |
|---|---|---|---|---|---|---|
| 0008 70DBh | ICU | Interrupt Request Register 219 | IR219 | 8 | 8 | 2 ICLK |
| 0008 70DCh | ICU | Interrupt Request Register 220 | IR220 | 8 | 8 | 2 ICLK |
| 0008 70DDh | ICU | Interrupt Request Register 221 | IR221 | 8 | 8 | 2 ICLK |
| 0008 70DEh | ICU | Interrupt Request Register 222 | IR222 | 8 | 8 | 2 ICLK |
| 0008 70DFh | ICU | Interrupt Request Register 223 | IR223 | 8 | 8 | 2 ICLK |
| 0008 70E0h | ICU | Interrupt Request Register 224 | IR224 | 8 | 8 | 2 ICLK |
| 0008 70E1h | ICU | Interrupt Request Register 225 | IR225 | 8 | 8 | 2 ICLK |
| 0008 70EEh | ICU | Interrupt Request Register 238 | IR238 | 8 | 8 | 2 ICLK |
| 0008 70EFh | ICU | Interrupt Request Register 239 | IR239 | 8 | 8 | 2 ICLK |
| 0008 70F0h | ICU | Interrupt Request Register 240 | IR240 | 8 | 8 | 2 ICLK |
| 0008 70F1h | ICU | Interrupt Request Register 241 | IR241 | 8 | 8 | 2 ICLK |
| 0008 70F2h | ICU | Interrupt Request Register 242 | IR242 | 8 | 8 | 2 ICLK |
| 0008 70F3h | ICU | Interrupt Request Register 243 | IR243 | 8 | 8 | 2 ICLK |
| 0008 70F4h | ICU | Interrupt Request Register 244 | IR244 | 8 | 8 | 2 ICLK |
| 0008 70F5h | ICU | Interrupt Request Register 245 | IR245 | 8 | 8 | 2 ICLK |
| 0008 70F6h | ICU | Interrupt Request Register 246 | IR246 | 8 | 8 | 2 ICLK |
| 0008 70F7h | ICU | Interrupt Request Register 247 | IR247 | 8 | 8 | 2 ICLK |
| 0008 70F8h | ICU | Interrupt Request Register 248 | IR248 | 8 | 8 | 2 ICLK |
| 0008 70F9h | ICU | Interrupt Request Register 249 | IR249 | 8 | 8 | 2 ICLK |
| 0008 711Bh | ICU | DTC Activation Enable Register 027 | DTCER027 | 8 | 8 | 2 ICLK |
| 0008 711Ch | ICU | DTC Activation Enable Register 028 | DTCER028 | 8 | 8 | 2 ICLK |
| 0008 711Dh | ICU | DTC Activation Enable Register 029 | DTCER029 | 8 | 8 | 2 ICLK |
| 0008 712Dh | ICU | DTC Activation Enable Register 045 | DTCER045 | 8 | 8 | 2 ICLK |
| 0008 712Eh | ICU | DTC Activation Enable Register 046 | DTCER046 | 8 | 8 | 2 ICLK |
| 0008 7140h | ICU | DTC Activation Enable Register 064 | DTCER064 | 8 | 8 | 2 ICLK |
| 0008 7141h | ICU | DTC Activation Enable Register 065 | DTCER065 | 8 | 8 | 2 ICLK |
| 0008 7142h | ICU | DTC Activation Enable Register 066 | DTCER066 | 8 | 8 | 2 ICLK |
| 0008 7143h | ICU | DTC Activation Enable Register 067 | DTCER067 | 8 | 8 | 2 ICLK |
| 0008 7144h | ICU | DTC Activation Enable Register 068 | DTCER068 | 8 | 8 | 2 ICLK |
| 0008 7145h | ICU | DTC Activation Enable Register 069 | DTCER069 | 8 | 8 | 2 ICLK |
| 0008 7146h | ICU | DTC Activation Enable Register 070 | DTCER070 | 8 | 8 | 2 ICLK |
| 0008 7147h | ICU | DTC Activation Enable Register 071 | DTCER071 | 8 | 8 | 2 ICLK |
| 0008 7166h | ICU | DTC Activation Enable Register 102 | DTCER102 | 8 | 8 | 2 ICLK |
| 0008 7167h | ICU | DTC Activation Enable Register 103 | DTCER103 | 8 | 8 | 2 ICLK |
| 0008 7172h | ICU | DTC Activation Enable Register 114 | DTCER114 | 8 | 8 | 2 ICLK |
| 0008 7173h | ICU | DTC Activation Enable Register 115 | DTCER115 | 8 | 8 | 2 ICLK |
| 0008 7174h | ICU | DTC Activation Enable Register 116 | DTCER116 | 8 | 8 | 2 ICLK |
| 0008 7175h | ICU | DTC Activation Enable Register 117 | DTCER117 | 8 | 8 | 2 ICLK |
| 0008 7179h | ICU | DTC Activation Enable Register 121 | DTCER121 | 8 | 8 | 2 ICLK |
| 0008 717Ah | ICU | DTC Activation Enable Register 122 | DTCER122 | 8 | 8 | 2 ICLK |
| 0008 717Dh | ICU | DTC Activation Enable Register 125 | DTCER125 | 8 | 8 | 2 ICLK |
| 0008 717Eh | ICU | DTC Activation Enable Register 126 | DTCER126 | 8 | 8 | 2 ICLK |
| 0008 718Bh | ICU | DTC Activation Enable Register 139 | DTCER139 | 8 | 8 | 2 ICLK |
| 0008 718Ch | ICU | DTC Activation Enable Register 140 | DTCER140 | 8 | 8 | 2 ICLK |
| 0008 718Dh | ICU | DTC Activation Enable Register 141 | DTCER141 | 8 | 8 | 2 ICLK |
| 0008 71DBh | ICU | DTC Activation Enable Register 219 | DTCER219 | 8 | 8 | 2 ICLK |
| 0008 71DCh | ICU | DTC Activation Enable Register 220 | DTCER220 | 8 | 8 | 2 ICLK |
| 0008 71DFh | ICU | DTC Activation Enable Register 223 | DTCER223 | 8 | 8 | 2 ICLK |
| 0008 71E0h | ICU | DTC Activation Enable Register 224 | DTCER224 | 8 | 8 | 2 ICLK |
| 0008 71EFh | ICU | DTC Activation Enable Register 239 | DTCER239 | 8 | 8 | 2 ICLK |
| 0008 71F0h | ICU | DTC Activation Enable Register 240 | DTCER240 | 8 | 8 | 2 ICLK |
| 0008 71F7h | ICU | DTC Activation Enable Register 247 | DTCER247 | 8 | 8 | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (8/13)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States |
|---|---|---|---|---|---|---|
| 0008 9034h | S12AD | A/D Data Register 10 | ADDR10 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9036h | S12AD | A/D Data Register 11 | ADDR11 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9038h | S12AD | A/D Data Register 12 | ADDR12 | 16 | 16 | 2 or 3 PCLKB |
| 0008 903Ah | S12AD | A/D Data Register 13 | ADDR13 | 16 | 16 | 2 or 3 PCLKB |
| 0008 903Ch | S12AD | A/D Data Register 14 | ADDR14 | 16 | 16 | 2 or 3 PCLKB |
| 0008 903Eh | S12AD | A/D Data Register 15 | ADDR15 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9060h | S12AD | A/D Sampling State Register 0 | ADSSTR0 | 8 | 8 | 2 or 3 PCLKB |
| 0008 9061h | S12AD | A/D Sampling State Register L | ADSSTRL | 8 | 8 | 2 or 3 PCLKB |
| 0008 9070h | S12AD | A/D Sampling State Register T | ADSSTRT | 8 | 8 | 2 or 3 PCLKB |
| 0008 9071h | S12AD | A/D Sampling State Register O | ADSSTRO | 8 | 8 | 2 or 3 PCLKB |
| 0008 9073h | S12AD | A/D Sampling State Register 1 | ADSSTR1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 9074h | S12AD | A/D Sampling State Register 2 | ADSSTR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 9075h | S12AD | A/D Sampling State Register 3 | ADSSTR3 | 8 | 8 | 2 or 3 PCLKB |
| 0008 9076h | S12AD | A/D Sampling State Register 4 | ADSSTR4 | 8 | 8 | 2 or 3 PCLKB |
| 0008 9078h | S12AD | A/D Sampling State Register 6 | ADSSTR6 | 8 | 8 | 2 or 3 PCLKB |
| 0008 A020h | SCI1 | Serial Mode Register | SMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A021h | SCI1 | Bit Rate Register | BRR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A022h | SCI1 | Serial Control Register | SCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A023h | SCI1 | Transmit Data Register | TDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A024h | SCI1 | Serial Status Register | SSR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A025h | SCI1 | Receive Data Register | RDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A026h | SCI1 | Smart Card Mode Register | SCMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A027h | SCI1 | Serial Extended Mode Register | SEMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A028h | SCI1 | Noise Filter Setting Register | SNFR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A029h | SCI1 | $I^2C$ Mode Register 1 | SIMR1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 A02Ah | SCI1 | $I^2C$ Mode Register 2 | SIMR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 A02Bh | SCI1 | $I^2C$ Mode Register 3 | SIMR3 | 8 | 8 | 2 or 3 PCLKB |
| 0008 A02Ch | SCI1 | $I^2C$ Status Register | SISR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A02Dh | SCI1 | SPI Mode Register | SPMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0A0h | SCI5 | Serial Mode Register | SMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0A1h | SCI5 | Bit Rate Register | BRR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0A2h | SCI5 | Serial Control Register | SCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0A3h | SCI5 | Transmit Data Register | TDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0A4h | SCI5 | Serial Status Register | SSR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0A5h | SCI5 | Receive Data Register | RDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0A6h | SCI5 | Smart Card Mode Register | SCMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0A7h | SCI5 | Serial Extended Mode Register | SEMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0A8h | SCI5 | Noise Filter Setting Register | SNFR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0A9h | SCI5 | $I^2C$ Mode Register 1 | SIMR1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0AAh | SCI5 | $I^2C$ Mode Register 2 | SIMR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0ABh | SCI5 | $I^2C$ Mode Register 3 | SIMR3 | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0ACh | SCI5 | $I^2C$ Status Register | SISR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0ADh | SCI5 | SPI Mode Register | SPMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B000h | CAC | CAC Control Register 0 | CACR0 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B001h | CAC | CAC Control Register 1 | CACR1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B002h | CAC | CAC Control Register 2 | CACR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B003h | CAC | CAC Interrupt Request Enable Register | CAICR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B004h | CAC | CAC Status Register | CASTR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B006h | CAC | CAC Upper-Limit Value Setting Register | CAULVR | 16 | 16 | 2 or 3 PCLKB |
| 0008 B008h | CAC | CAC Lower-Limit Value Setting Register | CALLVR | 16 | 16 | 2 or 3 PCLKB |
| 0008 B00Ah | CAC | CAC Counter Buffer Register | CACNTBR | 16 | 16 | 2 or 3 PCLKB |
| 0008 B080h | DOC | DOC Control Register | DOCR | 8 | 8 | 2 or 3 PCLKB |

**Table 4.1 List of I/O Registers (Address Order) (11/13)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States |
|---|---|---|---|---|---|---|
| 0008 C0C3h | PORT3 | Pull-Up Control Register | PCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0C5h | PORT5 | Pull-Up Control Register | PCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0CAh | PORTA | Pull-Up Control Register | PCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0CBh | PORTB | Pull-Up Control Register | PCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0CCh | PORTC | Pull-Up Control Register | PCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0CEh | PORTE | Pull-Up Control Register | PCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0D1h | PORTH | Pull-Up Control Register | PCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C11Fh | MPC | Write-Protect Register | PWPR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C120h | PORT | Port Switching Register B | PSRB | 8 | 8 | 2 or 3 PCLKB |
| 0008 C121h | PORT | Port Switching Register A | PSRA | 8 | 8 | 2 or 3 PCLKB |
| 0008 C14Ch | MPC | P14 Pin Function Control Register | P14PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C14Dh | MPC | P15 Pin Function Control Register | P15PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C14Eh | MPC | P16 Pin Function Control Register | P16PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C14Fh | MPC | P17 Pin Function Control Register | P17PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C156h | MPC | P26 Pin Function Control Register | P26PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C157h | MPC | P27 Pin Function Control Register | P27PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C158h | MPC | P30 Pin Function Control Register | P30PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C159h | MPC | P31 Pin Function Control Register | P31PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C15Ah | MPC | P32 Pin Function Control Register | P32PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C160h | MPC | P40 Pin Function Control Register | P40PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C161h | MPC | P41 Pin Function Control Register | P41PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C162h | MPC | P42 Pin Function Control Register | P42PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C163h | MPC | P43 Pin Function Control Register | P43PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C164h | MPC | P44 Pin Function Control Register | P44PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C166h | MPC | P46 Pin Function Control Register | P46PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C190h | MPC | PA0 Pin Function Control Register | PA0PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C191h | MPC | PA1 Pin Function Control Register | PA1PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C193h | MPC | PA3 Pin Function Control Register | PA3PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C194h | MPC | PA4 Pin Function Control Register | PA4PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C196h | MPC | PA6 Pin Function Control Register | PA6PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C198h | MPC | PB0 Pin Function Control Register | PB0PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C199h | MPC | PB1 Pin Function Control Register | PB1PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C19Bh | MPC | PB3 Pin Function Control Register | PB3PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C19Dh | MPC | PB5 Pin Function Control Register | PB5PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C19Eh | MPC | PB6 Pin Function Control Register | PB6PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C19Fh | MPC | PB7 Pin Function Control Register | PB7PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1A2h | MPC | PC2 Pin Function Control Register | PC2PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1A3h | MPC | PC3 Pin Function Control Register | PC3PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1A4h | MPC | PC4 Pin Function Control Register | PC4PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1A5h | MPC | PC5 Pin Function Control Register | PC5PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1A6h | MPC | PC6 Pin Function Control Register | PC6PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1A7h | MPC | PC7 Pin Function Control Register | PC7PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1B0h | MPC | PE0 Pin Function Control Register | PE0PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1B1h | MPC | PE1 Pin Function Control Register | PE1PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1B2h | MPC | PE2 Pin Function Control Register | PE2PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1B3h | MPC | PE3 Pin Function Control Register | PE3PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1B4h | MPC | PE4 Pin Function Control Register | PE4PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1B5h | MPC | PE5 Pin Function Control Register | PE5PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1B6h | MPC | PE6 Pin Function Control Register | PE6PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1B7h | MPC | PE7 Pin Function Control Register | PE7PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1C8h | MPC | PH0 Pin Function Control Register | PH0PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1C9h | MPC | PH1 Pin Function Control Register | PH1PFS | 8 | 8 | 2 or 3 PCLKB |

### Table 5.4 DC Characteristics (2)

Conditions: 1.8 V ≤ VCC < 2.7 V, 1.8 V ≤ AVCC0 < 2.7 V, VSS = AVSS0 = 0 V, $T_a$ = –40 to +105°C

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Schmitt trigger input voltage | Ports P16, P17, port PA6, port PB0 (5 V tolerant) | $V_{IH}$ | VCC × 0.8 | — | 5.8 | V | |
| | Ports P03, P05, ports P14, P15, ports P26, P27, ports P30 to P32, P35, ports P54, P55, ports PA0, PA1, PA3, PA4, ports PB1, PB3, PB5 to PB7, ports PC0 to PC7, ports PE0 to PE7, ports PH0 to PH3, PH7, RES# | | VCC × 0.8 | — | VCC + 0.3 | | |
| | All pins | | –0.3 | — | VCC × 0.2 | | |
| | All pins | $\Delta V_T$ | VCC × 0.01 | — | — | | |
| Input voltage (except for Schmitt trigger input pins) | MD | $V_{IH}$ | VCC × 0.9 | — | VCC + 0.3 | V | |
| | XTAL (external clock input) | | VCC × 0.8 | — | VCC + 0.3 | | |
| | Ports P40 to P44, P46, ports PJ6, PJ7 | | AVCC0 × 0.7 | — | AVCC0 + 0.3 | | |
| | MD | $V_{IL}$ | –0.3 | — | VCC × 0.1 | | |
| | XTAL (external clock input) | | –0.3 | — | VCC × 0.2 | | |
| | Ports P40 to P44, P46, ports PJ6, PJ7 | | –0.3 | — | AVCC0 × 0.3 | | |

### Table 5.5 DC Characteristics (3)

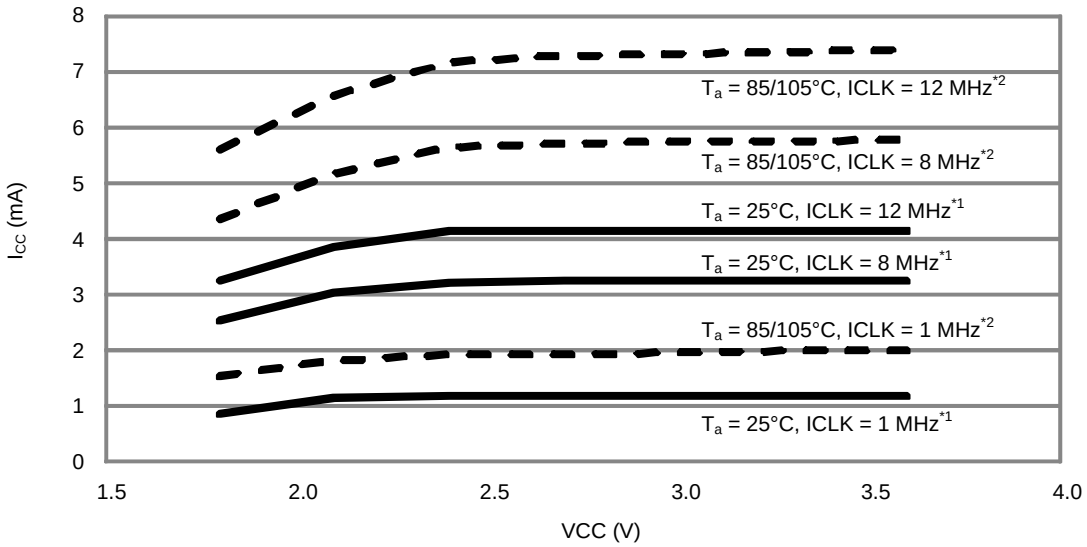
Conditions: 1.8 V ≤ VCC ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, $T_a$ = –40 to +105°C

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Input leakage current | RES#, MD, port P35, port PH7 | $\lvert I_{in} \rvert$ | — | — | 1.0 | µA | $V_{in}$ = 0 V, VCC |
| Three-state leakage current (off-state) | Ports for 5 V tolerant | $\lvert I_{TSI} \rvert$ | — | — | 1.0 | µA | $V_{in}$ = 0 V, 5.8 V |
| | Pins other than above | | — | — | 1.0 | | $V_{in}$ = 0 V, VCC |
| Input capacitance | All input pins (except for port P16, port P35) | $C_{in}$ | — | — | 15 | pF | $V_{in}$ = 0 mV, Frequency: 1 MHz, $T_a$ = 25°C |
| | Port P16, port P35 | | — | — | 30 | | |

### Table 5.6 DC Characteristics (4)

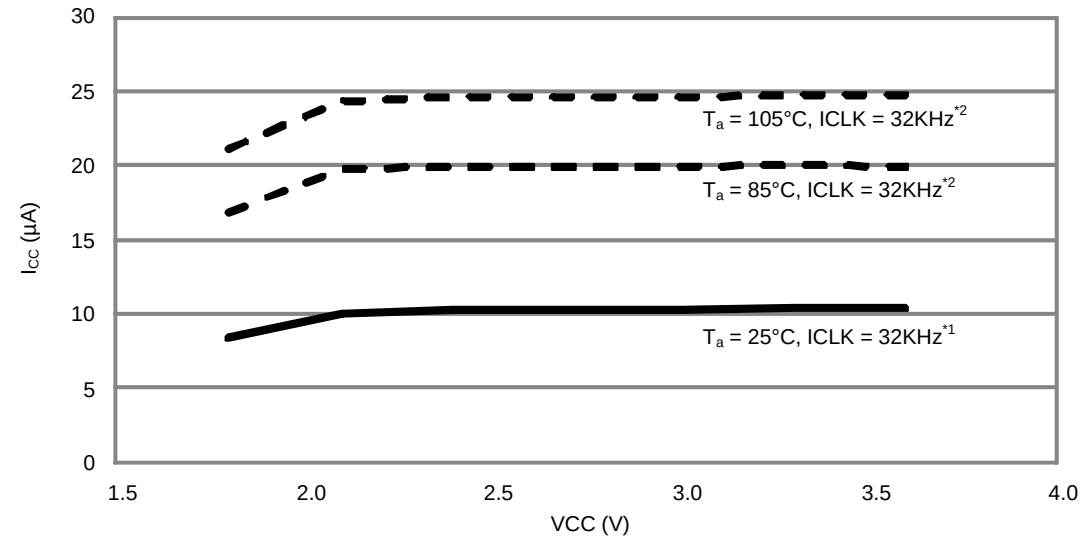
Conditions: 1.8 V ≤ VCC ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, $T_a$ = –40 to +105°C

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Input pull-up resistor | All ports (except for port P35, port PH7) | $R_U$ | 10 | 20 | 100 | kΩ | $V_{in}$ = 0 V |




Note 1. All peripheral operation is normal. Average value of the tested middle samples during product evaluation
Note 2. All peripheral operation is maximum. Average value of the tested upper-limit samples during product evaluation.

**Figure 5.2 Voltage Dependency in Middle-Speed Operating Mode (Reference Data)**




Note 1. All peripheral operation is normal. Average value of the tested middle samples during product evaluation
Note 2. All peripheral operation is maximum. Average value of the tested upper-limit samples during product evaluation.

**Figure 5.3 Voltage Dependency in Low-Speed Operating Mode (Reference Data)**

**Table 5.16 Permissible Output Currents (2)**

Conditions: 1.8 V ≤ VCC ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V,
$T_a$ = –40 to +105°C (G version)

| Item | | Symbol | Max. | Unit |
|---|---|---|---|---|
| Permissible output low current (average value per pin) | Ports P40 to P44, P46, ports PJ6, PJ7 | $I_{OL}$ | 0.4 | mA |
| | Ports other than above | | 8.0 | |
| Permissible output low current (maximum value per pin) | Ports P40 to P44, P46, ports PJ6, PJ7 | | 0.4 | |
| | Ports other than above | | 8.0 | |
| Permissible output low current | Total of ports P40 to P44, P46, ports PJ6, PJ7 | $\Sigma I_{OL}$ | 1.6 | |
| | Total of ports P03, P05, ports P26, P27, ports P30, P31 | | 20 | |
| | Total of ports P14 to P17, port P32, ports P54, P55, ports PB0, PB1, PB3, PB5 to PB7, ports PC2 to PC7, ports PH0 to PH3 | | 20 | |
| | Total of ports PA0, PA1, PA3, PA4, PA6, ports PE0 to PE7 | | 20 | |
| | Total of all output pins | | 40 | |
| Permissible output high current (average value per pin) | Ports P40 to P44, P46, ports PJ6, PJ7 | $I_{OH}$ | –0.1 | |
| | Ports other than above | | –4.0 | |
| Permissible output high current (maximum value per pin) | Ports P40 to P44, P46, ports PJ6, PJ7 | | –0.1 | |
| | Ports other than above | | –4.0 | |
| Permissible output high current | Total of ports P40 to P44, P46, ports PJ6, PJ7 | $\Sigma I_{OH}$ | –0.6 | |
| | Total of ports P03, P05, ports P26, P27, ports P30, P31 | | –10 | |
| | Total of ports P14 to P17, port P32, ports P54, P55, ports PB0, PB1, PB3, PB5 to PB7, ports PC2 to PC7, ports PH0 to PH3 | | –15 | |
| | Total of ports PA0, PA1, PA3, PA4, PA6, ports PE0 to PE7 | | –15 | |
| | Total of all output pins | | –40 | |

Note: Do not exceed the permissible total supply current.

### Table 5.17 Output Voltage (1)

Conditions: 2.7 V ≤ VCC ≤ 3.6 V, 2.7 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, $T_a$ = –40 to +10°C

| Item | | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Low-level output voltage | All output ports (except for RIIC, ports P40 to P44, P46, ports PJ6, PJ7) | | $V_{OL}$ | — | 0.6 | V | $I_{OL}$ = 3.0 mA |
| | | | | — | 0.4 | | $I_{OL}$ = 1.5 mA |
| | Ports P40 to P44, P46, ports PJ6, PJ7 | | | — | 0.4 | | $I_{OL}$ = 0.4 mA |
| | RIIC pins | Standard mode | | — | 0.4 | | $I_{OL}$ = 3.0 mA |
| | | Fast mode | | — | 0.6 | | $I_{OL}$ = 6.0 mA |
| High-level output voltage | All output ports (except for ports P40 to P44, P46, ports PJ6, PJ7) | | $V_{OH}$ | VCC – 0.5 | — | V | $I_{OH}$ = –2.0 mA |
| | Ports P40 to P44, P46, ports PJ6, PJ7 | | | AVCC0 – 0.5 | — | | $I_{OH}$ = –0.1 mA |

### Table 5.18 Output Voltage (2)

Conditions: 1.8 V ≤ VCC ≤ 2.7 V, 1.8 V ≤ AVCC0 ≤ 2.7 V, VSS = AVSS0 = 0 V, $T_a$ = –40 to +105°C

| Item | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Low-level output voltage | All output ports (except for ports P40 to P44, P46, ports PJ6, PJ7) | $V_{OL}$ | — | 0.6 | V | $I_{OL}$ = 1.5 mA |
| | Ports P40 to P44, P46, ports PJ6, PJ7 | | — | 0.4 | | $I_{OL}$ = 0.4 mA |
| High-level output voltage | All output ports (except for ports P40 to P44, P46, ports PJ6, PJ7) | $V_{OH}$ | VCC – 0.5 | — | V | $I_{OH}$ = –1.0 mA |
| | Ports P40 to P44, P46, ports PJ6, PJ7 | | AVCC0 – 0.5 | — | | $I_{OH}$ = –0.1 mA |

### 5.2.1 Standard I/O Pin Output Characteristics (1)

Figure 5.7 to Figure 5.10 show the characteristics of general ports (except for the RIIC output pin, ports P40 to P44, P46, ports PJ6, PJ7).

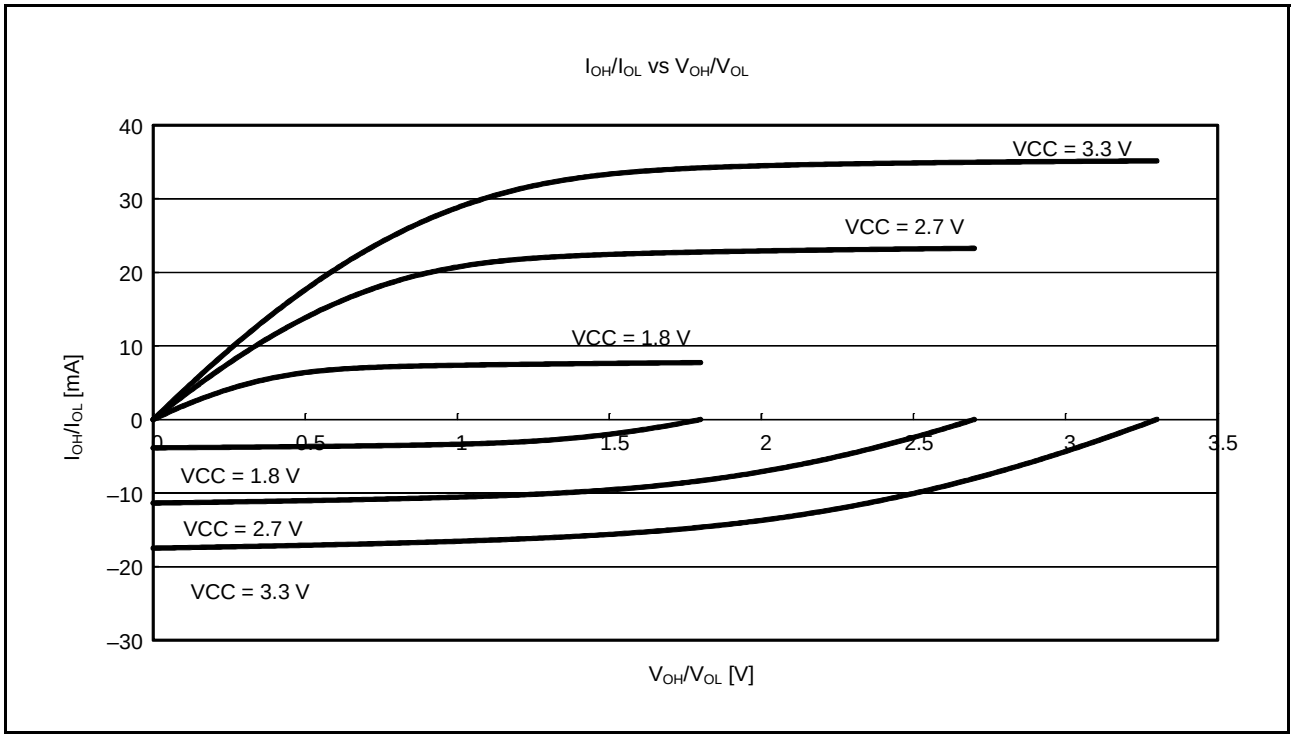



**Figure 5.7 $V_{OH}/V_{OL}$ and $I_{OH}/I_{OL}$ Voltage Characteristics of General Ports (Except for the RIIC Output Pin, Ports P40 to P44, P46, Ports PJ6, PJ7) at $T_a$ = 25°C (Reference Data)**

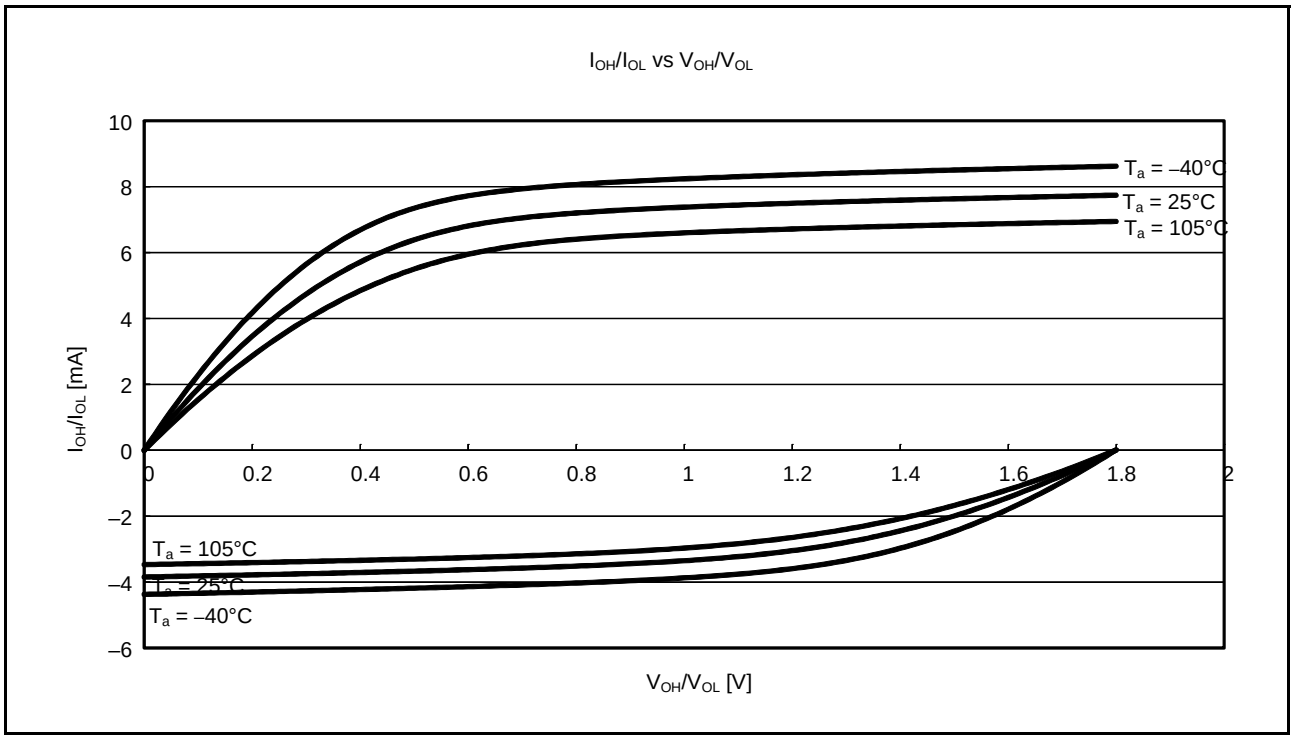



**Figure 5.8 $V_{OH}/V_{OL}$ and $I_{OH}/I_{OL}$ Temperature Characteristics of General Ports (Except for the RIIC Output Pin, Ports P40 to P44, P46, Ports PJ6, PJ7) at VCC = 1.8 V (Reference Data)**

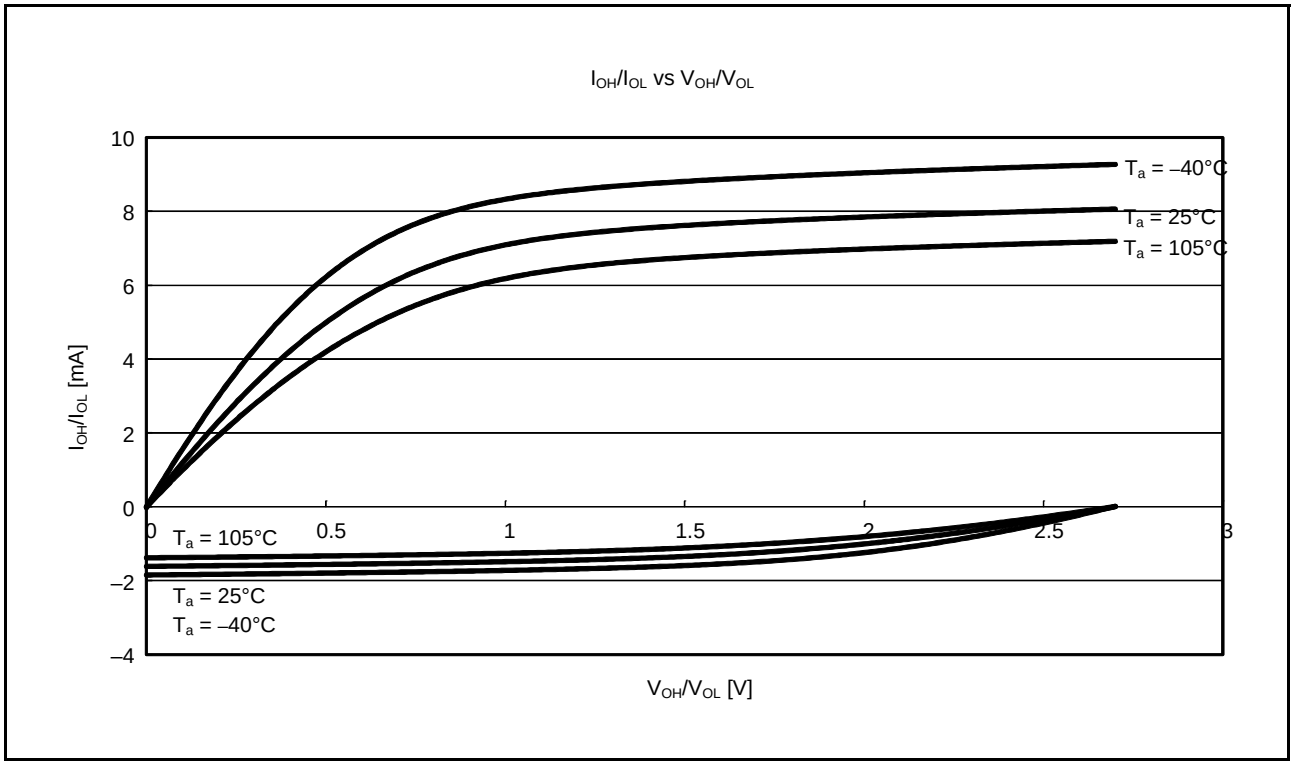



**Figure 5.16 $V_{OH}/V_{OL}$ and $I_{OH}/I_{OL}$ Temperature Characteristics of Ports P40 to P44, P46, Ports PJ6, PJ7 at VCC = 2.7 V (Reference Data)**

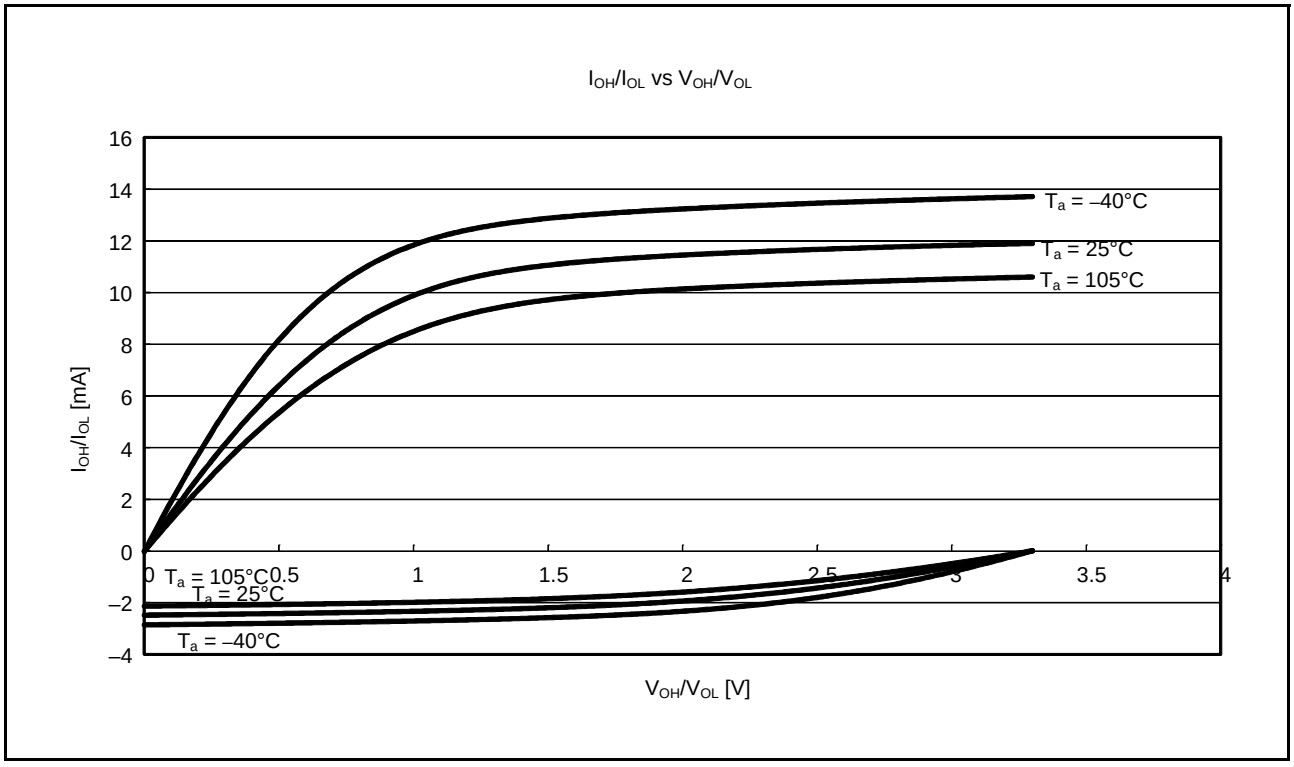



**Figure 5.17 $V_{OH}/V_{OL}$ and $I_{OH}/I_{OL}$ Temperature Characteristics of Ports P40 to P44, P46, Ports PJ6, PJ7 at VCC = 3.3 V (Reference Data)**

**Table 5.27 Timing of Recovery from Low Power Consumption Modes (4)**

Conditions: 1.8 V ≤ VCC ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, $T_a$ = –40 to +105°C

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Recovery time from deep sleep mode*1 | High-speed mode*2 | $t_{DSLP}$ | — | 2 | 3.5 | µs | |
| | Middle-speed mode*3 | $t_{DSLP}$ | — | 3 | 4 | µs | |
| | Low-speed mode*4 | $t_{DSLP}$ | — | 400 | 500 | µs | |

Note: When the division ratios of PCLKB, PCLKD, FCLK, and ICLK are all set to 1.
Note 1. Oscillators continue oscillating in deep sleep mode.
Note 2. When the frequency of the system clock is 32 MHz.
Note 3. When the frequency of the system clock is 12 MHz.
Note 4. When the frequency of the system clock is 32.768 kHz.

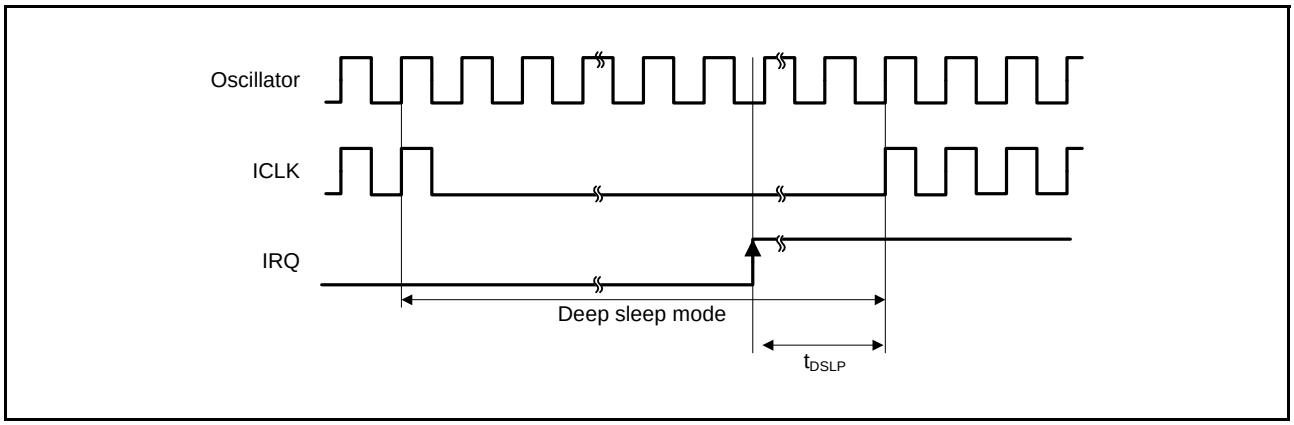



**Figure 5.29 Deep Sleep Mode Cancellation Timing**

**Table 5.28 Timing of Recovery from Low Power Consumption Modes (5) Operating Mode Transition Time**

Conditions: 1.8 V ≤ VCC ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, $T_a$ = -40 to +105°C

| Mode before Transition | Mode after Transition | ICLK Frequency | Transition Time | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| High-speed operating mode | Middle-speed operating mode | 8 MHz | — | 10 | — | µs |
| Middle-speed operating mode | High-speed operating mode | 8 MHz | — | 37.5 | — | µs |
| Low-speed operating mode | Middle-speed operating mode, high-speed operating mode | 32.768 kHz | — | 213.62 | — | µs |
| Middle-speed operating mode, high-speed operating mode | Low-speed operating mode | 32.768 kHz | — | 183.11 | — | µs |

Note: When the division ratios of PCLKB, PCLKD, FCLK, and ICLK are all set to 1.

**Table 5.32 Timing of On-Chip Peripheral Modules (3)**

Conditions: 1.8 V ≤ VCC ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, $T_a$ = –40 to +105°C, C = 30 pF

| Item | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|
| Simple SPI | SCK clock cycle output (master) | | $t_{SPcyc}$ | 4 | 65536 | $t_{Pcyc}$ | Figure 5.39 |
| | SCK clock cycle input (slave) | | | 6 | 65536 | | |
| | SCK clock high pulse width | | $t_{SPCKWH}$ | 0.4 | 0.6 | $t_{SPcyc}$ | |
| | SCK clock low pulse width | | $t_{SPCKWL}$ | 0.4 | 0.6 | $t_{SPcyc}$ | |
| | SCK clock rise/fall time | | $t_{SPCKr}$, $t_{SPCKf}$ | — | 20 | ns | |
| | Data input setup time (master) | 2.7 V or above | $t_{SU}$ | 65 | — | ns | Figure 5.40, Figure 5.42 |
| | | 1.8 V or above | | 95 | — | | |
| | Data input setup time (slave) | | | 40 | — | | |
| | Data input hold time | | $t_H$ | 40 | — | ns | |
| | SS input setup time | | $t_{LEAD}$ | 3 | — | $t_{Pcyc}$ | |
| | SS input hold time | | $t_{LAG}$ | 3 | — | $t_{Pcyc}$ | |
| | Data output delay time (master) | | $t_{OD}$ | — | 40 | ns | |
| | Data output delay time (slave) | 2.7 V or above | | — | 65 | | |
| | | 1.8 V or above | | — | 85 | | |
| | Data output hold time (master) | 2.7 V or above | $t_{OH}$ | –10 | — | ns | |
| | | 1.8 V or above | | –20 | — | | |
| | Data output hold time (slave) | | | –10 | — | | |
| | Data rise/fall time | | $t_{Dr}$, $t_{Df}$ | — | 20 | ns | |
| | SS input rise/fall time | | $t_{SSLr}$, $t_{SSLf}$ | — | 20 | ns | |
| | Slave access time | | $t_{SA}$ | — | 6 | $t_{Pcyc}$ | Figure 5.44, Figure 5.45 |
| | Slave output release time | | $t_{REL}$ | — | 6 | $t_{Pcyc}$ | |

Note 1. $t_{Pcyc}$: PCLK cycle

**Table 5.33 Timing of On-Chip Peripheral Modules (4)**

Conditions: 2.7 V ≤ VCC ≤ 3.6 V, 2.7 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, fPCLKB ≤ 32 MHz, $T_a$ = –40 to +105°C

| Item | | Symbol | Min.*1 | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| RIIC (Standard mode, SMBus) | SCL0 input cycle time | $t_{SCL}$ | 6 (12) × $t_{IICcyc}$ + 1300 | — | ns | Figure 5.46 |
| | SCL0 input high pulse width | $t_{SCLH}$ | 3 (6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL0 input low pulse width | $t_{SCLL}$ | 3 (6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL0, SDA0 input rise time | $t_{Sr}$ | — | 1000 | ns | |
| | SCL0, SDA0 input fall time | $t_{Sf}$ | — | 300 | ns | |
| | SCL0, SDA0 input spike pulse removal time | $t_{SP}$ | 0 | 1 (4) × $t_{IICcyc}$ | ns | |
| | SDA0 input bus free time | $t_{BUF}$ | 3 (6) × $t_{IICcyc}$ + 300 | — | ns | |
| | START condition input hold time | $t_{STAH}$ | $t_{IICcyc}$ + 300 | — | ns | |
| | Repeated START condition input setup time | $t_{STAS}$ | 1000 | — | ns | |
| | STOP condition input setup time | $t_{STOS}$ | 1000 | — | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc}$ + 50 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL0, SDA0 capacitive load | $C_b$ | — | 400 | pF | |
| RIIC (Fast mode) | SCL0 input cycle time | $t_{SCL}$ | 6 (12) × $t_{IICcyc}$ + 600 | — | ns | Figure 5.46 |
| | SCL0 input high pulse width | $t_{SCLH}$ | 3 (6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL0 input low pulse width | $t_{SCLL}$ | 3 (6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL0, SDA0 input rise time | $t_{Sr}$ | —*2 | 300 | ns | |
| | SCL0, SDA0 input fall time | $t_{Sf}$ | —*2 | 300 | ns | |
| | SCL0, SDA0 input spike pulse removal time | $t_{SP}$ | 0 | 1 (4) × $t_{IICcyc}$ | ns | |
| | SDA0 input bus free time | $t_{BUF}$ | 3 (6) × $t_{IICcyc}$ + 300 | — | ns | |
| | START condition input hold time | $t_{STAH}$ | $t_{IICcyc}$ + 300 | — | ns | |
| | Repeated START condition input setup time | $t_{STAS}$ | 300 | — | ns | |
| | STOP condition input setup time | $t_{STOS}$ | 300 | — | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc}$ + 50 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL0, SDA0 capacitive load | $C_b$ | — | 400 | pF | |

Note: $t_{IICcyc}$: RIIC internal reference count clock (IICφ) cycle

Note 1. The value in parentheses is used when the ICMR3.NF[1:0] bits are set to 11b while a digital filter is enabled with the ICFER.NFE bit = 1.

Note 2. The minimum tsr and tsf specifications for fast mode are not set.

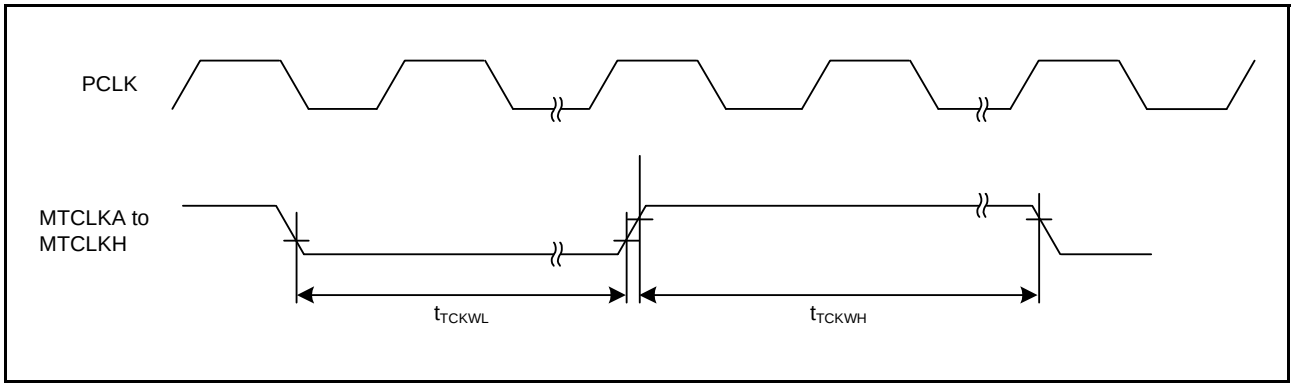



**Figure 5.34 MTU2 Clock Input Timing**

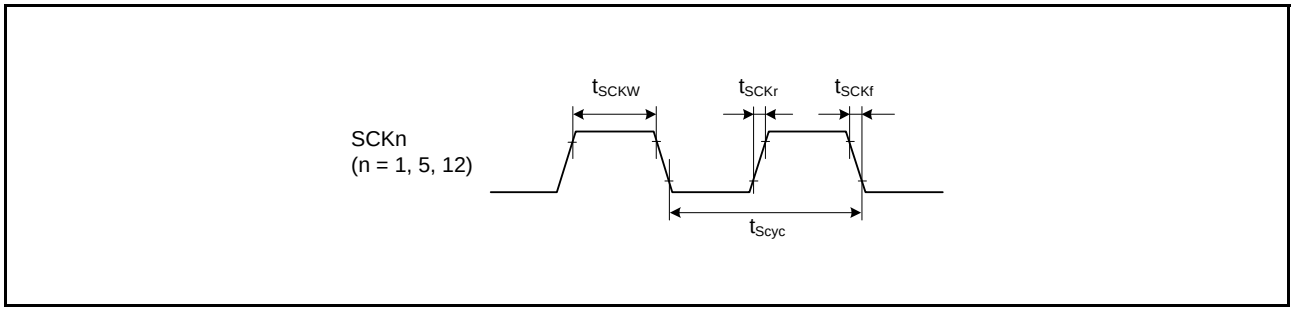



**Figure 5.35 SCK Clock Input Timing**

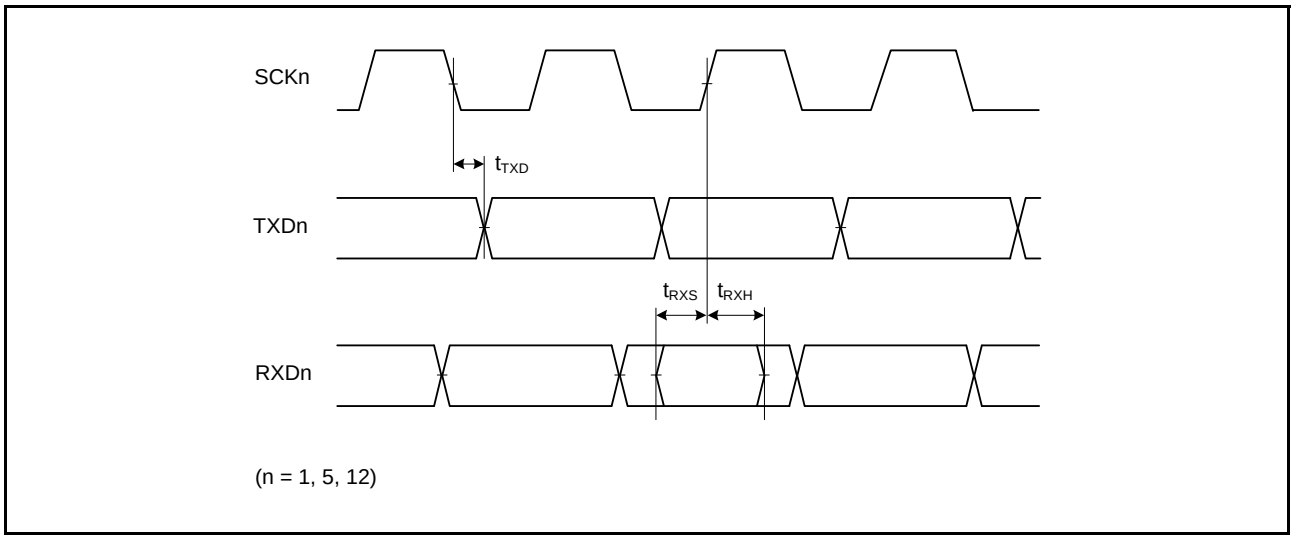



**Figure 5.36 SCI Input/Output Timing: Clock Synchronous Mode**

### Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actually output code.

### Offset error

Offset error is the difference between a transition point of the ideal first output code and the actual first output code.

### Full-scale error

Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

## 5.5 Temperature Sensor Characteristics

**Table 5.40 Temperature Sensor Characteristics**

Conditions: 2.0 V ≤ VCC ≤ 3.6 V, 2.0 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, $T_a$ = –40 to +105°C

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Relative accuracy | — | — | ±1.5 | — | °C | 2.4 V or above |
| | | — | ±2.0 | — | | Below 2.4 V |
| Temperature slope | — | — | –3.65 | — | mV/°C | |
| Output voltage (at 25°C) | — | — | 1.05 | — | V | VCC = 3.3 V |
| Temperature sensor start time | $t_{START}$ | — | — | 5 | µs | |
| Sampling time | — | 5 | — | — | µs | |

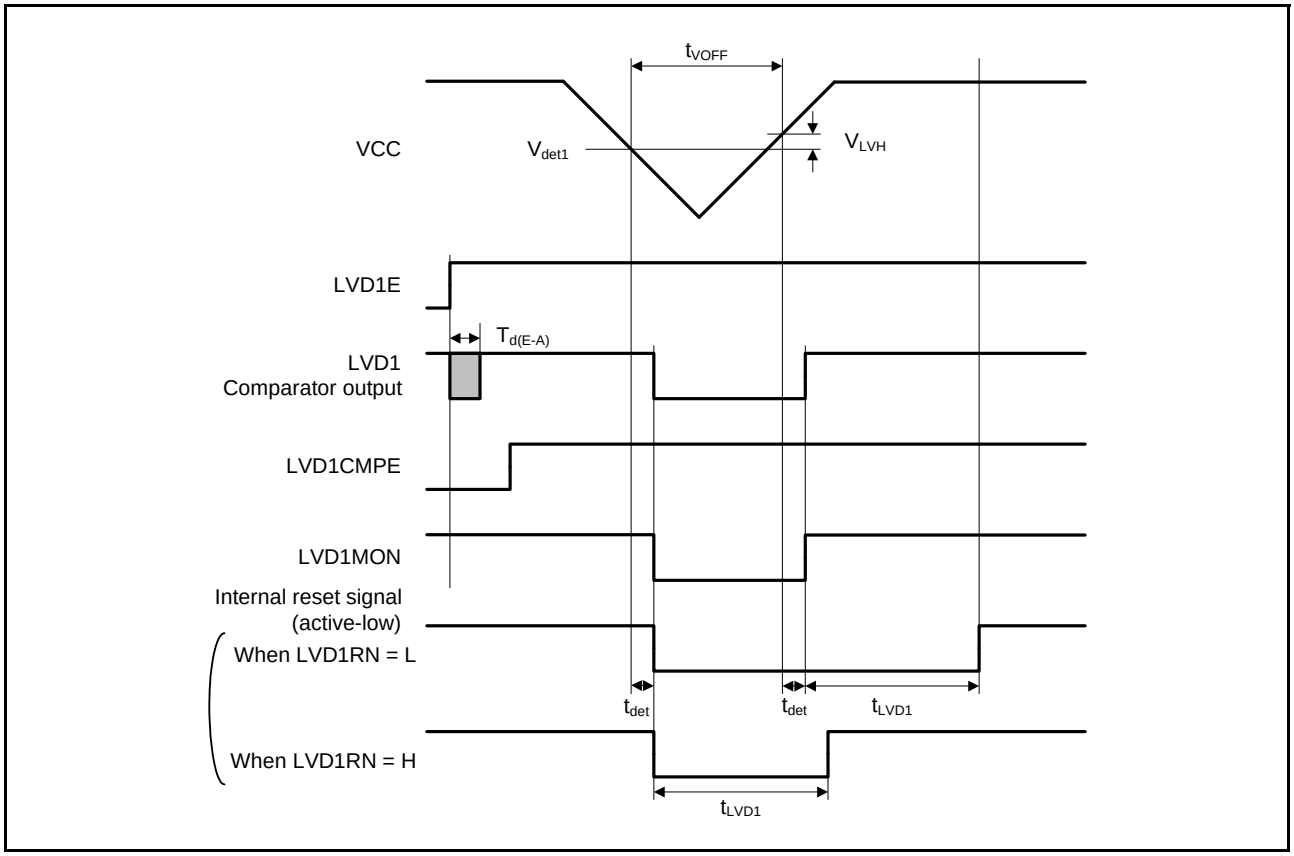



**Figure 5.51 Voltage Detection Circuit Timing ($V_{det1}$)**

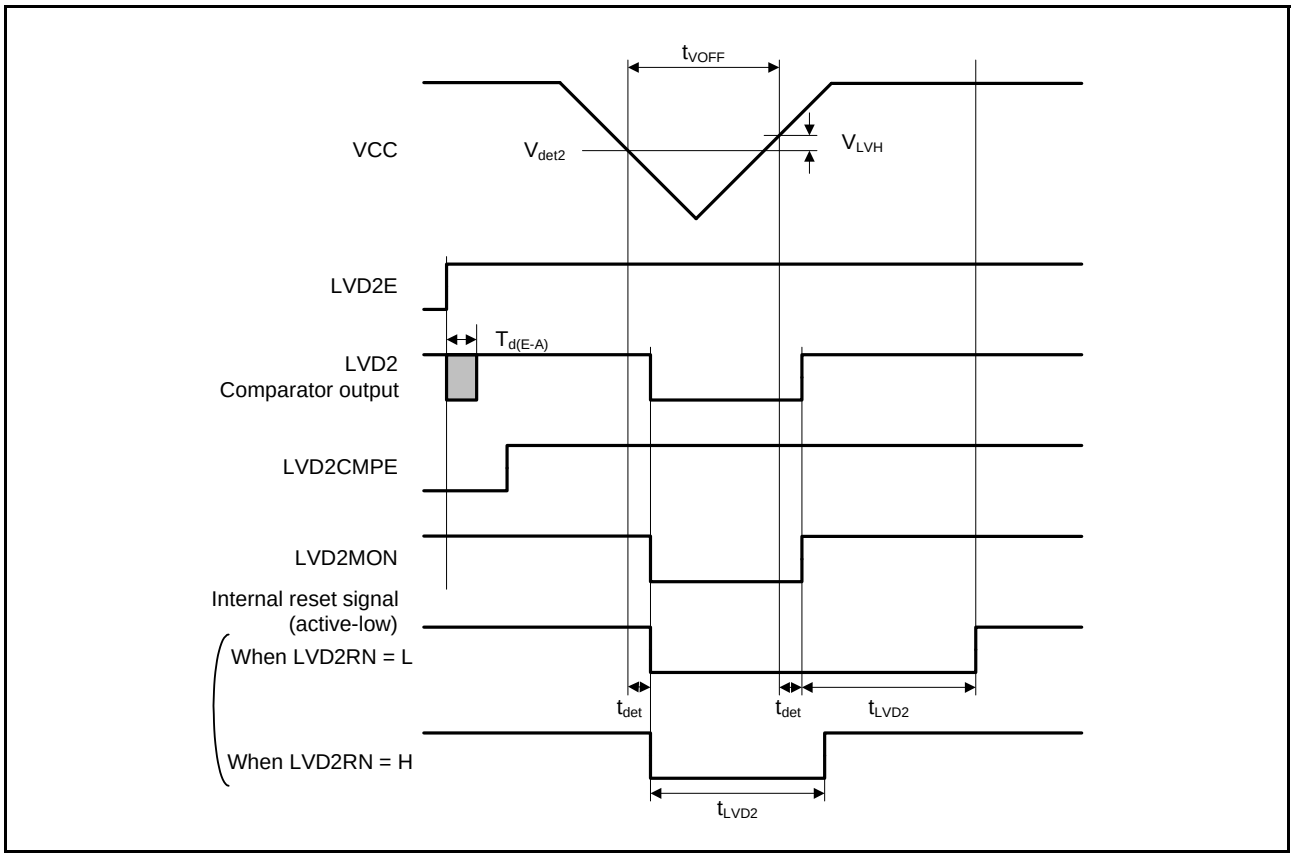
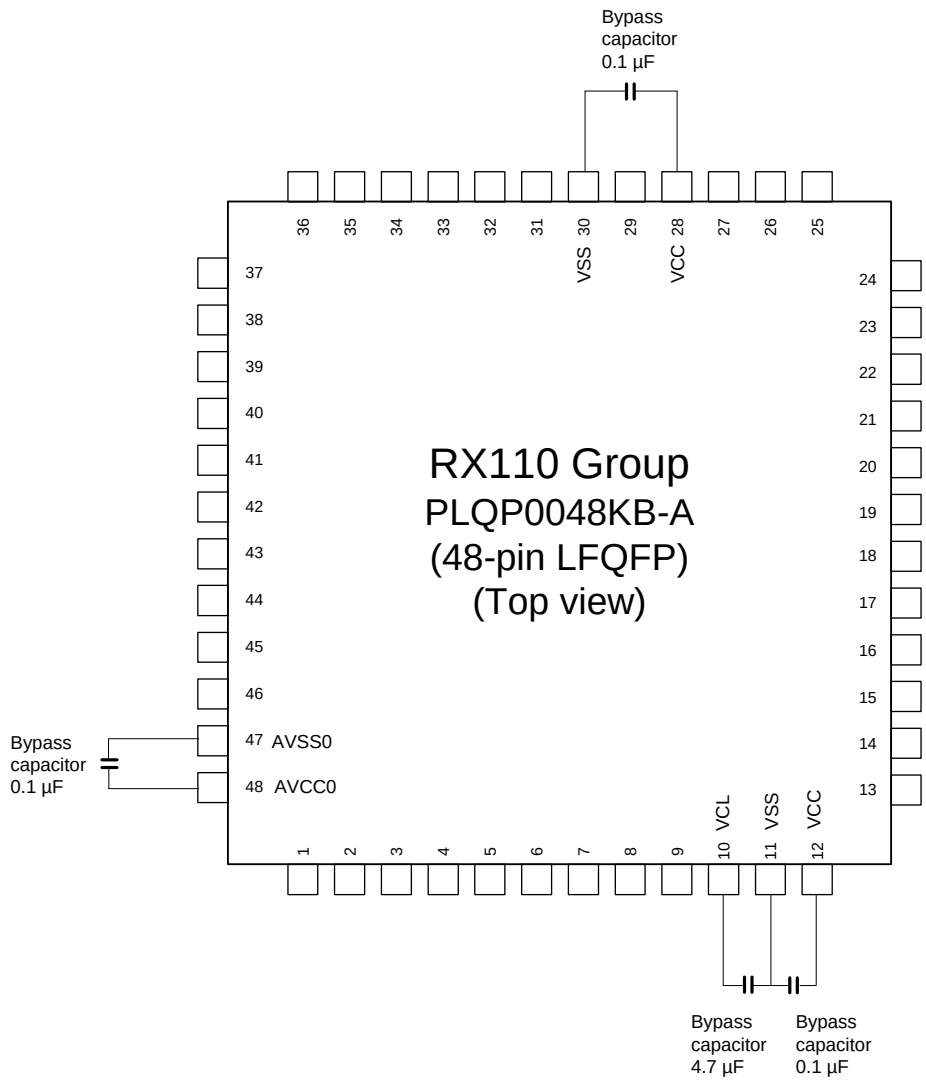


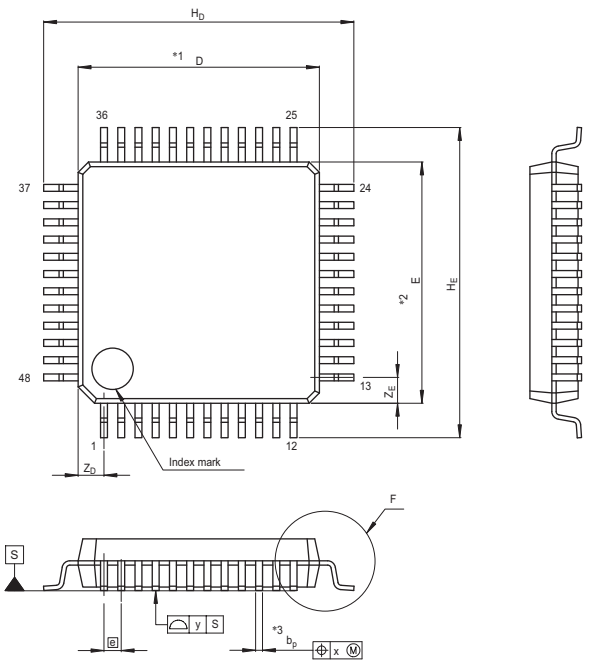

**Figure 5.52 Voltage Detection Circuit Timing ($V_{det2}$)**



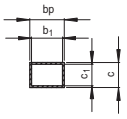

Note. Do not apply the power supply voltage to the VCL pin.
Use a 4.7-µF multilayer ceramic for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

**Figure 5.55 Connecting Capacitors (48-pin LFQFP)**

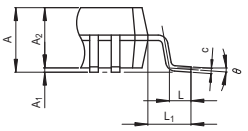
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LFQFP48-7x7-0.50 | PLQP0048KB-A | 48P6Q-A | 0.2g |






Terminal cross section




Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 6.9 | 7.0 | 7.1 |
| E | 6.9 | 7.0 | 7.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 8.8 | 9.0 | 9.2 |
| $H_E$ | 8.8 | 9.0 | 9.2 |
| A | — | — | 1.7 |
| $A_1$ | 0 | 0.1 | 0.2 |
| $b_p$ | 0.17 | 0.22 | 0.27 |
| $b_1$ | — | 0.20 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| θ | 0° | — | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.10 |
| $Z_D$ | — | 0.75 | — |
| $Z_E$ | — | 0.75 | — |
| L | 0.35 | 0.5 | 0.65 |
| $L_1$ | — | 1.0 | — |

Figure D 48-Pin LFQFP (PLQP0048KB-A)