Renesas Electronics America Inc - R5F51104ADFL#30 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f51104adfl-30

Table 1.1 Outline of Specifications (3/3)

Classification	Module/Function	Description
Data operation circuit (DOC)		Comparison, addition, and subtraction of 16-bit data
Unique ID		32-byte ID code for the MCU
Power supply voltages/Operating frequencies		VCC = 1.8 to 2.4 V: 8 MHz, VCC = 2.4 to 2.7 V: 16 MHz, VCC = 2.7 to 3.6 V: 32 MHz
Supply current		3.2 mA at 32 MHz (typ.)
Operating temperatures		D version: –40 to +85°C, G version: –40 to +105°C
Packages		64-pin LFQFP (PLQP0064KB-A) 10 × 10 mm, 0.5 mm pitch 64-pin LQFP (PLQP0064GA-A) 14 × 14 mm, 0.8 mm pitch 64-pin WFLGA (PWLG0064KA-A) 5 × 5 mm, 0.5 mm pitch 48-pin LFQFP (PLQP0048KB-A) 7 × 7 mm, 0.5 mm pitch 48-pin HWQFN (PWQN0048KB-A) 7 × 7 mm, 0.5 mm pitch 40-pin HWQFN (PWQN0040KC-A) 6 × 6 mm, 0.5 mm pitch 36-pin WFLGA (PWLG0036KA-A) 4 × 4 mm, 0.5 mm pitch
On-chip debugging system		E1 emulator (FINE interface)

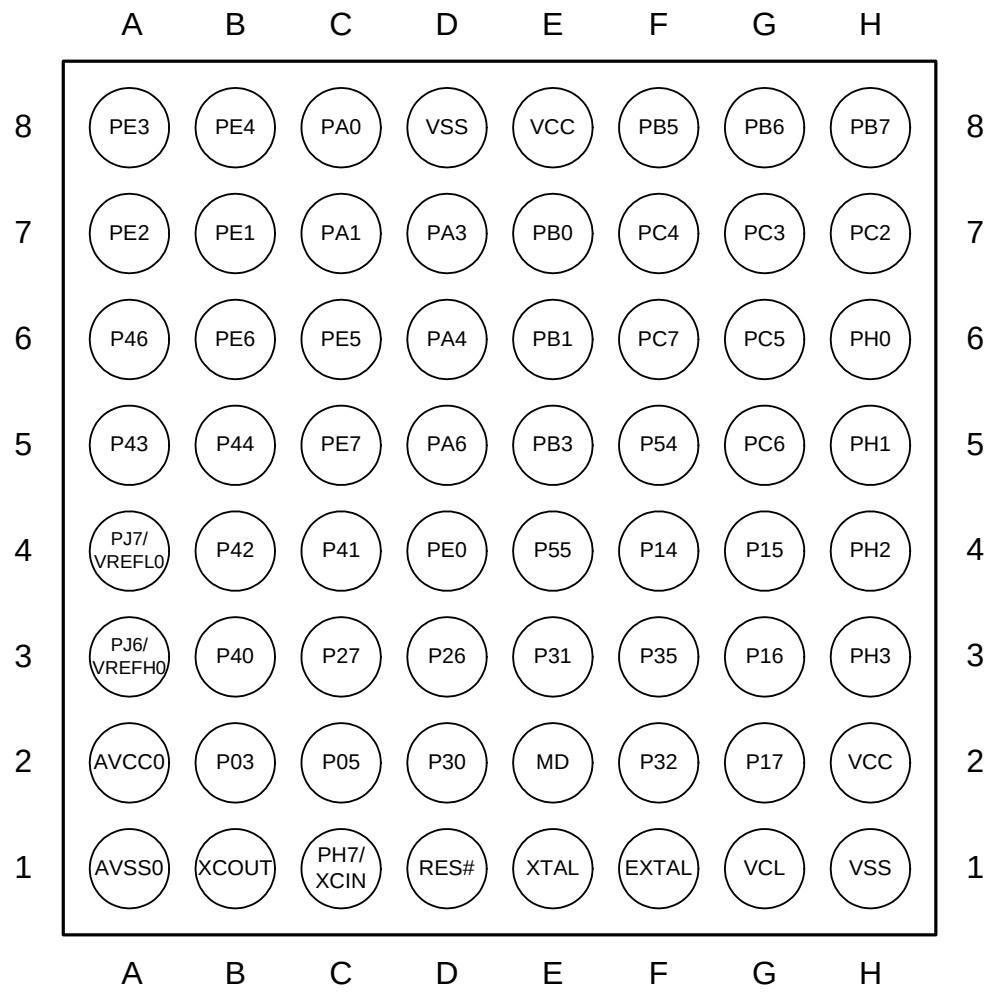
1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/3)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	—	Connect this pin to the VSS pin via the 4.7 µF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC when not using the 12-bit A/D converter.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter. Connect this pin to VSS when not using the 12-bit A/D converter.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC when not using the 12-bit A/D converter.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter. Connect this pin to VSS when not using the 12-bit A/D converter.
Clock	XTAL	Output/ Input *1	Pins for connecting a crystal resonator. An external clock can be input through the XTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCIN and XCOUT.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin.
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on this pin must not be changed during operation.
System control	RES#	Input	Reset pin. This LSI enters the reset state when this signal goes low.
CAC	CACREF	Input	Input pin for the clock frequency accuracy measurement circuit.
On-chip emulator	FINED	I/O	FINE interface pin.
LVD	CMPA2	Input	Detection target voltage pin for voltage detection 2.
Interrupts	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ7	Input	Interrupt request pins.
Multi-function timer pulse unit 2	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.
Realtime clock	RTCOUT	Output	Output pin for the 1-Hz/64-Hz clock.
Serial communications interface (SCIe)	• Asynchronous mode/clock synchronous mode		
	SCK1, SCK5	I/O	Input/output pins for the clock.
	RXD1, RXD5	Input	Input pins for receiving data.
	TXD1, TXD5	Output	Output pins for transmitting data.
	CTS1#, CTS5#	Input	Input pins for controlling the start of transmission and reception.
	RTS1#, RTS5#	Output	Output pins for controlling the start of transmission and reception.

RX110 Group
PWLG0064KA-A
(64-pin WFLGA)
(Upper perspective view)



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (64-Pin WFLGA)”.
Note: For the position of A1 pin in the package, see “Package Dimensions”.

Figure 1.4 Pin Assignments of the 64-Pin WFLGA

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

When executing an instruction after writing to multiple registers, only read the last I/O register written to and execute the instruction using that value; it is not necessary to execute the instruction using the values written to all the registers.

(3) Number of cycles necessary for accessing I/O registers

See Table 4.1 for details on the number of clock cycles necessary for accessing I/O registers.
The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided clock synchronization cycles +
Number of bus cycles for internal peripheral buses 1, 2, and 4 to 6

The number of bus cycles of internal peripheral buses 1, 2, and 4 to 6 differs according to the register to be accessed. When peripheral functions connected to internal peripheral buses 2, and 4 to 6 or registers for the external bus control unit (except for bus error related registers) are accessed, the number of divided clock synchronization cycles is added. The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK) or bus access timing.
In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access cycles shown in Table 4.1.
When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the bus access from the different bus master (DTC).

(4) Notes on sleep mode and mode transitions

During sleep mode or mode transitions, do not write to the system control related registers (indicated by ‘SYSTEM’ in the Module Symbol column in Table 4.1, List of I/O Registers (Address Order)).

Table 4.1 List of I/O Registers (Address Order) (9/13)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 B082h	DOC	DOC Data Input Register	DODIR	16	16	2 or 3 PCLKB
0008 B084h	DOC	DOC Data Setting Register	DODSR	16	16	2 or 3 PCLKB
0008 B300h	SCI12	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 B301h	SCI12	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 B302h	SCI12	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 B303h	SCI12	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 B304h	SCI12	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 B305h	SCI12	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 B306h	SCI12	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 B307h	SCI12	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 B308h	SCI12	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 B309h	SCI12	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 B30Ah	SCI12	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 B30Bh	SCI12	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 B30Ch	SCI12	I^2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 B30Dh	SCI12	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 B320h	SCI12	Extended Serial Mode Enable Register	ESMER	8	8	2 or 3 PCLKB
0008 B321h	SCI12	Control Register 0	CR0	8	8	2 or 3 PCLKB
0008 B322h	SCI12	Control Register 1	CR1	8	8	2 or 3 PCLKB
0008 B323h	SCI12	Control Register 2	CR2	8	8	2 or 3 PCLKB
0008 B324h	SCI12	Control Register 3	CR3	8	8	2 or 3 PCLKB
0008 B325h	SCI12	Port Control Register	PCR	8	8	2 or 3 PCLKB
0008 B326h	SCI12	Interrupt Control Register	ICR	8	8	2 or 3 PCLKB
0008 B327h	SCI12	Status Register	STR	8	8	2 or 3 PCLKB
0008 B328h	SCI12	Status Clear Register	STCR	8	8	2 or 3 PCLKB
0008 B329h	SCI12	Control Field 0 Data Register	CF0DR	8	8	2 or 3 PCLKB
0008 B32Ah	SCI12	Control Field 0 Compare Enable Register	CF0CR	8	8	2 or 3 PCLKB
0008 B32Bh	SCI12	Control Field 0 Receive Data Register	CF0RR	8	8	2 or 3 PCLKB
0008 B32Ch	SCI12	Primary Control Field 1 Data Register	PCF1DR	8	8	2 or 3 PCLKB
0008 B32Dh	SCI12	Secondary Control Field 1 Data Register	SCF1DR	8	8	2 or 3 PCLKB
0008 B32Eh	SCI12	Control Field 1 Compare Enable Register	CF1CR	8	8	2 or 3 PCLKB
0008 B32Fh	SCI12	Control Field 1 Receive Data Register	CF1RR	8	8	2 or 3 PCLKB
0008 B330h	SCI12	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 B331h	SCI12	Timer Mode Register	TMR	8	8	2 or 3 PCLKB
0008 B332h	SCI12	Timer Prescaler Register	TPRE	8	8	2 or 3 PCLKB
0008 B333h	SCI12	Timer Count Register	TCNT	8	8	2 or 3 PCLKB
0008 C000h	PORT0	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C001h	PORT1	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C002h	PORT2	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C003h	PORT3	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C004h	PORT4	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C005h	PORT5	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Ah	PORTA	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Bh	PORTB	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Ch	PORTC	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Eh	PORTE	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C011h	PORTH	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C012h	PORTJ	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C020h	PORT0	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C021h	PORT1	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C022h	PORT2	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C023h	PORT3	Port Output Data Register	PODR	8	8	2 or 3 PCLKB

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = VREFL0 = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC	–0.3 to +4.6	V
Input voltage	Ports for 5 V tolerant*1	V_{in}	–0.3 to +6.5	V
	Ports P40 to P44, P46, ports PJ6, PJ7	V_{in}	–0.3 to AVCC0 +0.3	V
	Ports other than above	V_{in}	–0.3 to VCC +0.3	V
Reference power supply voltage		VREFH0	–0.3 to AVCC0 +0.3	V
Analog power supply voltage		AVCC0	–0.3 to +4.6	V
Analog input voltage		V_{AN}	–0.3 to AVCC0 + 0.3 (when AN000 to AN004 and AN006 used) –0.3 to VCC + 0.3 (when AN008 to AN015 used)	V
Operating temperature*2		T_{opr}	–40 to +85 –40 to +105	°C
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.
To preclude any malfunctions due to noise interference, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, and between the VREFH0 and VREFL0 pins. Place capacitors of about 0.1 µF as close as possible to every power supply pin and use the shortest and heaviest possible traces. Also, connect capacitors as stabilization capacitance.

Connect the VCL pin to a VSS pin via a 4.7 µF capacitor. The capacitor must be placed close to the pin, refer to section 5.9.1, Connecting VCL Capacitor and Bypass Capacitors.

Do not input signals or an I/O pull-up power supply to ports other than 5-V tolerant ports while the device is not powered. The current injection that results from input of such a signal or I/O pull-up may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.
If input voltage (within the specified range from -0.3 to + 6.5V) is applied to 5-V tolerant ports, it will not cause problems such as damage to the MCU.

Note 1. Ports P16, P17, PA6, and PB0 are 5 V tolerant.
Note 2. The upper limit of operating temperature is 85°C or 105°C, depending on the product. For details, refer to 1.2 List of Products.

Table 5.2 Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Power supply voltages	VCC*1	1.8	—	3.6	V
	VSS	—	0	—	V
Analog power supply voltages	AVCC0*1, *2	1.8	—	3.6	V
	AVSS0	—	0	—	V
	VREFH0	1.8	—	AVCC0	V
	VREFL0	—	0	—	V

Note 1. Supply AVCC0 simultaneously with or after supplying VCC.
Note 2. Refer to section 27.6.10, Voltage Range of Analog Power Supply Pins in the User's Manual: Hardware to determine the AVCC0 voltage.

Table 5.10 DC Characteristics (8)

Conditions: 1.8 V ≤ VCC ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.*2	Max.	Unit	Test Conditions
Analog power supply current	During A/D conversion (at high-speed conversion)	I_{AVCC}	—	0.7	1.2	mA	
	Waiting for A/D conversion (all units)		—	—	0.3	μA	
Reference power supply current	During A/D conversion (at high-speed conversion)	I_{REFH0}	—	25	52	μA	
	Waiting for A/D conversion (all units)		—	—	60	nA	
Temperature sensor*1		I_{TEMP}	—	75	—	μA	
LDV1, 2	Per channel	I_{LVD}	—	0.15	—	μA	

Note 1. Current consumed by the power supply (VCC).
Note 2. When VCC = AVCC0 = 3.3 V.

Table 5.11 DC Characteristics (9)

Conditions: 1.8 V ≤ VCC ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RAM standby voltage	V_{RAM}	1.8	—	—	V	

Table 5.12 DC Characteristics (10)

Conditions: 0 V ≤ VCC ≤ 3.6 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power-on VCC rising gradient	At normal startup*1	SrVCC	0.02	—	20	ms/V	
	During fast startup time*2		0.02	—	2		
	Voltage monitoring 1 reset enabled at startup*3, *4		0.02	—	—		

Note: When powering on AVCC0 and VCC, power them on at the same time or VCC first.
Note 1. When OFS1.(STUPLVD1REN, FASTSTUP) = 11b.
Note 2. When OFS1.(STUPLVD1REN, FASTSTUP) = 10b.
Note 3. When OFS1.STUPLVD1REN = 0.
Note 4. Turn on the power supply voltage according to the normal startup rising gradient because the register settings set by OFS1 are not read in boot mode.

Table 5.13 DC Characteristics (11)

Conditions: 1.8 V ≤ VCC ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C
The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (3.6 V) and lower limit (1.8 V).
When VCC change exceeds VCC ±10%, the allowable voltage change rising/falling gradient dt/dVCC must be met.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Allowable ripple frequency	$f_{r\ (VCC)}$	—	—	10	kHz	Figure 5.6 $V_{r\ (VCC)}$ ≤ VCC × 0.2
		—	—	1	MHz	Figure 5.6 $V_{r\ (VCC)}$ ≤ VCC × 0.08
		—	—	10	MHz	Figure 5.6 $V_{r\ (VCC)}$ ≤ VCC × 0.06
Allowable voltage change rising/ falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

Table 5.17 Output Voltage (1)

Conditions: 2.7 V ≤ VCC ≤ 3.6 V, 2.7 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, T_a = –40 to +10°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Low-level output voltage	All output ports (except for RIIC, ports P40 to P44, P46, ports PJ6, PJ7)		V_{OL}	—	0.6	V	I_{OL} = 3.0 mA
				—	0.4		I_{OL} = 1.5 mA
	Ports P40 to P44, P46, ports PJ6, PJ7			—	0.4		I_{OL} = 0.4 mA
	RIIC pins	Standard mode		—	0.4		I_{OL} = 3.0 mA
		Fast mode		—	0.6		I_{OL} = 6.0 mA
High-level output voltage	All output ports (except for ports P40 to P44, P46, ports PJ6, PJ7)		V_{OH}	VCC – 0.5	—	V	I_{OH} = –2.0 mA
	Ports P40 to P44, P46, ports PJ6, PJ7			AVCC0 – 0.5	—		I_{OH} = –0.1 mA

Table 5.18 Output Voltage (2)

Conditions: 1.8 V ≤ VCC ≤ 2.7 V, 1.8 V ≤ AVCC0 ≤ 2.7 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Max.	Unit	Test Conditions
Low-level output voltage	All output ports (except for ports P40 to P44, P46, ports PJ6, PJ7)	V_{OL}	—	0.6	V	I_{OL} = 1.5 mA
	Ports P40 to P44, P46, ports PJ6, PJ7		—	0.4		I_{OL} = 0.4 mA
High-level output voltage	All output ports (except for ports P40 to P44, P46, ports PJ6, PJ7)	V_{OH}	VCC – 0.5	—	V	I_{OH} = –1.0 mA
	Ports P40 to P44, P46, ports PJ6, PJ7		AVCC0 – 0.5	—		I_{OH} = –0.1 mA

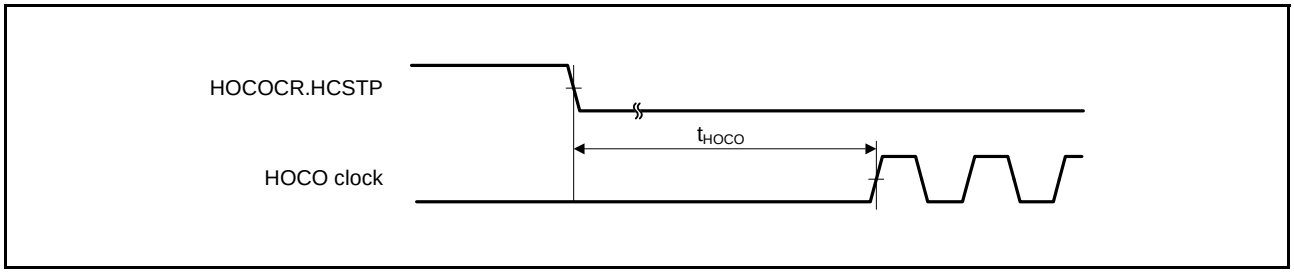


Figure 5.23 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting HOCOCR.HCSTP Bit)

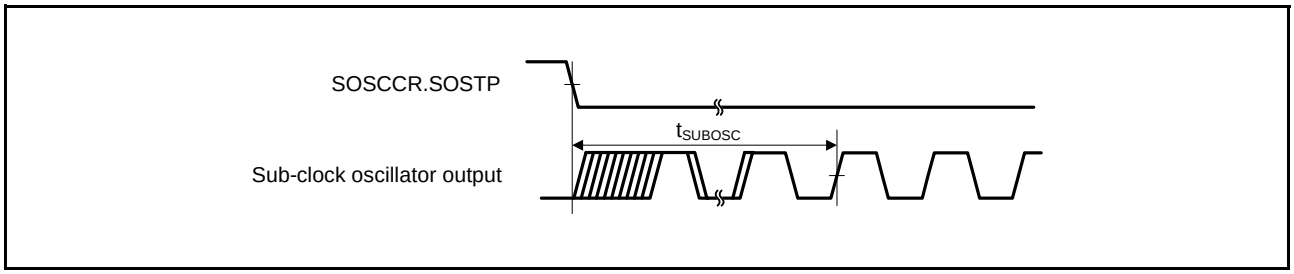


Figure 5.24 Sub-Clock Oscillation Start Timing

Table 5.31 Timing of On-Chip Peripheral Modules (2)

Conditions: 1.8 V ≤ VCC ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C, C = 30 pF

Item				Symbol	Min.	Max.	Unit	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc} *1	Figure 5.39
		Slave			8	4096		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time	Output	2.7 V or above	t_{SPCKr}, t_{SPCKf}	—	10	ns	
			1.8 V or above		—	15		
		Input			—	1	µs	
	Data input setup time	Master	2.7 V or above	t_{SU}	10	—	ns	Figure 5.40 to Figure 5.45
			1.8 V or above		30	—		
		Slave			$25 - t_{Pcyc}$	—		
	Data input hold time	Master	RSPCK set to a division ratio other than PCLKB divided by 2	t_H	t_{Pcyc}	—	ns	
			RSPCK set to PCLKB divided by 2	t_{HF}	0	—		
		Slave		t_H	$20 + 2 \times t_{Pcyc}$	—		
	SSL setup time	Master		t_{LEAD}	$–30 + N^{*2} \times t_{SPcyc}$	—	ns	
		Slave			2	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	$–30 + N^{*3} \times t_{SPcyc}$	—	ns	
		Slave			2	—	t_{Pcyc}	
	Data output delay time	Master	2.7 V or above	t_{OD}	—	14	ns	
			1.8 V or above		—	30		
		Slave	2.7 V or above		—	$3 \times t_{Pcyc} + 65$		
			1.8 V or above		—	$3 \times t_{Pcyc} + 105$		
	Data output hold time	Master	2.7 V or above	t_{OH}	0	—	ns	
			1.8 V or above		–20	—		
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$4 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output	2.7 V or above	t_{Dr}, t_{Df}	—	10	ns	
			1.8 V or above		—	20		
		Input			—	1	µs	
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	20	ns	
		Input			—	1	µs	
	Slave access time		2.7 V or above	t_{SA}	—	6	t_{Pcyc}	Figure 5.44, Figure 5.45
			1.8 V or above		—	7		
	Slave output release time		2.7 V or above	t_{REL}	—	5	t_{Pcyc}	
			1.8 V or above		—	6		

Note 1. t_{Pcyc}: PCLK cycle
Note 2. N: An integer from 1 to 8 that can be set by the RSPI clock delay register (SPCKD)
Note 3. N: An integer from 1 to 8 that can be set by the RSPI slave select negation delay register (SSLND)

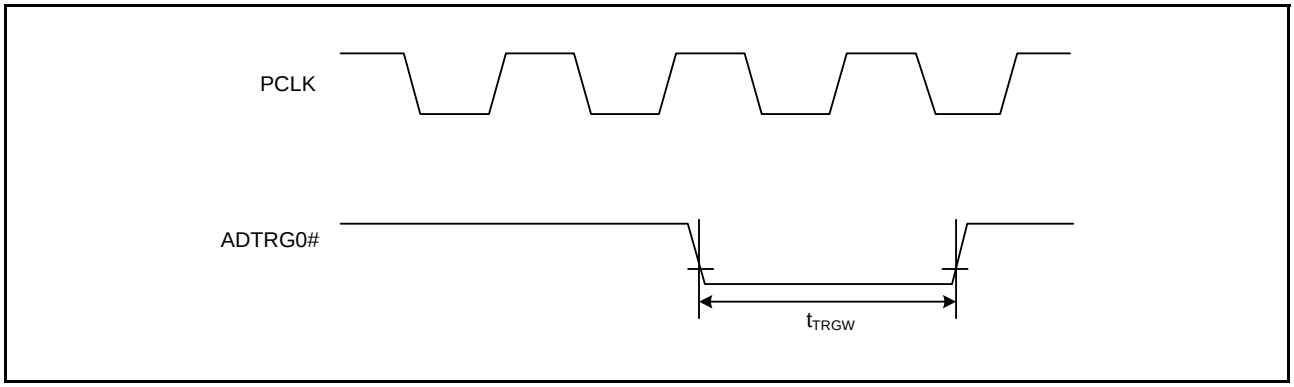


Figure 5.37 A/D Converter External Trigger Input Timing

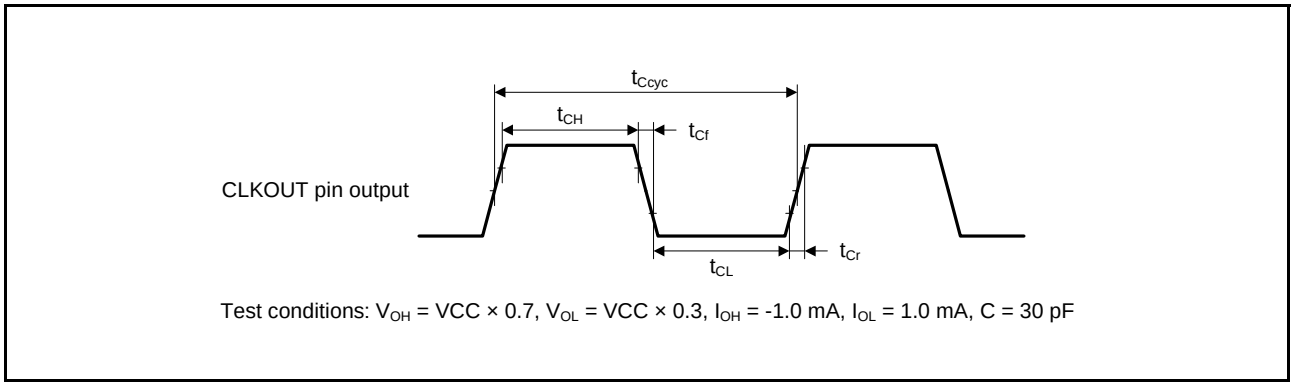


Figure 5.38 CLKOUT Output Timing

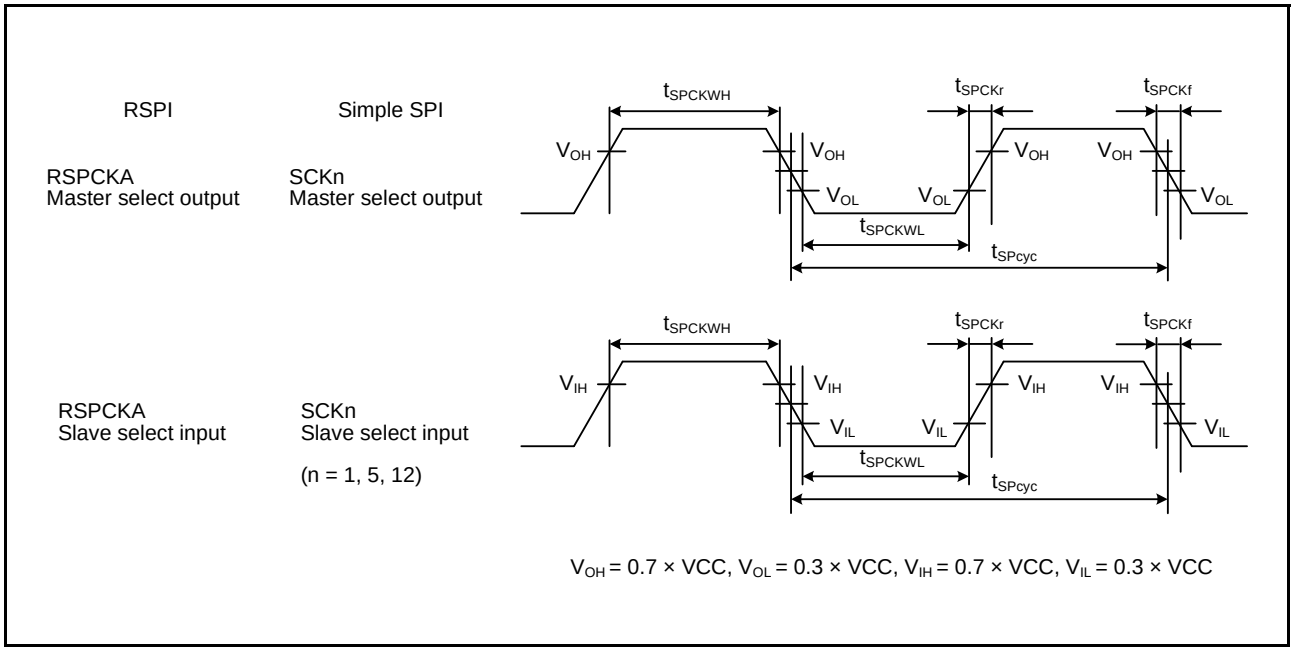


Figure 5.39 RSPI Clock Timing and Simple SPI Clock Timing

Table 5.38 A/D Converter Channel Classification

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN004, AN006	AVCC0 = 1.8 to 3.6 V	Pins AN000 to AN004 and AN006 cannot be used as digital outputs when the A/D converter is in use.
Normal-precision channel	AN008 to AN015		
Internal reference voltage input channel	Internal reference voltage	AVCC0 = 2.0 to 3.6 V	
Temperature sensor input channel	Temperature sensor output	AVCC0 = 2.0 to 3.6 V	

Table 5.39 A/D Internal Reference Voltage Characteristics

Conditions: 2.0 V ≤ VCC ≤ 3.6 V, 2.0 V ≤ AVCC0 ≤ 3.6 V*1, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
Internal reference voltage input channel*2	1.36	1.43	1.50	V	

Note 1. The internal reference voltage cannot be selected for input channels when AVCC0 < 2.0 V.
Note 2. The A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the A/D converter.

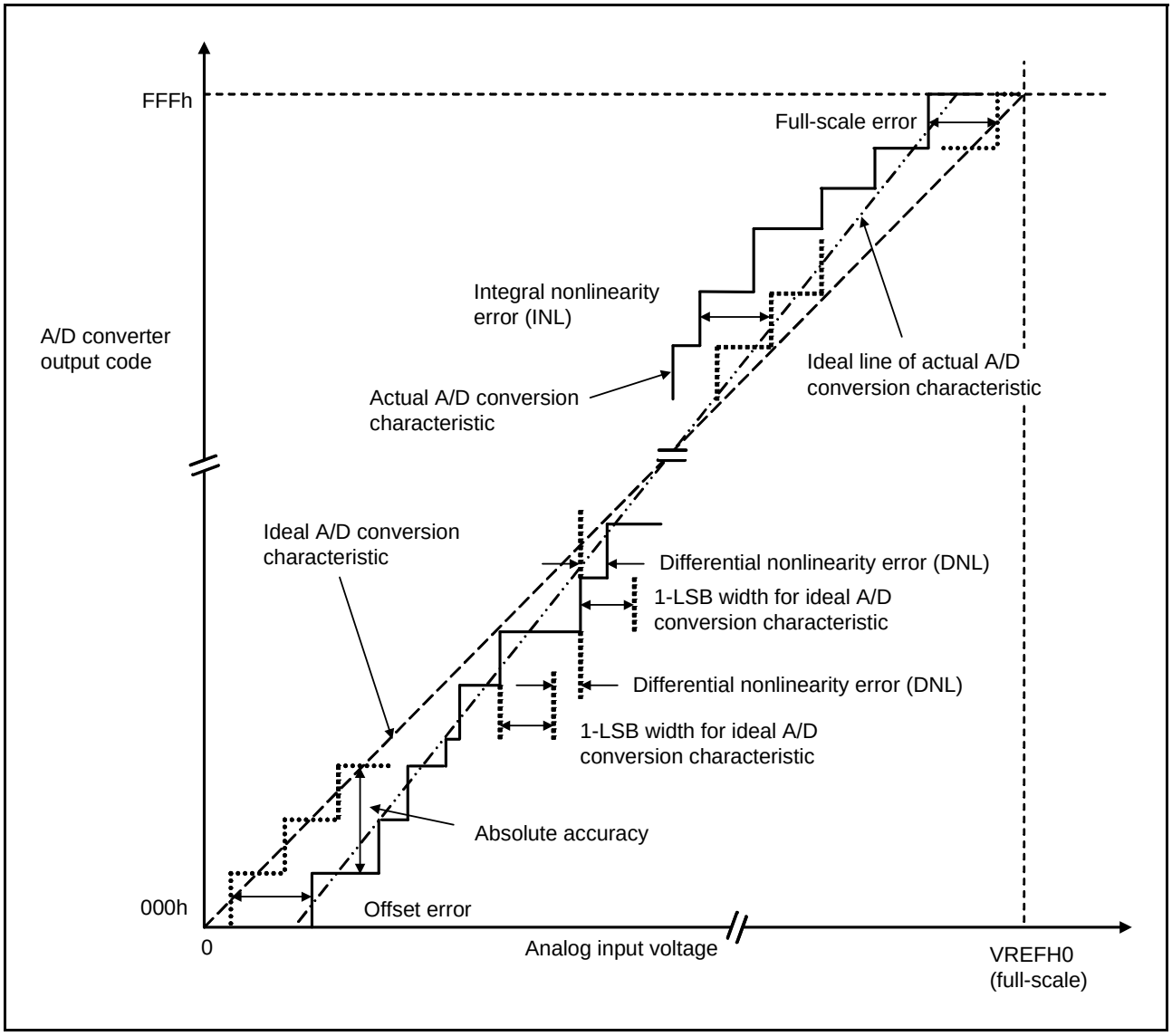


Figure 5.48 Illustration of A/D Converter Characteristic Terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage (VREFH0 = 3.072 V), then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, 1.5 mV, ... are used as analog input voltages.

If analog input voltage is 6 mV, absolute accuracy = ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh though an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actually output code.

Offset error

Offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

5.5 Temperature Sensor Characteristics

Table 5.40 Temperature Sensor Characteristics

Conditions: 2.0 V ≤ VCC ≤ 3.6 V, 2.0 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	—	±1.5	—	°C	2.4 V or above
		—	±2.0	—		Below 2.4 V
Temperature slope	—	—	–3.65	—	mV/°C	
Output voltage (at 25°C)	—	—	1.05	—	V	VCC = 3.3 V
Temperature sensor start time	t_{START}	—	—	5	µs	
Sampling time	—	5	—	—	µs	

5.8 ROM (Flash Memory for Code Storage) Characteristics

Table 5.44 ROM (Flash Memory for Code Storage) Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Reprogramming/erasure cycle*1		N_{PEC}	1000	—	—	Times	
Data hold time	After 1000 times of N_{PEC}	t_{DRP}	20*2, *3	—	—	Year	T_a = +85°C

Note 1. Definition of reprogram/erase cycle: The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 256 times for different addresses in 1-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. Characteristic when using the flash memory programmer and the self-programming library provided from Renesas Electronics.
Note 3. This result is obtained from reliability testing.

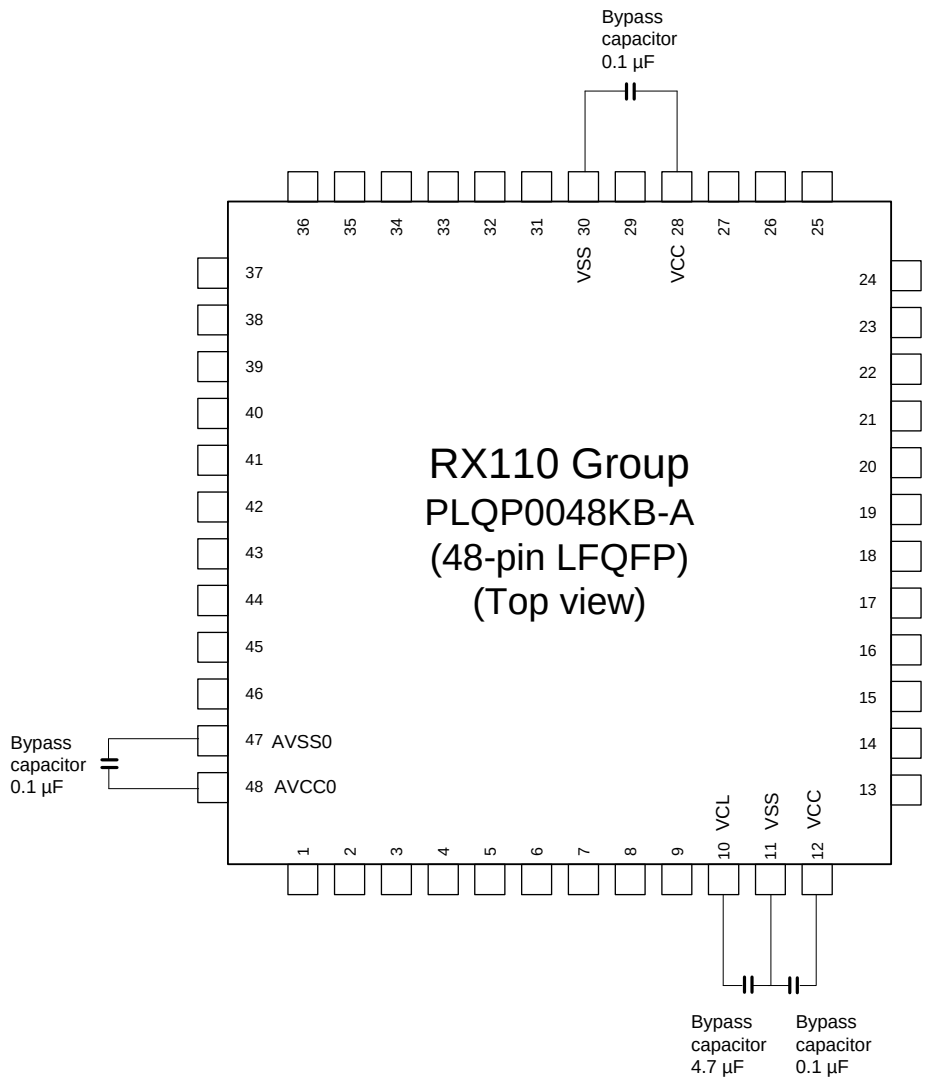
Table 5.45 ROM (Flash Memory for Code Storage) Characteristics (2)

High-speed operating mode Conditions: 2.7 V ≤ VCC ≤ 3.6 V, 2.7 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	4-byte	t_{P4}	—	103	931	—	52	489	µs
Erasure time	1-Kbyte	t_{E1K}	—	8.23	267	—	5.48	214	ms
	128-Kbyte	t_{E128K}	—	203	463	—	20	228	ms
Blank check time	4-byte	t_{BC4}	—	—	48	—	—	15.9	µs
	1-Kbyte	t_{BC1K}	—	—	1.58	—	—	0.127	ms
Erase operation forcible stop time		t_{SED}	—	—	21.6	—	—	12.8	µs
Start-up area switching setting time		t_{SAS}	—	12.6	543	—	6.16	432	ms
Access window time		t_{AWS}	—	12.6	543	—	6.16	432	ms
ROM mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	µs
ROM mode transition wait time 2		t_{MS}	5	—	—	5	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%. Confirm the frequency accuracy of the clock source.



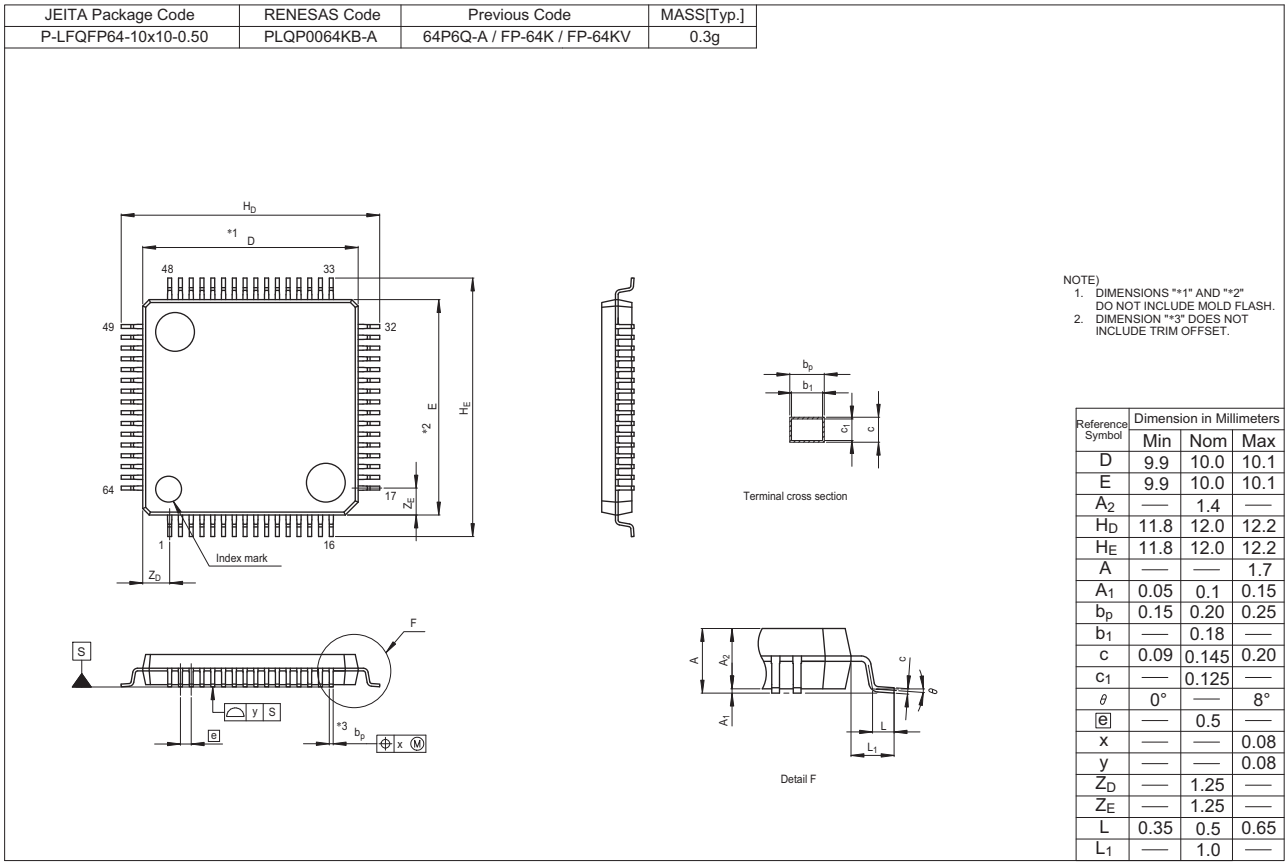
Note. Do not apply the power supply voltage to the VCL pin.
Use a 4.7-µF multilayer ceramic for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

Figure 5.55 Connecting Capacitors (48-pin LFQFP)

Appendix 1. Package Dimensions

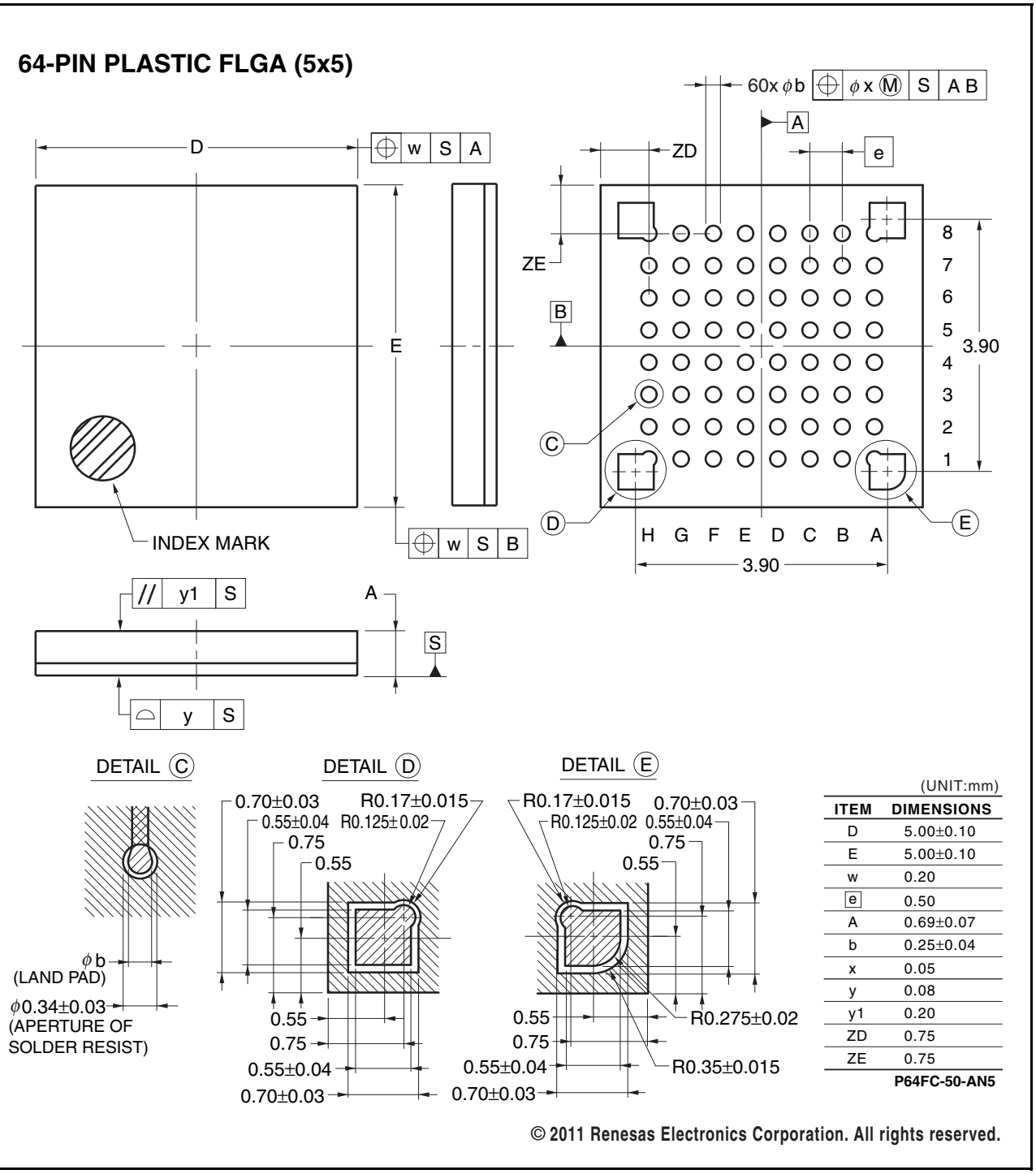
Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure A 64-Pin LFQFP (PLQP0064KB-A)



(UNIT:mm)

ITEM	DIMENSIONS
D	5.00±0.10
E	5.00±0.10
w	0.20
e	0.50
A	0.69±0.07
b	0.25±0.04
x	0.05
y	0.08
y1	0.20
ZD	0.75
ZE	0.75

P64FC-50-AN5

Figure C 64-Pin WFLGA (PWLG0064KA-A)

REVISION HISTORY	RX110 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.51	Jul 03, 2013	—	First edition, issued
1.00	Dec , 2013	1. Overview	
		6, 7	Table 1.3 List of Products changed
		8	Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type changed
		9	Figure 1.2 Block Diagram changed
		4. I/O Registers	
		44	Table 4.1 List of I/O Registers (Address Order) changed
		5. Electrical Characteristics	
		45 to 91	Changed

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.