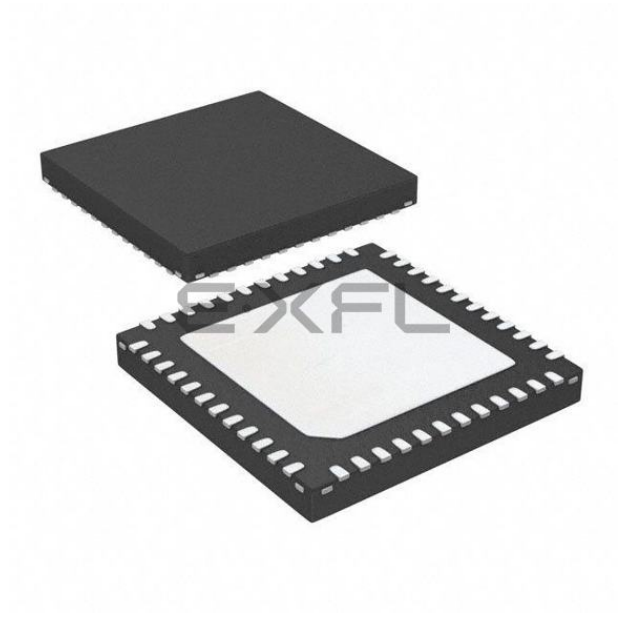

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-WFQFN Exposed Pad
Supplier Device Package	48-HWQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f51104adne-u0

Table 1.1 Outline of Specifications (3/3)

Classification	Module/Function	Description
Data operation circuit (DOC)		Comparison, addition, and subtraction of 16-bit data
Unique ID		32-byte ID code for the MCU
Power supply voltages/Operating frequencies		VCC = 1.8 to 2.4 V: 8 MHz, VCC = 2.4 to 2.7 V: 16 MHz, VCC = 2.7 to 3.6 V: 32 MHz
Supply current		3.2 mA at 32 MHz (typ.)
Operating temperatures		D version: –40 to +85°C, G version: –40 to +105°C
Packages		64-pin LFQFP (PLQP0064KB-A) 10 × 10 mm, 0.5 mm pitch 64-pin LQFP (PLQP0064GA-A) 14 × 14 mm, 0.8 mm pitch 64-pin WFLGA (PWLG0064KA-A) 5 × 5 mm, 0.5 mm pitch 48-pin LFQFP (PLQP0048KB-A) 7 × 7 mm, 0.5 mm pitch 48-pin HWQFN (PWQN0048KB-A) 7 × 7 mm, 0.5 mm pitch 40-pin HWQFN (PWQN0040KC-A) 6 × 6 mm, 0.5 mm pitch 36-pin WFLGA (PWLG0036KA-A) 4 × 4 mm, 0.5 mm pitch
On-chip debugging system		E1 emulator (FINE interface)

Table 1.2 Comparison of Functions for Different Packages

Module/Functions		RX110 Group			
		64 Pins	48 Pins	40 Pins	36 Pins
Interrupts	External interrupts	NMI, IRQ0 to IRQ7			
DMA	Data transfer controller	Supported			
Timers	Multi-function timer pulse unit 2	4 channels (MTU0 to MTU2, MTU5)			
	Compare match timer	2 channels × 1 unit			
	Realtime clock	Supported		Not supported	
	Independent watchdog timer	Supported			
Communication functions	Serial communications interfaces [simple I2C, simple SPI]	2 channels (SCI1, SCI5)			
	Serial communications interface [simple I2C, simple SPI]	1 channel (SCI12)			
	I2C bus interface	1 channel			
	Serial peripheral interface	1 channel	1 channel (SSLA1 and SSLA3 are not supported)		1 channel (SSLA1 to SSLA3 are not supported)
12-bit A/D converter (including high-precision channels)		14 channels (6 channels)	10 channels (4 channels)	8 channels (3 channels)	7 channels (2 channels)
Temperature sensor		Supported			
CRC calculator		Supported			
Packages		64-pin LFQFP 64-pin LQFP 64-pin WFLGA	48-pin LFQFP 48-pin HWQFN	40-pin HWQFN	36-pin WFLGA

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products (1/2)

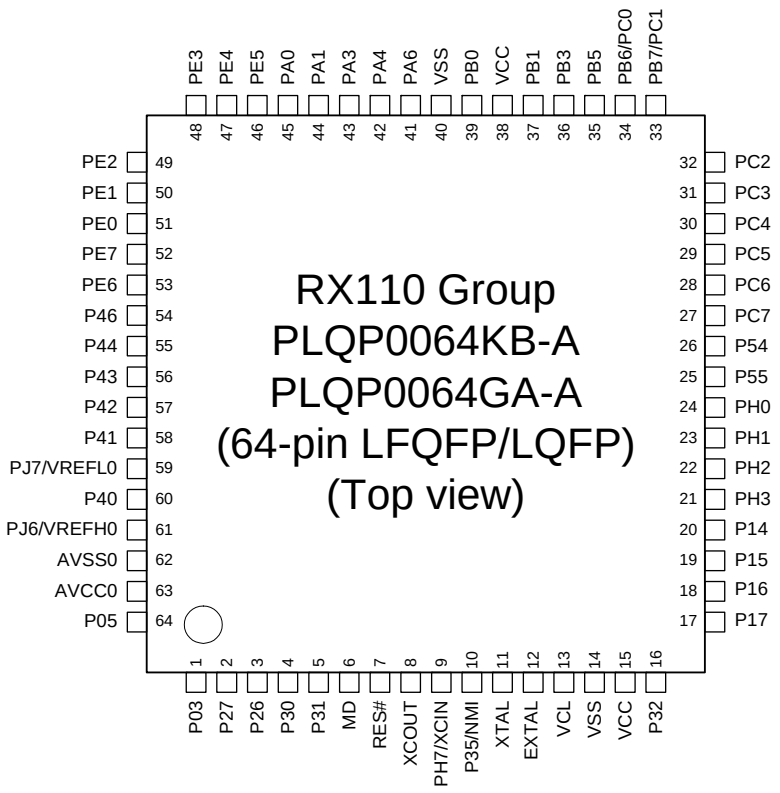
Group	Part No.	Orderable Part No.	Package	ROM Capacity	RAM Capacity	Maximum Operating Frequency	Operating Temperature
RX110	R5F51105AGFM	R5F51105AGFM#30	PLQP0064KB-A	128 Kbytes	16 Kbytes	32 MHz	–40 to +105°C
	R5F51105AGFK	R5F51105AGFK#30	PLQP0064GA-A				
	R5F51105AGFL	R5F51105AGFL#30	PLQP0048KB-A				
	R5F51105AGNE	R5F51105AGNE#U0	PWQN0048KB-A				
	R5F51104AGFM	R5F51104AGFM#30	PLQP0064KB-A	96 Kbytes			
	R5F51104AGFK	R5F51104AGFK#30	PLQP0064GA-A				
	R5F51104AGFL	R5F51104AGFL#30	PLQP0048KB-A				
	R5F51104AGNE	R5F51104AGNE#U0	PWQN0048KB-A				
	R5F51103AGFM	R5F51103AGFM#30	PLQP0064KB-A	64 Kbytes	10 Kbytes		
	R5F51103AGFK	R5F51103AGFK#30	PLQP0064GA-A				
	R5F51103AGFL	R5F51103AGFL#30	PLQP0048KB-A				
	R5F51103AGNE	R5F51103AGNE#U0	PWQN0048KB-A				
	R5F51103AGNF	R5F51103AGNF#U0	PWQN0040KC-A				
	R5F51101AGFM	R5F51101AGFM#30	PLQP0064KB-A	32 Kbytes			
	R5F51101AGFK	R5F51101AGFK#30	PLQP0064GA-A				
	R5F51101AGFL	R5F51101AGFL#30	PLQP0048KB-A				
	R5F51101AGNE	R5F51101AGNE#U0	PWQN0048KB-A				
	R5F51101AGNF	R5F51101AGNF#U0	PWQN0040KC-A				
	R5F5110JAGFM	R5F5110JAGFM#30	PLQP0064KB-A	16 Kbytes	8 Kbytes		
	R5F5110JAGFK	R5F5110JAGFK#30	PLQP0064GA-A				
	R5F5110JAGFL	R5F5110JAGFL#30	PLQP0048KB-A				
	R5F5110JAGNE	R5F5110JAGNE#U0	PWQN0048KB-A				
	R5F5110JAGNF	R5F5110JAGNF#U0	PWQN0040KC-A				
	R5F5110HAGNF	R5F5110HAGNF#U0	PWQN0040KC-A	8 Kbytes			

Table 1.4 Pin Functions (2/3)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIe)	• Simple I2C mode		
	SSCL1, SSCL5	I/O	Input/output pins for the I2C clock.
	SSDA1, SSDA5	I/O	Input/output pins for the I2C data.
	• Simple SPI mode		
	SCK1, SCK5	I/O	Input/output pins for the clock.
	SMISO1, SMISO5	I/O	Input/output pins for slave transmit data.
	SMOSI1, SMOSI5	I/O	Input/output pins for master transmit data.
	SS1#, SS5#	Input	Chip-select input pins.
Serial communications interface (SCIf)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock.
	RXD12	Input	Input pin for receiving data.
	TXD12	Output	Output pin for transmitting data.
	CTS12#	Input	Input pin for controlling the start of transmission and reception.
	RTS12#	Output	Output pin for controlling the start of transmission and reception.
	• Simple I2C mode		
	SSCL12	I/O	Input/output pin for the I2C clock.
	SSDA12	I/O	Input/output pin for the I2C data.
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock.
	SMISO12	I/O	Input/output pin for slave transmit data.
	SMOSI12	I/O	Input/output pin for master transmit data.
	SS12#	Input	Chip-select input pin.
	• Extended serial mode		
	RXDX12	Input	Input pin for data reception by SCIf.
	TXDX12	Output	Output pin for data transmission by SCIf.
	SIOX12	I/O	Input/output pin for data reception or transmission by SCIf.
I2C bus interface	SCL0	I/O	Input/output pin for I2C bus interface clocks. Bus can be directly driven by the N-channel open drain output.
	SDA0	I/O	Input/output pin for I2C bus interface data. Bus can be directly driven by the N-channel open drain output.
Serial peripheral interface	RSPCKA	I/O	Input/output pin for the RSPI clock.
	MOSIA	I/O	Input/output pin for transmitting data from the RSPI master.
	MISOA	I/O	Input/output pin for transmitting data from the RSPI slave.
	SSLA0	I/O	Input/output pin to select the slave for the RSPI.
	SSLA1 to SSLA3	Output	Output pins to select the slave for the RSPI.
12-bit A/D converter	AN000 to AN004, AN006, AN008 to AN015	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0#	Input	Input pin for the external trigger signals that start the A/D conversion.
I/O ports	P03, P05	I/O	2-bit input/output pins.
	P14 to P17	I/O	4-bit input/output pins.
	P26, P27	I/O	2-bit input/output pins.
	P30 to P32, P35	I/O	4-bit input/output pins (P35 input pin).
	P40 to P44, P46	I/O	6-bit input/output pins.
	P54, P55	I/O	2-bit input/output pins.
	PA0, PA1, PA3, PA4, PA6	I/O	5-bit input/output pins.
	PB0, PB1, PB3, PB5 to PB7	I/O	6-bit input/output pins.

1.5 Pin Assignments

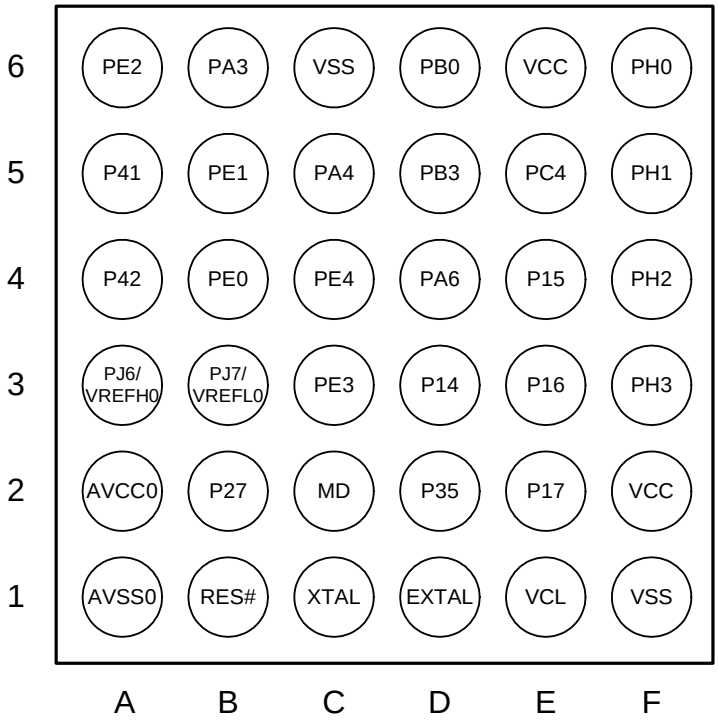
Figure 1.3 to Figure 1.7 show the pin assignments. Table 1.5 to Table 1.9 show the lists of pins and pin functions.



Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (64-Pin LFQFP/LQFP)”.

Figure 1.3 Pin Assignments of the 64-Pin LFQFP/LQFP

RX110 Group
PWLG0036KA-A
(36-pin WFLGA)
(Upper perspective view)



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (36-Pin WFLGA)”.
Note: For the position of A1 pin in the package, see “Package Dimensions”.

Figure 1.7 Pin Assignments of the 36-Pin WFLGA

Table 1.5 List of Pins and Pin Functions (64-Pin LFQFP/LQFP) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, RTC)	Communication (SCIe, SCIf, RSPI, RIIC)	Others
1		P03			
2		P27	MTIOC2B	SCK1/SCK12	IRQ3/CMPA2/ CACREF/ADTRG0#
3		P26	MTIOC2A	TXD1/SMOSI1/SSDA1	
4		P30		RXD1/SMISO1/SSCL1	IRQ0
5		P31		CTS1#/RTS1#/SS1#	IRQ1
6	MD				FINED
7	RES#				
8	XCOUT				
9	XCIN	PH7			
10		P35			NMI
11	XTAL				
12	EXTAL				
13	VCL				
14	VSS				
15	VCC				
16		P32	MTIOC0C/RTCOUT		IRQ2
17		P17	MTIOC0C	SCK1/MISOA/SDA0/RXD12/RXDX12/ SMISO12/SSCL12	IRQ7
18		P16	RTCOUT	TXD1/SMOSI1/SSDA1/MOSIA/SCL0	IRQ6/ADTRG0#
19		P15	MTIOC0B/MTCLKB	RXD1/SMISO1/SSCL1/RSPCKA	IRQ5/CLKOUT
20		P14	MTIOC0A/MTCLKA	CTS1#/RTS1#/SS1#/SSLA0/TXD12/ TXDX12/SIOX12/SMOSI12/SSDA12	IRQ4
21		PH3	MTIOC1A		
22		PH2			IRQ1
23		PH1			IRQ0
24		PH0	MTIOC1B		CACREF
25		P55			
26		P54			
27		PC7	MTCLKB	TXD1/SMOSI1/SSDA1/MISOA	CACREF
28		PC6	MTCLKA	RXD1/SMISO1/SSCL1/MOSIA	
29		PC5	MTCLKD	SCK1/RSPCKA	
30		PC4	MTCLKC	SCK5/SSLA0	IRQ2/CLKOUT
31		PC3		TXD5/SMOSI5/SSDA5	
32		PC2		RXD5/SMISO5/SSCL5/SSLA3	
33		PB7/PC1			
34		PB6/PC0			
35		PB5	MTIOC2A/MTIOC1B		
36		PB3	MTIOC0A		
37		PB1	MTIOC0C		IRQ4
38	VCC				
39		PB0	MTIC5W/MTIOC0C/ RTCOUT	SCL0/RSPCKA	IRQ2/ADTRG0#
40	VSS				
41		PA6	MTIC5V/MTCLKB/MTIOC2A	CTS5#/RTS5#/SS5#/SDA0/MOSIA	IRQ3
42		PA4	MTIC5U/MTCLKA/MTIOC2B	TXD5/SMOSI5/SSDA5/SSLA0	IRQ5
43		PA3	MTIOC0D/MTCLKD/ MTIOC1B	RXD5/SMISO5/SSCL5/MISOA	IRQ6
44		PA1	MTIOC0B/MTCLKC/ RTCOUT	SCK5/SSLA2	

Table 1.8 List of Pins and Pin Functions (40-Pin HWQFN)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, RTC)	Communication (SCIe, SCIf, RSPI, RIIC)	Others
1		P27	MTIOC2B	SCK1/SCK12	IRQ3/CMPA2/ CACREF/ADTRG0#
2		P26	MTIOC2A	TXD1/SMOSI1/SSDA1	
3	MD				FINED
4	RES#				
5		P35			NMI
6	XTAL				
7	EXTAL				
8	VCL				
9	VSS				
10	VCC				
11		P32	MTIOC0C		IRQ2
12		P17	MTIOC0C	SCK1/MISOA/SDA0/RXD12/RXDX12/ SMISO12/SSCL12	IRQ7
13		P16		TXD1/SMOSI1/SSDA1/SCL0/MOSIA	IRQ6/ADTRG0#
14		P15	MTIOC0B/MTCLKB	RXD1/SMISO1/SSCL1/RSPCKA	IRQ5/CLKOUT
15		P14	MTIOC0A/MTCLKA	CTS1#/RTS1#/SS1#/SSLA0/TXD12/ TXDX12/SIOX12/SMOSI12/SSDA12	IRQ4
16		PH3	MTIOC1A		
17		PH2			IRQ1
18		PH1			IRQ0
19		PH0	MTIOC1B		CACREF
20		PC4	MTCLKC	SCK5/SSLA0	IRQ2/CLKOUT
21		PB3	MTIOC0A		
22	VCC				
23		PB0	MTIOC0C/MTIC5W	SCL0/RSPCKA	IRQ2/ADTRG0#
24	VSS				
25		PA6	MTIOC2A/MTIC5V/MTCLKB	CTS5#/RTS5#/SS5#/SDA0/MOSIA	IRQ3
26		PA4	MTIOC2B/MTIC5U/MTCLKA	TXD5/SMOSI5/SSDA5/SSLA0	IRQ5
27		PA3	MTIOC0D/MTIOC1B/ MTCLKD	RXD5/SMISO5/SSCL5/MISOA	IRQ6
28		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	
29		PE4	MTIOC1A	MOSIA	IRQ4/AN012
30		PE3	MTIOC0A/MTIOC1B	CTS12#/RTS12#/SS12#/RSPCKA	IRQ3/AN011
31		PE2		RXD12/RXDX12/SMISO12/SSCL12	IRQ7/AN010
32		PE1		TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12	IRQ1/AN009
33		PE0	MTIOC2A	SCK12	IRQ0/AN008
34		P46*1			AN006
35		P42*1			AN002
36		P41*1			AN001
37	VREFL0	PJ7*1			
38	VREFH0	PJ6*1			
39	AVSS0				
40	AVCC0				

Note 1. The power source of the I/O buffer for these pins is AVCC0.

Table 4.1 List of I/O Registers (Address Order) (2/13)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 702Dh	ICU	Interrupt Request Register 045	IR045	8	8	2 ICLK
0008 702Eh	ICU	Interrupt Request Register 046	IR046	8	8	2 ICLK
0008 702Fh	ICU	Interrupt Request Register 047	IR047	8	8	2 ICLK
0008 7039h	ICU	Interrupt Request Register 057	IR057	8	8	2 ICLK
0008 703Fh	ICU	Interrupt Request Register 063	IR063	8	8	2 ICLK
0008 7040h	ICU	Interrupt Request Register 064	IR064	8	8	2 ICLK
0008 7041h	ICU	Interrupt Request Register 065	IR065	8	8	2 ICLK
0008 7042h	ICU	Interrupt Request Register 066	IR066	8	8	2 ICLK
0008 7043h	ICU	Interrupt Request Register 067	IR067	8	8	2 ICLK
0008 7044h	ICU	Interrupt Request Register 068	IR068	8	8	2 ICLK
0008 7045h	ICU	Interrupt Request Register 069	IR069	8	8	2 ICLK
0008 7046h	ICU	Interrupt Request Register 070	IR070	8	8	2 ICLK
0008 7047h	ICU	Interrupt Request Register 071	IR071	8	8	2 ICLK
0008 7058h	ICU	Interrupt Request Register 088	IR088	8	8	2 ICLK
0008 7059h	ICU	Interrupt Request Register 089	IR089	8	8	2 ICLK
0008 705Ah	ICU	Interrupt Request Register 090	IR090	8	8	2 ICLK
0008 705Ch	ICU	Interrupt Request Register 092	IR092	8	8	2 ICLK
0008 705Dh	ICU	Interrupt Request Register 093	IR093	8	8	2 ICLK
0008 7066h	ICU	Interrupt Request Register 102	IR102	8	8	2 ICLK
0008 7067h	ICU	Interrupt Request Register 103	IR103	8	8	2 ICLK
0008 706Ah	ICU	Interrupt Request Register 106	IR106	8	8	2 ICLK
0008 7072h	ICU	Interrupt Request Register 114	IR114	8	8	2 ICLK
0008 7073h	ICU	Interrupt Request Register 115	IR115	8	8	2 ICLK
0008 7074h	ICU	Interrupt Request Register 116	IR116	8	8	2 ICLK
0008 7075h	ICU	Interrupt Request Register 117	IR117	8	8	2 ICLK
0008 7076h	ICU	Interrupt Request Register 118	IR118	8	8	2 ICLK
0008 7077h	ICU	Interrupt Request Register 119	IR119	8	8	2 ICLK
0008 7078h	ICU	Interrupt Request Register 120	IR120	8	8	2 ICLK
0008 7079h	ICU	Interrupt Request Register 121	IR121	8	8	2 ICLK
0008 707Ah	ICU	Interrupt Request Register 122	IR122	8	8	2 ICLK
0008 707Bh	ICU	Interrupt Request Register 123	IR123	8	8	2 ICLK
0008 707Ch	ICU	Interrupt Request Register 124	IR124	8	8	2 ICLK
0008 707Dh	ICU	Interrupt Request Register 125	IR125	8	8	2 ICLK
0008 707Eh	ICU	Interrupt Request Register 126	IR126	8	8	2 ICLK
0008 707Fh	ICU	Interrupt Request Register 127	IR127	8	8	2 ICLK
0008 7080h	ICU	Interrupt Request Register 128	IR128	8	8	2 ICLK
0008 7081h	ICU	Interrupt Request Register 129	IR129	8	8	2 ICLK
0008 7082h	ICU	Interrupt Request Register 130	IR130	8	8	2 ICLK
0008 7083h	ICU	Interrupt Request Register 131	IR131	8	8	2 ICLK
0008 7084h	ICU	Interrupt Request Register 132	IR132	8	8	2 ICLK
0008 7085h	ICU	Interrupt Request Register 133	IR133	8	8	2 ICLK
0008 7086h	ICU	Interrupt Request Register 134	IR134	8	8	2 ICLK
0008 7087h	ICU	Interrupt Request Register 135	IR135	8	8	2 ICLK
0008 7088h	ICU	Interrupt Request Register 136	IR136	8	8	2 ICLK
0008 7089h	ICU	Interrupt Request Register 137	IR137	8	8	2 ICLK
0008 708Ah	ICU	Interrupt Request Register 138	IR138	8	8	2 ICLK
0008 708Bh	ICU	Interrupt Request Register 139	IR139	8	8	2 ICLK
0008 708Ch	ICU	Interrupt Request Register 140	IR140	8	8	2 ICLK
0008 708Dh	ICU	Interrupt Request Register 141	IR141	8	8	2 ICLK
0008 70AAh	ICU	Interrupt Request Register 170	IR170	8	8	2 ICLK
0008 70ABh	ICU	Interrupt Request Register 171	IR171	8	8	2 ICLK
0008 70DAh	ICU	Interrupt Request Register 218	IR218	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (4/13)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 71F8h	ICU	DTC Activation Enable Register 248	DTCER248	8	8	2 ICLK
0008 7202h	ICU	Interrupt Request Enable Register 02	IER02	8	8	2 ICLK
0008 7203h	ICU	Interrupt Request Enable Register 03	IER03	8	8	2 ICLK
0008 7204h	ICU	Interrupt Request Enable Register 04	IER04	8	8	2 ICLK
0008 7205h	ICU	Interrupt Request Enable Register 05	IER05	8	8	2 ICLK
0008 7207h	ICU	Interrupt Request Enable Register 07	IER07	8	8	2 ICLK
0008 7208h	ICU	Interrupt Request Enable Register 08	IER08	8	8	2 ICLK
0008 720Bh	ICU	Interrupt Request Enable Register 0B	IER0B	8	8	2 ICLK
0008 720Ch	ICU	Interrupt Request Enable Register 0C	IER0C	8	8	2 ICLK
0008 720Eh	ICU	Interrupt Request Enable Register 0E	IER0E	8	8	2 ICLK
0008 720Fh	ICU	Interrupt Request Enable Register 0F	IER0F	8	8	2 ICLK
0008 7210h	ICU	Interrupt Request Enable Register 10	IER10	8	8	2 ICLK
0008 7211h	ICU	Interrupt Request Enable Register 11	IER11	8	8	2 ICLK
0008 721Bh	ICU	Interrupt Request Enable Register 1B	IER1B	8	8	2 ICLK
0008 721Ch	ICU	Interrupt Request Enable Register 1C	IER1C	8	8	2 ICLK
0008 721Dh	ICU	Interrupt Request Enable Register 1D	IER1D	8	8	2 ICLK
0008 721Eh	ICU	Interrupt Request Enable Register 1E	IER1E	8	8	2 ICLK
0008 721Fh	ICU	Interrupt Request Enable Register 1F	IER1F	8	8	2 ICLK
0008 72E0h	ICU	Software Interrupt Activation Register	SWINTR	8	8	2 ICLK
0008 72F0h	ICU	Fast Interrupt Set Register	FIR	16	16	2 ICLK
0008 7300h	ICU	Interrupt Source Priority Register 000	IPR000	8	8	2 ICLK
0008 7303h	ICU	Interrupt Source Priority Register 003	IPR003	8	8	2 ICLK
0008 7304h	ICU	Interrupt Source Priority Register 004	IPR004	8	8	2 ICLK
0008 7305h	ICU	Interrupt Source Priority Register 005	IPR005	8	8	2 ICLK
0008 7320h	ICU	Interrupt Source Priority Register 032	IPR032	8	8	2 ICLK
0008 7321h	ICU	Interrupt Source Priority Register 033	IPR033	8	8	2 ICLK
0008 7322h	ICU	Interrupt Source Priority Register 034	IPR034	8	8	2 ICLK
0008 732Ch	ICU	Interrupt Source Priority Register 044	IPR044	8	8	2 ICLK
0008 7339h	ICU	Interrupt Source Priority Register 057	IPR057	8	8	2 ICLK
0008 733Fh	ICU	Interrupt Source Priority Register 063	IPR063	8	8	2 ICLK
0008 7340h	ICU	Interrupt Source Priority Register 064	IPR064	8	8	2 ICLK
0008 7341h	ICU	Interrupt Source Priority Register 065	IPR065	8	8	2 ICLK
0008 7342h	ICU	Interrupt Source Priority Register 066	IPR066	8	8	2 ICLK
0008 7343h	ICU	Interrupt Source Priority Register 067	IPR067	8	8	2 ICLK
0008 7344h	ICU	Interrupt Source Priority Register 068	IPR068	8	8	2 ICLK
0008 7345h	ICU	Interrupt Source Priority Register 069	IPR069	8	8	2 ICLK
0008 7346h	ICU	Interrupt Source Priority Register 070	IPR070	8	8	2 ICLK
0008 7347h	ICU	Interrupt Source Priority Register 071	IPR071	8	8	2 ICLK
0008 7358h	ICU	Interrupt Source Priority Register 088	IPR088	8	8	2 ICLK
0008 7359h	ICU	Interrupt Source Priority Register 089	IPR089	8	8	2 ICLK
0008 735Ch	ICU	Interrupt Source Priority Register 092	IPR092	8	8	2 ICLK
0008 735Dh	ICU	Interrupt Source Priority Register 093	IPR093	8	8	2 ICLK
0008 7366h	ICU	Interrupt Source Priority Register 102	IPR102	8	8	2 ICLK
0008 7367h	ICU	Interrupt Source Priority Register 103	IPR103	8	8	2 ICLK
0008 7372h	ICU	Interrupt Source Priority Register 114	IPR114	8	8	2 ICLK
0008 7376h	ICU	Interrupt Source Priority Register 118	IPR118	8	8	2 ICLK
0008 7379h	ICU	Interrupt Source Priority Register 121	IPR121	8	8	2 ICLK
0008 737Bh	ICU	Interrupt Source Priority Register 123	IPR123	8	8	2 ICLK
0008 737Dh	ICU	Interrupt Source Priority Register 125	IPR125	8	8	2 ICLK
0008 737Fh	ICU	Interrupt Source Priority Register 127	IPR127	8	8	2 ICLK
0008 738Bh	ICU	Interrupt Source Priority Register 139	IPR139	8	8	2 ICLK
0008 73DAh	ICU	Interrupt Source Priority Register 218	IPR218	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (6/13)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 830Ah	RIIC0	Timeout Internal Counter L	TMOCNTL	8	8	2 or 3 PCLKB
0008 830Bh	RIIC0	Slave Address Register U0	SARU0	8	8	2 or 3 PCLKB
0008 830Bh	RIIC0	Timeout Internal Counter U	TMOCNTU	8	8 *1	2 or 3 PCLKB
0008 830Ch	RIIC0	Slave Address Register L1	SARL1	8	8	2 or 3 PCLKB
0008 830Dh	RIIC0	Slave Address Register U1	SARU1	8	8	2 or 3 PCLKB
0008 830Eh	RIIC0	Slave Address Register L2	SARL2	8	8	2 or 3 PCLKB
0008 830Fh	RIIC0	Slave Address Register U2	SARU2	8	8	2 or 3 PCLKB
0008 8310h	RIIC0	I^2C Bus Bit Rate Low-Level Register	ICBRL	8	8	2 or 3 PCLKB
0008 8311h	RIIC0	I^2C Bus Bit Rate High-Level Register	ICBRH	8	8	2 or 3 PCLKB
0008 8312h	RIIC0	I^2C Bus Transmit Data Register	ICDRT	8	8	2 or 3 PCLKB
0008 8313h	RIIC0	I^2C Bus Receive Data Register	ICDRR	8	8	2 or 3 PCLKB
0008 8380h	RSPI0	RSPI Control Register	SPCR	8	8	2 or 3 PCLKB
0008 8381h	RSPI0	RSPI Slave Select Polarity Register	SSLP	8	8	2 or 3 PCLKB
0008 8382h	RSPI0	RSPI Pin Control Register	SPPCR	8	8	2 or 3 PCLKB
0008 8383h	RSPI0	RSPI Status Register	SPSR	8	8	2 or 3 PCLKB
0008 8384h	RSPI0	RSPI Data Register	SPDR	32	16, 32	2 or 3 PCLKB/2ICLK
0008 8388h	RSPI0	RSPI Sequence Control Register	SPSCR	8	8	2 or 3 PCLKB
0008 8389h	RSPI0	RSPI Sequence Status Register	SPSSR	8	8	2 or 3 PCLKB
0008 838Ah	RSPI0	RSPI Bit Rate Register	SPBR	8	8	2 or 3 PCLKB
0008 838Bh	RSPI0	RSPI Data Control Register	SPDCR	8	8	2 or 3 PCLKB
0008 838Ch	RSPI0	RSPI Clock Delay Register	SPCKD	8	8	2 or 3 PCLKB
0008 838Dh	RSPI0	RSPI Slave Select Negation Delay Register	SSLND	8	8	2 or 3 PCLKB
0008 838Eh	RSPI0	RSPI Next-Access Delay Register	SPND	8	8	2 or 3 PCLKB
0008 838Fh	RSPI0	RSPI Control Register 2	SPCR2	8	8	2 or 3 PCLKB
0008 8390h	RSPI0	RSPI Command Register 0	SPCMD0	16	16	2 or 3 PCLKB
0008 8392h	RSPI0	RSPI Command Register 1	SPCMD1	16	16	2 or 3 PCLKB
0008 8394h	RSPI0	RSPI Command Register 2	SPCMD2	16	16	2 or 3 PCLKB
0008 8396h	RSPI0	RSPI Command Register 3	SPCMD3	16	16	2 or 3 PCLKB
0008 8398h	RSPI0	RSPI Command Register 4	SPCMD4	16	16	2 or 3 PCLKB
0008 839Ah	RSPI0	RSPI Command Register 5	SPCMD5	16	16	2 or 3 PCLKB
0008 839Ch	RSPI0	RSPI Command Register 6	SPCMD6	16	16	2 or 3 PCLKB
0008 839Eh	RSPI0	RSPI Command Register 7	SPCMD7	16	16	2 or 3 PCLKB
0008 8680h	MTU	Timer Start Register	TSTR	8	8, 16	2 or 3 PCLKB
0008 8681h	MTU	Timer Synchronous Register	TSYR	8	8, 16	2 or 3 PCLKB
0008 8690h	MTU0	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB
0008 8691h	MTU1	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB
0008 8692h	MTU2	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB
0008 8695h	MTU5	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB
0008 8700h	MTU0	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8701h	MTU0	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB
0008 8702h	MTU0	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKB
0008 8703h	MTU0	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKB
0008 8704h	MTU0	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 8705h	MTU0	Timer Status Register	TSR	8	8	2 or 3 PCLKB
0008 8706h	MTU0	Timer Counter	TCNT	16	16	2 or 3 PCLKB
0008 8708h	MTU0	Timer General Register A	TGRA	16	16	2 or 3 PCLKB
0008 870Ah	MTU0	Timer General Register B	TGRB	16	16	2 or 3 PCLKB
0008 870Ch	MTU0	Timer General Register C	TGRC	16	16	2 or 3 PCLKB
0008 870Eh	MTU0	Timer General Register D	TGRD	16	16	2 or 3 PCLKB
0008 8720h	MTU0	Timer General Register E	TGRE	16	16	2 or 3 PCLKB
0008 8722h	MTU0	Timer General Register F	TGRF	16	16	2 or 3 PCLKB
0008 8724h	MTU0	Timer Interrupt Enable Register 2	TIER2	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (9/13)

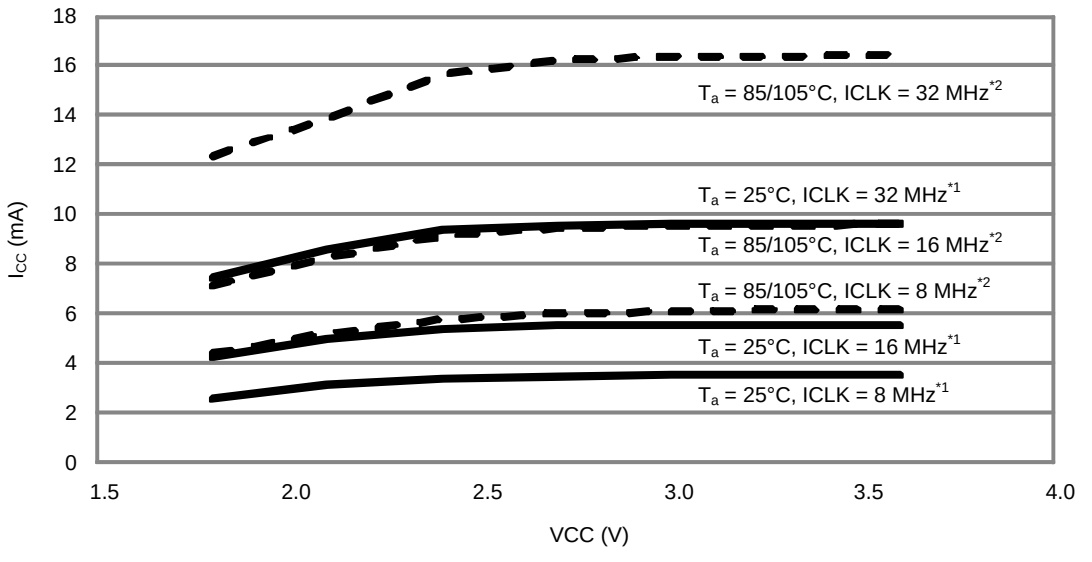
Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 B082h	DOC	DOC Data Input Register	DODIR	16	16	2 or 3 PCLKB
0008 B084h	DOC	DOC Data Setting Register	DODSR	16	16	2 or 3 PCLKB
0008 B300h	SCI12	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 B301h	SCI12	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 B302h	SCI12	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 B303h	SCI12	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 B304h	SCI12	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 B305h	SCI12	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 B306h	SCI12	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 B307h	SCI12	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 B308h	SCI12	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 B309h	SCI12	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 B30Ah	SCI12	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 B30Bh	SCI12	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 B30Ch	SCI12	I^2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 B30Dh	SCI12	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 B320h	SCI12	Extended Serial Mode Enable Register	ESMER	8	8	2 or 3 PCLKB
0008 B321h	SCI12	Control Register 0	CR0	8	8	2 or 3 PCLKB
0008 B322h	SCI12	Control Register 1	CR1	8	8	2 or 3 PCLKB
0008 B323h	SCI12	Control Register 2	CR2	8	8	2 or 3 PCLKB
0008 B324h	SCI12	Control Register 3	CR3	8	8	2 or 3 PCLKB
0008 B325h	SCI12	Port Control Register	PCR	8	8	2 or 3 PCLKB
0008 B326h	SCI12	Interrupt Control Register	ICR	8	8	2 or 3 PCLKB
0008 B327h	SCI12	Status Register	STR	8	8	2 or 3 PCLKB
0008 B328h	SCI12	Status Clear Register	STCR	8	8	2 or 3 PCLKB
0008 B329h	SCI12	Control Field 0 Data Register	CF0DR	8	8	2 or 3 PCLKB
0008 B32Ah	SCI12	Control Field 0 Compare Enable Register	CF0CR	8	8	2 or 3 PCLKB
0008 B32Bh	SCI12	Control Field 0 Receive Data Register	CF0RR	8	8	2 or 3 PCLKB
0008 B32Ch	SCI12	Primary Control Field 1 Data Register	PCF1DR	8	8	2 or 3 PCLKB
0008 B32Dh	SCI12	Secondary Control Field 1 Data Register	SCF1DR	8	8	2 or 3 PCLKB
0008 B32Eh	SCI12	Control Field 1 Compare Enable Register	CF1CR	8	8	2 or 3 PCLKB
0008 B32Fh	SCI12	Control Field 1 Receive Data Register	CF1RR	8	8	2 or 3 PCLKB
0008 B330h	SCI12	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 B331h	SCI12	Timer Mode Register	TMR	8	8	2 or 3 PCLKB
0008 B332h	SCI12	Timer Prescaler Register	TPRE	8	8	2 or 3 PCLKB
0008 B333h	SCI12	Timer Count Register	TCNT	8	8	2 or 3 PCLKB
0008 C000h	PORT0	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C001h	PORT1	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C002h	PORT2	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C003h	PORT3	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C004h	PORT4	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C005h	PORT5	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Ah	PORTA	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Bh	PORTB	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Ch	PORTC	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Eh	PORTE	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C011h	PORTH	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C012h	PORTJ	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C020h	PORT0	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C021h	PORT1	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C022h	PORT2	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C023h	PORT3	Port Output Data Register	PODR	8	8	2 or 3 PCLKB

Table 5.7 DC Characteristics (5) (2/2)

Conditions: 1.8 V ≤ VCC ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ *4	Max	Unit	Test Conditions
Supply current*1	Low-speed operating mode	Normal operating mode	No peripheral operation*7	ICLK = 32.768 kHz	I_{CC}	3.9	—	µA	
			All peripheral operation: Normal*8, *9	ICLK = 32.768 kHz		10.4	—		
			All peripheral operation: Max.*8, *9	ICLK = 32.768 kHz		—	36		
		Sleep mode	No peripheral operation*7	ICLK = 32.768 kHz		2.1	—		
			All peripheral operation: Normal*8	ICLK = 32.768 kHz		5.6	—		
		Deep sleep mode	No peripheral operation*7	ICLK = 32.768 kHz		1.7	—		
			All peripheral operation: Normal*8	ICLK = 32.768 kHz		3.9	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. Clock supply to the peripheral functions is stopped. The clock source is HOCO. FCLK and PCLK are set to divided by 64.
Note 3. Clocks are supplied to the peripheral functions. The clock source is HOCO. FCLK and PCLK are set to the same frequency as ICLK.
Note 4. Values when VCC = 3.3 V.
Note 5. Clock supply to the peripheral functions is stopped. The clock source is the main oscillation circuit when ICLK = 12 MHz and HOCO when ICLK = 8 or 1 MHz. FCLK and PCLK are set to divided by 64.
Note 6. Clocks are supplied to the peripheral functions. The clock source is the main oscillation circuit when ICLK = 12 MHz and HOCO when ICLK = 8 or 1 MHz. FCLK and PCLK are set to the same frequency as ICLK.
Note 7. Clock supply to the peripheral functions is stopped. The clock source is the sub-clock oscillator. FCLK and PCLK are set to divided by 64.
Note 8. Clocks are supplied to the peripheral functions. The clock source is the sub-clock oscillator. FCLK and PCLK are set to the same frequency as ICLK.
Note 9. Values when the MSTPCRA.MSTPA17 bit (12-bit A/D converter module stop bit) is set to “transition to the module stop state is made”.



Note 1. All peripheral operation is normal. Average value of the tested middle samples during product evaluation
Note 2. All peripheral operation is maximum. Average value of the tested upper-limit samples during product evaluation.

Figure 5.1 Voltage Dependency in High-Speed Operating Mode (Reference Data)

Table 5.16 Permissible Output Currents (2)

Conditions: 1.8 V ≤ VCC ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V,
T_a = –40 to +105°C (G version)

Item		Symbol	Max.	Unit
Permissible output low current (average value per pin)	Ports P40 to P44, P46, ports PJ6, PJ7	I_{OL}	0.4	mA
	Ports other than above		8.0	
Permissible output low current (maximum value per pin)	Ports P40 to P44, P46, ports PJ6, PJ7		0.4	
	Ports other than above		8.0	
Permissible output low current	Total of ports P40 to P44, P46, ports PJ6, PJ7	ΣI_{OL}	1.6	
	Total of ports P03, P05, ports P26, P27, ports P30, P31		20	
	Total of ports P14 to P17, port P32, ports P54, P55, ports PB0, PB1, PB3, PB5 to PB7, ports PC2 to PC7, ports PH0 to PH3		20	
	Total of ports PA0, PA1, PA3, PA4, PA6, ports PE0 to PE7		20	
	Total of all output pins		40	
Permissible output high current (average value per pin)	Ports P40 to P44, P46, ports PJ6, PJ7	I_{OH}	–0.1	
	Ports other than above		–4.0	
Permissible output high current (maximum value per pin)	Ports P40 to P44, P46, ports PJ6, PJ7		–0.1	
	Ports other than above		–4.0	
Permissible output high current	Total of ports P40 to P44, P46, ports PJ6, PJ7	ΣI_{OH}	–0.6	
	Total of ports P03, P05, ports P26, P27, ports P30, P31		–10	
	Total of ports P14 to P17, port P32, ports P54, P55, ports PB0, PB1, PB3, PB5 to PB7, ports PC2 to PC7, ports PH0 to PH3		–15	
	Total of ports PA0, PA1, PA3, PA4, PA6, ports PE0 to PE7		–15	
	Total of all output pins		–40	

Note: Do not exceed the permissible total supply current.

5.3 AC Characteristics

5.3.1 Clock Timing

Table 5.19 Operation Frequency Value (High-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.8 to 2.4 V	2.4 to 2.7 V	2.7 to 3.6 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	8	16	32	MHz
	FlashIF clock (FCLK)*1, *2		8	16	32	
	Peripheral module clock (PCLKB)		8	16	32	
	Peripheral module clock (PCLKD)*3		8	16	32	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the A/D converter is in use.

Table 5.20 Operation Frequency Value (Middle-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.8 to 2.4 V	2.4 to 2.7 V	2.7 to 3.6 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	8	12	12	MHz
	FlashIF clock (FCLK)*1, *2		8	12	12	
	Peripheral module clock (PCLKB)		8	12	12	
	Peripheral module clock (PCLKD)*3		8	12	12	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%.
Note 3. The lower-limit frequency of PCLKD is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the A/D converter is in use.

Table 5.21 Operation Frequency Value (Low-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.8 to 2.4 V	2.4 to 2.7 V	2.7 to 3.6 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	32.768			kHz
	FlashIF clock (FCLK)*1		32.768			
	Peripheral module clock (PCLKB)		32.768			
	Peripheral module clock (PCLKD)*2		32.768			

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The A/D converter cannot be used.

Table 5.22 Clock Timing

Conditions: 1.8 V ≤ VCC ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
XTAL external clock input cycle time		t_{Xcyc}	50	—	—	ns	Figure 5.18
XTAL external clock input high pulse width		t_{XH}	20	—	—	ns	
XTAL external clock input low pulse width		t_{XL}	20	—	—	ns	
XTAL external clock rising time		t_{Xr}	—	—	5	ns	
XTAL external clock falling time		t_{Xf}	—	—	5	ns	
XTAL external clock input wait time*1		t_{EXWT}	0.5	—	—	μs	
Main clock oscillator oscillation frequency	2.4 ≤ VCC ≤ 3.6	f_{MAIN}	1	—	20	MHz	
	1.8 ≤ VCC < 2.4		1	—	8		
Main clock oscillation stabilization time (crystal)*2		$t_{MAINOSC}$	—	3	—	ms	Figure 5.20
Main clock oscillation stabilization time (ceramic resonator)*2		$t_{MAINOSC}$	—	50		μs	
LOCO clock oscillation frequency		f_{LOCO}	3.44	4.0	4.56	MHz	
LOCO clock oscillation stabilization time		t_{LOCO}	—	—	0.5	μs	Figure 5.21
IWDT-dedicated clock oscillation frequency		f_{ILOCO}	12.75	15	17.25	kHz	
IWDT-dedicated clock oscillation stabilization time		t_{ILOCO}	—	—	50	μs	Figure 5.19
HOCO clock oscillation frequency		f_{HOCO}	31.52	32	32.48	MHz	T_a = –40 to 85°C
			31.68	32	32.32		T_a = –20 to 85°C
			31.36	32	32.64		T_a = –40 to 105°C
HOCO clock oscillation stabilization time		t_{HOCO2}	—	—	56	μs	Figure 5.23
Sub-clock oscillator oscillation frequency*4		f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization time*3		t_{SUBOSC}	—	0.5	—	s	Figure 5.24

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating) when the external clock is stable.

Note 2. Reference values when an 8-MHz oscillator is used.
When specifying the main clock oscillator stabilization time, set the MOSCWTCR register with a stabilization time value that is equal to or greater than the oscillator-manufacturer-recommended value.
After changing the setting of the MOSCCR.MOSTP bit so that the main clock oscillator operates, read the OSCOVFSR.MOOVF flag to confirm that is has become 1, and then start using the main clock.

Note 3. After changing the setting of the SOSCCR.SOSTP bit or RCR3.RTCEN bit so that the sub-clock oscillator operates, only start using the sub-clock after the sub-clock oscillation stabilization wait time that is equal to or greater than the oscillator-manufacturer-recommended value has elapsed.
Reference value when a 32.768-kHz resonator is used.

Note 4. Only 32.768 kHz can be used.

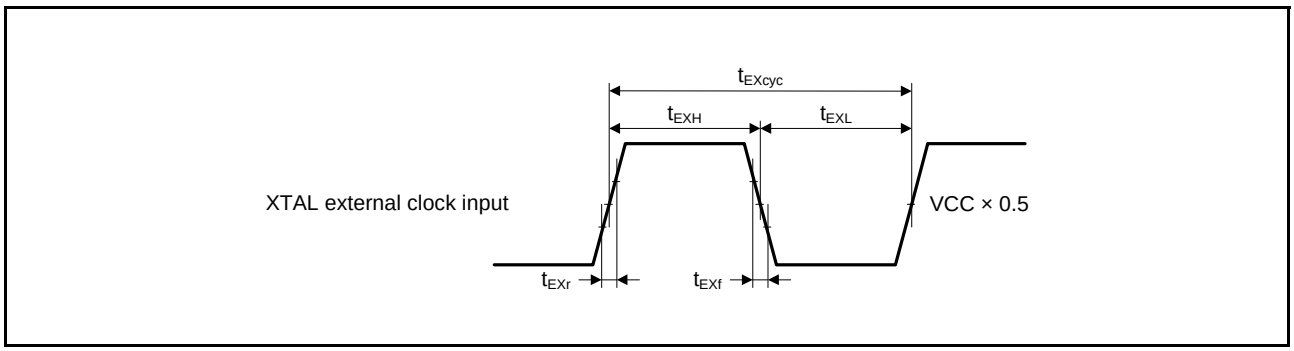


Figure 5.18 XTAL External Clock Input Timing

5.3.4 Control Signal Timing

Table 5.29 Control Signal Timing

Conditions: 1.8 V ≤ VCC ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled (NMIFLTE.NFLTEN = 0)	t_{Pcyc} × 2 ≤ 200 ns
		t_{Pcyc} × 2*1	—	—			t_{Pcyc} × 2 > 200 ns
		200	—	—		NMI digital filter enabled (NMIFLTE.NFLTEN = 1)	t_{NMICK} × 3 ≤ 200 ns
		t_{NMICK} × 3.5*2	—	—			t_{NMICK} × 3 > 200 ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled (IRQFLTE0.FLTENi = 0)	t_{Pcyc} × 2 ≤ 200 ns
		t_{Pcyc} × 2*1	—	—			t_{Pcyc} × 2 > 200 ns
		200	—	—		IRQ digital filter enabled (IRQFLTE0.FLTENi = 1)	t_{IRQCK} × 3 ≤ 200 ns
		t_{IRQCK} × 3.5*3	—	—			t_{IRQCK} × 3 > 200 ns

Note: 200 ns minimum in software standby mode.
Note 1. t_{Pcyc} indicates the cycle of PCLKB.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

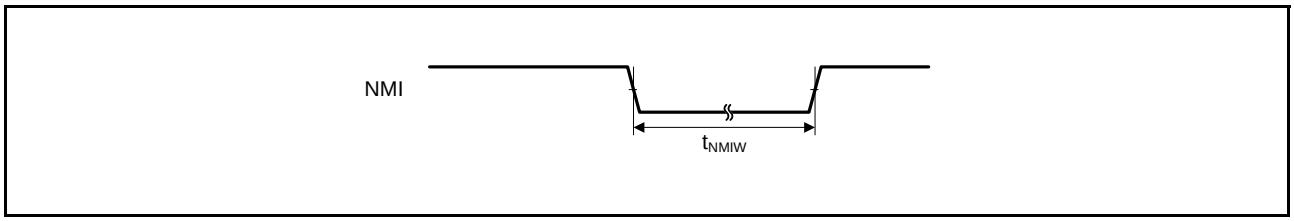


Figure 5.30 NMI Interrupt Input Timing

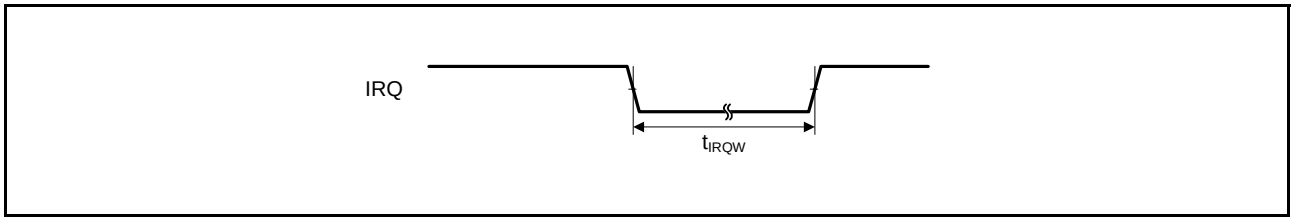


Figure 5.31 IRQ Interrupt Input Timing

Table 5.31 Timing of On-Chip Peripheral Modules (2)

Conditions: 1.8 V ≤ VCC ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C, C = 30 pF

Item				Symbol	Min.	Max.	Unit	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc} *1	Figure 5.39
		Slave			8	4096		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time	Output	2.7 V or above	t_{SPCKr}, t_{SPCKf}	—	10	ns	
			1.8 V or above		—	15		
		Input			—	1	µs	
	Data input setup time	Master	2.7 V or above	t_{SU}	10	—	ns	Figure 5.40 to Figure 5.45
			1.8 V or above		30	—		
		Slave			$25 - t_{Pcyc}$	—		
	Data input hold time	Master	RSPCK set to a division ratio other than PCLKB divided by 2	t_H	t_{Pcyc}	—	ns	
			RSPCK set to PCLKB divided by 2	t_{HF}	0	—		
		Slave		t_H	$20 + 2 \times t_{Pcyc}$	—		
	SSL setup time	Master		t_{LEAD}	$–30 + N^{*2} \times t_{SPcyc}$	—	ns	
		Slave			2	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	$–30 + N^{*3} \times t_{SPcyc}$	—	ns	
		Slave			2	—	t_{Pcyc}	
	Data output delay time	Master	2.7 V or above	t_{OD}	—	14	ns	
			1.8 V or above		—	30		
		Slave	2.7 V or above		—	$3 \times t_{Pcyc} + 65$		
			1.8 V or above		—	$3 \times t_{Pcyc} + 105$		
	Data output hold time	Master	2.7 V or above	t_{OH}	0	—	ns	
			1.8 V or above		–20	—		
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$4 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output	2.7 V or above	t_{Dr}, t_{Df}	—	10	ns	
			1.8 V or above		—	20		
		Input			—	1	µs	
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	20	ns	
		Input			—	1	µs	
	Slave access time		2.7 V or above	t_{SA}	—	6	t_{Pcyc}	Figure 5.44, Figure 5.45
			1.8 V or above		—	7		
	Slave output release time		2.7 V or above	t_{REL}	—	5	t_{Pcyc}	
			1.8 V or above		—	6		

Note 1. t_{Pcyc}: PCLK cycle
Note 2. N: An integer from 1 to 8 that can be set by the RSPI clock delay register (SPCKD)
Note 3. N: An integer from 1 to 8 that can be set by the RSPI slave select negation delay register (SSLND)

5.4 A/D Conversion Characteristics

Table 5.35 A/D Conversion Characteristics (1)

Conditions: 2.7 V ≤ VCC ≤ 3.6 V, 2.7 V ≤ AVCC0 ≤ 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0, VSS = AVSS0 = VREFL0 = 0 V,
T_a = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		4	—	32	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 32 MHz)	Permissible signal source impedance (Max.) = 0.3 kΩ	1.031 (0.313)*2	—	—	µs	High-precision channel ADCSR.ADHSC bit = 1 ADSSTRn.SST[7:0] bits = 09h
		1.375 (0.641)*2	—	—		Normal-precision channel ADCSR.ADHSC bit = 1 ADSSTRn.SST[7:0] bits = 14h
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±0.5	±4.5	LSB	High-precision channel PJ6PFS.ASEL bit = 1 PJ7PFS.ASEL bit = 1
				±6.0	LSB	Other than above
Full-scale error		—	±0.75	±4.5	LSB	High-precision channel PJ6PFS.ASEL bit = 1 PJ7PFS.ASEL bit = 1
				±6.0	LSB	Other than above
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±1.25	±5.0	LSB	High-precision channel PJ6PFS.ASEL bit = 1 PJ7PFS.ASEL bit = 1
				±8.0	LSB	Other than above
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.0	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actually output code.

Offset error

Offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

5.5 Temperature Sensor Characteristics

Table 5.40 Temperature Sensor Characteristics

Conditions: 2.0 V ≤ VCC ≤ 3.6 V, 2.0 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	—	±1.5	—	°C	2.4 V or above
		—	±2.0	—		Below 2.4 V
Temperature slope	—	—	–3.65	—	mV/°C	
Output voltage (at 25°C)	—	—	1.05	—	V	VCC = 3.3 V
Temperature sensor start time	t_{START}	—	—	5	µs	
Sampling time	—	5	—	—	µs	