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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5110jadfl-30

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications, and Table 1.2 gives a comparison of the functions of the products in different packages.
Table 1.1 is for products with the greatest number of functions, so the number of peripheral modules and channels will differ in accordance with the package type. For details, see Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/3)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 32 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per one clock cycle • Address space: 4-Gbyte linear • Register set General purpose: Sixteen 32-bit registers Control: Eight 32-bit registers Accumulator: One 64-bit register • Basic instructions: 73 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32-bit × 32-bit → 64-bit • On-chip divider: 32-bit ÷ 32-bit → 32 bits • Barrel shifter: 32 bits
Memory	ROM	• Capacity: 8 K /16 K /32 K /64 K /96 K /128 Kbytes • 32 MHz, no-wait memory access • Programming/erasing method: Serial programming (asynchronous serial communication), self-programming
	RAM	• Capacity: 8 K /10 K /16 Kbytes • 32 MHz, no-wait memory access
MCU operating mode		Single-chip mode
Clock	Clock generation circuit	• Main clock oscillator, sub-clock oscillator, low-speed on-chip oscillator, high-speed on-chip oscillator, and IWDT-dedicated on-chip oscillator • Oscillation stop detection: Available • Clock frequency accuracy measurement circuit (CAC) • Independent settings for the system clock (ICLK), peripheral module clock (PCLK), and FlashIF clock (FCLK) The CPU and system sections such as other bus masters run in synchronization with the system clock (ICLK): 32 MHz (at max.) Peripheral modules run in synchronization with the PCLK: 32 MHz (at max.) The flash peripheral circuit runs in synchronization with the FCLK: 32 MHz (at max.) • The ICLK frequency can only be set to FCLK, PCLKB, or PCLKD multiplied by n (n: 1, 2, 4, 8, 16, 32, 64).
Resets		RES# pin reset, power-on reset, voltage monitoring reset, independent watchdog timer reset, and software reset
Voltage detection	Voltage detection circuit (LVDAa)	• When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. Voltage detection circuit 1 is capable of selecting the detection voltage from 10 levels Voltage detection circuit 2 is capable of selecting the detection voltage from 4 levels
Low power consumption	Low power consumption functions	• Module stop function • Three low power consumption modes Sleep mode, deep sleep mode, and software standby mode
	Function for lower operating power consumption	• Operating power control modes High-speed operating mode, middle-speed operating mode, and low-speed operating mode
Interrupt	Interrupt controller (ICUb)	• Interrupt vectors: 65 • External interrupts: 9 (NMI, IRQ0 to IRQ7 pins) • Non-maskable interrupts: 4 (NMI pin, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, and IWDT interrupt) • 16 levels specifiable for the order of priority
DMA	Data transfer controller (DTCa)	• Transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Interrupts • Chain transfer function

Table 1.1 Outline of Specifications (3/3)

Classification	Module/Function	Description
Data operation circuit (DOC)		Comparison, addition, and subtraction of 16-bit data
Unique ID		32-byte ID code for the MCU
Power supply voltages/Operating frequencies		VCC = 1.8 to 2.4 V: 8 MHz, VCC = 2.4 to 2.7 V: 16 MHz, VCC = 2.7 to 3.6 V: 32 MHz
Supply current		3.2 mA at 32 MHz (typ.)
Operating temperatures		D version: –40 to +85°C, G version: –40 to +105°C
Packages		64-pin LFQFP (PLQP0064KB-A) 10 × 10 mm, 0.5 mm pitch 64-pin LQFP (PLQP0064GA-A) 14 × 14 mm, 0.8 mm pitch 64-pin WFLGA (PWLG0064KA-A) 5 × 5 mm, 0.5 mm pitch 48-pin LFQFP (PLQP0048KB-A) 7 × 7 mm, 0.5 mm pitch 48-pin HWQFN (PWQN0048KB-A) 7 × 7 mm, 0.5 mm pitch 40-pin HWQFN (PWQN0040KC-A) 6 × 6 mm, 0.5 mm pitch 36-pin WFLGA (PWLG0036KA-A) 4 × 4 mm, 0.5 mm pitch
On-chip debugging system		E1 emulator (FINE interface)

Table 1.3 List of Products (2/2)

Group	Part No.	Orderable Part No.	Package	ROM Capacity	RAM Capacity	Maximum Operating Frequency	Operating Temperature
RX110	R5F51105ADFM	R5F51105ADFM#30	PLQP0064KB-A	128 Kbytes	16 Kbytes	32MHz	–40 to +85°C
	R5F51105ADFK	R5F51105ADFK#30	PLQP0064GA-A				
	R5F51105ADLF	R5F51105ADLF#U0	PWLG0064KA-A				
	R5F51105ADFL	R5F51105ADFL#30	PLQP0048KB-A				
	R5F51105ADNE	R5F51105ADNE#U0	PWQN0048KB-A				
	R5F51104ADFM	R5F51104ADFM#30	PLQP0064KB-A	96 Kbytes			
	R5F51104ADFK	R5F51104ADFK#30	PLQP0064GA-A				
	R5F51104ADLF	R5F51104ADLF#U0	PWLG0064KA-A				
	R5F51104ADFL	R5F51104ADFL#30	PLQP0048KB-A				
	R5F51104ADNE	R5F51104ADNE#U0	PWQN0048KB-A				
	R5F51103ADFM	R5F51103ADFM#30	PLQP0064KB-A	64 Kbytes	10 Kbytes		
	R5F51103ADFK	R5F51103ADFK#30	PLQP0064GA-A				
	R5F51103ADLF	R5F51103ADLF#U0	PWLG0064KA-A				
	R5F51103ADFL	R5F51103ADFL#30	PLQP0048KB-A				
	R5F51103ADNE	R5F51103ADNE#U0	PWQN0048KB-A				
	R5F51103ADLM	R5F51103ADLM#U0	PWLG0036KA-A				
	R5F51103ADNF	R5F51103ADNF#U0	PWQN0040KC-A				
	R5F51101ADFM	R5F51101ADFM#30	PLQP0064KB-A	32 Kbytes			
	R5F51101ADFK	R5F51101ADFK#30	PLQP0064GA-A				
	R5F51101ADLF	R5F51101ADLF#U0	PWLG0064KA-A				
	R5F51101ADFL	R5F51101ADFL#30	PLQP0048KB-A				
	R5F51101ADNE	R5F51101ADNE#U0	PWQN0048KB-A				
	R5F51101ADLM	R5F51101ADLM#U0	PWLG0036KA-A				
	R5F51101ADNF	R5F51101ADNF#U0	PWQN0040KC-A				
	R5F5110JADFM	R5F5110JADFM#30	PLQP0064KB-A	16 Kbytes	8 Kbytes		
	R5F5110JADFK	R5F5110JADFK#30	PLQP0064GA-A				
	R5F5110JADLF	R5F5110JADLF#U0	PWLG0064KA-A				
	R5F5110JADFL	R5F5110JADFL#30	PLQP0048KB-A				
	R5F5110JADNE	R5F5110JADNE#U0	PWQN0048KB-A				
	R5F5110JADLM	R5F5110JADLM#U0	PWLG0036KA-A				
	R5F5110JADNF	R5F5110JADNF#U0	PWQN0040KC-A				
	R5F5110HADLM	R5F5110HADLM#U0	PWLG0036KA-A	8 Kbytes			
	R5F5110HADNF	R5F5110HADNF#U0	PWQN0040KC-A				

Note: Orderable part numbers are current as of when this manual was published. Please make sure to refer to the relevant product page on the Renesas website for the latest part numbers.

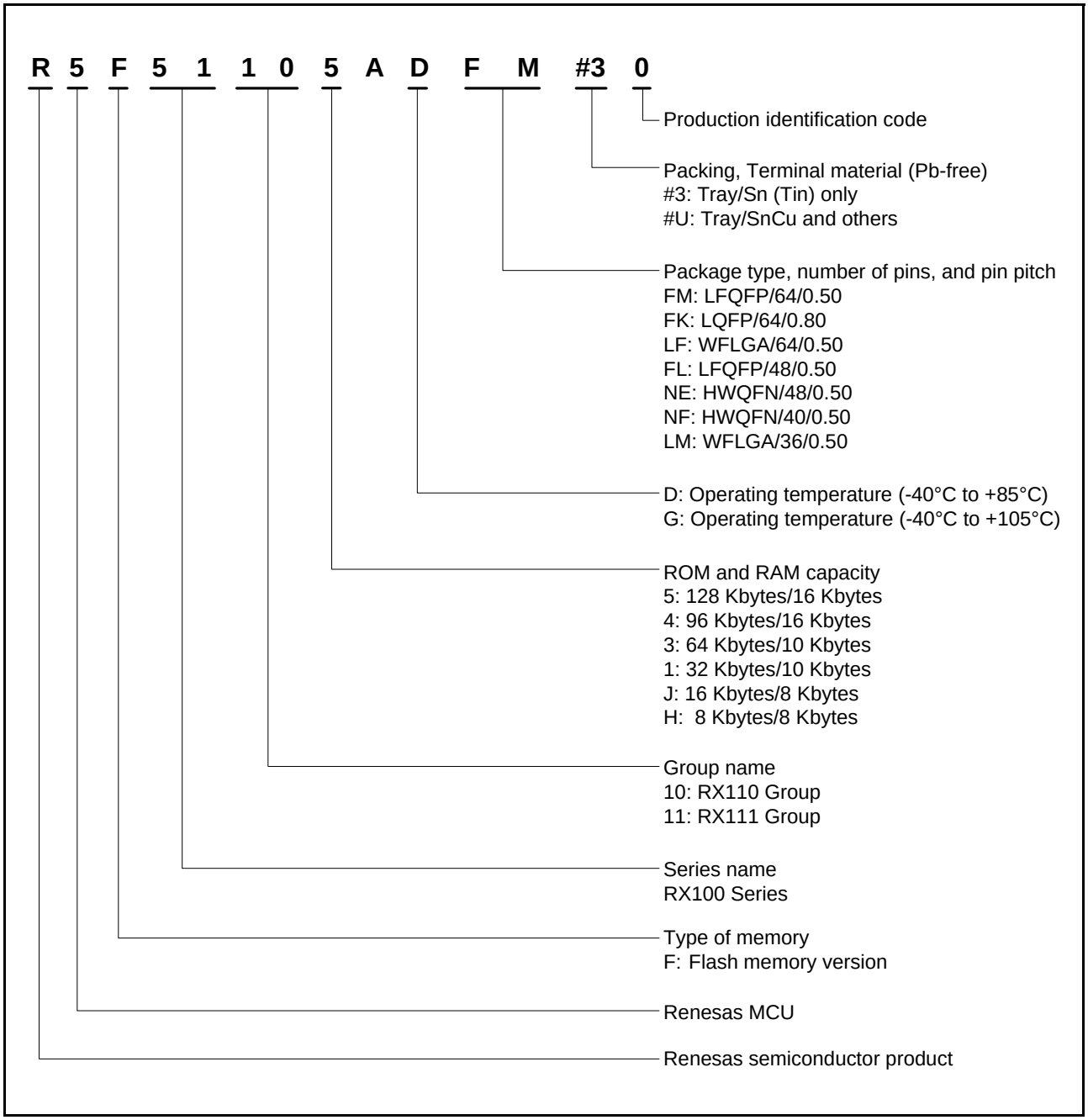
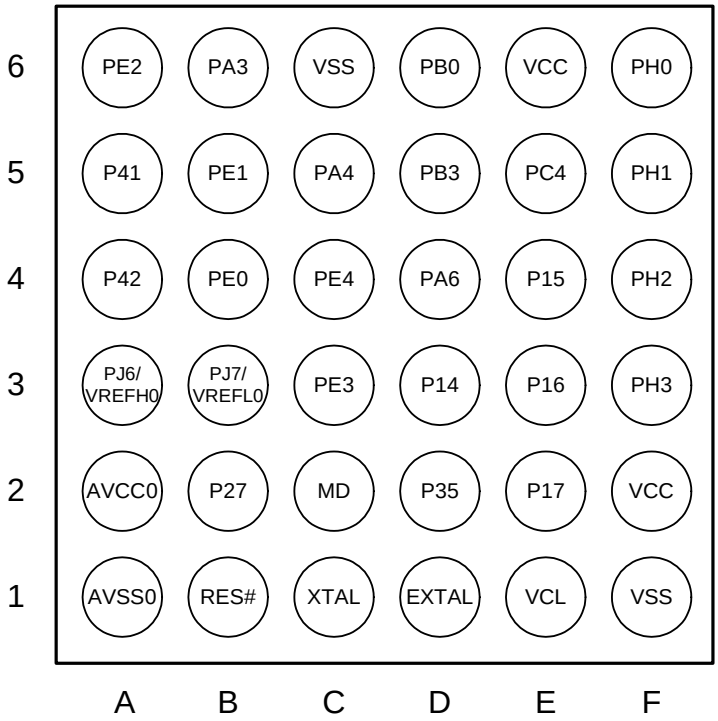


Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type

RX110 Group
PWLG0036KA-A
(36-pin WFLGA)
(Upper perspective view)



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (36-Pin WFLGA)”.
Note: For the position of A1 pin in the package, see “Package Dimensions”.

Figure 1.7 Pin Assignments of the 36-Pin WFLGA

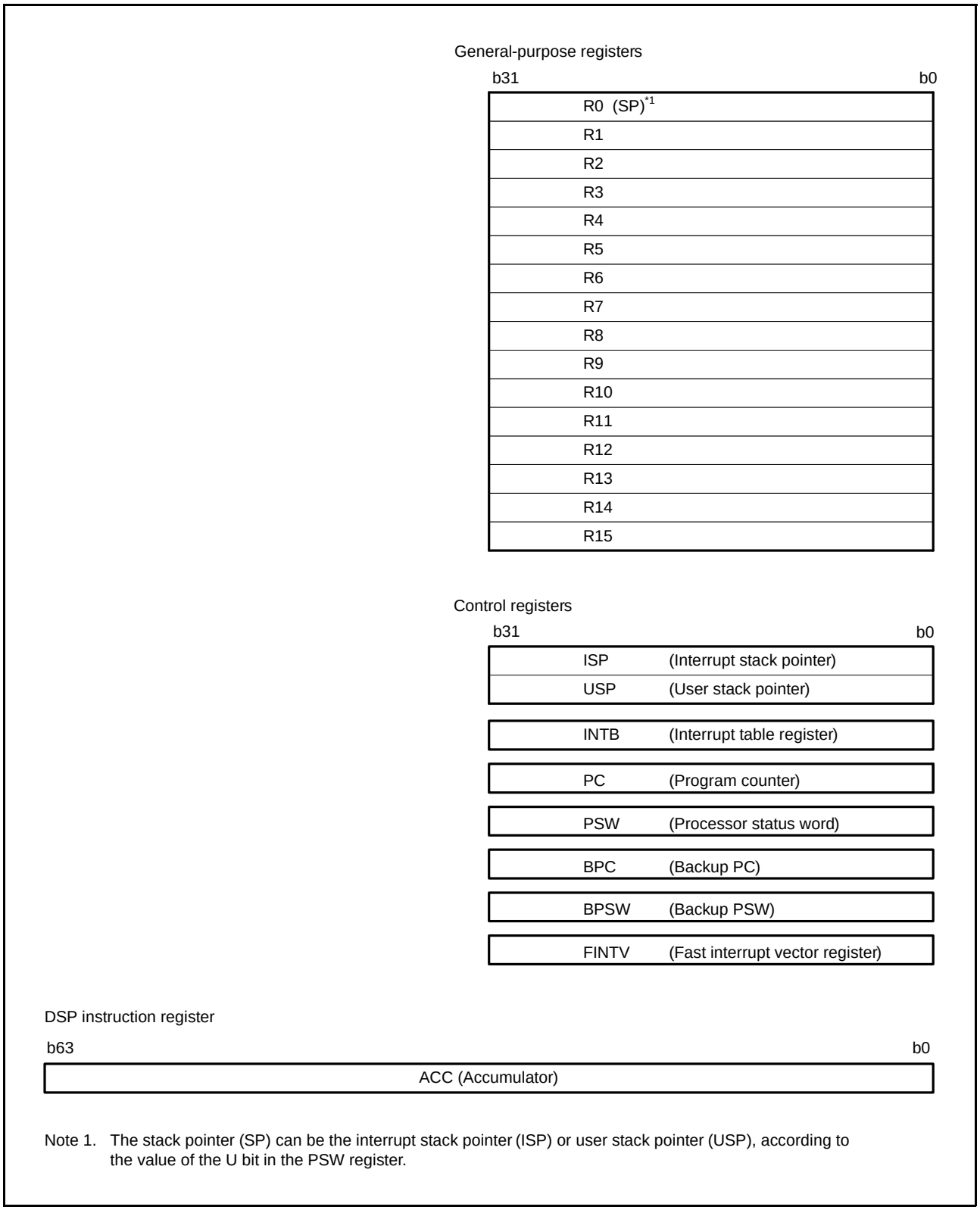
Table 1.7 List of Pins and Pin Functions (48-Pin LFQFP/HWQFN) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, RTC)	Communication (SCIe, SCIf, RSPI, RIIC)	Others
45		P40*1			AN000
46	VREFH0	PJ6*1			
47	AVSS0				
48	AVCC0				

Note 1. The power source of the I/O buffer for these pins is AVCC0.

2. CPU

Figure 2.1 shows the register set of the CPU.



Note 1. The stack pointer (SP) can be the interrupt stack pointer (ISP) or user stack pointer (USP), according to the value of the U bit in the PSW register.

Figure 2.1 Register Set of the CPU

2.1 General-Purpose Registers (R0 to R15)

This CPU has 16 general-purpose registers (R0 to R15). R0 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP). The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).
Set the ISP or USP to a multiple of 4, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

(3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(4) Processor Status Word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

2.3 Register Associated with DSP Instructions

(1) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.
Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.
Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

When executing an instruction after writing to multiple registers, only read the last I/O register written to and execute the instruction using that value; it is not necessary to execute the instruction using the values written to all the registers.

(3) Number of cycles necessary for accessing I/O registers

See Table 4.1 for details on the number of clock cycles necessary for accessing I/O registers.
The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided clock synchronization cycles +
Number of bus cycles for internal peripheral buses 1, 2, and 4 to 6

The number of bus cycles of internal peripheral buses 1, 2, and 4 to 6 differs according to the register to be accessed. When peripheral functions connected to internal peripheral buses 2, and 4 to 6 or registers for the external bus control unit (except for bus error related registers) are accessed, the number of divided clock synchronization cycles is added. The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK) or bus access timing.
In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access cycles shown in Table 4.1.
When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the bus access from the different bus master (DTC).

(4) Notes on sleep mode and mode transitions

During sleep mode or mode transitions, do not write to the system control related registers (indicated by ‘SYSTEM’ in the Module Symbol column in Table 4.1, List of I/O Registers (Address Order)).

Table 4.1 List of I/O Registers (Address Order) (4/13)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 71F8h	ICU	DTC Activation Enable Register 248	DTCER248	8	8	2 ICLK
0008 7202h	ICU	Interrupt Request Enable Register 02	IER02	8	8	2 ICLK
0008 7203h	ICU	Interrupt Request Enable Register 03	IER03	8	8	2 ICLK
0008 7204h	ICU	Interrupt Request Enable Register 04	IER04	8	8	2 ICLK
0008 7205h	ICU	Interrupt Request Enable Register 05	IER05	8	8	2 ICLK
0008 7207h	ICU	Interrupt Request Enable Register 07	IER07	8	8	2 ICLK
0008 7208h	ICU	Interrupt Request Enable Register 08	IER08	8	8	2 ICLK
0008 720Bh	ICU	Interrupt Request Enable Register 0B	IER0B	8	8	2 ICLK
0008 720Ch	ICU	Interrupt Request Enable Register 0C	IER0C	8	8	2 ICLK
0008 720Eh	ICU	Interrupt Request Enable Register 0E	IER0E	8	8	2 ICLK
0008 720Fh	ICU	Interrupt Request Enable Register 0F	IER0F	8	8	2 ICLK
0008 7210h	ICU	Interrupt Request Enable Register 10	IER10	8	8	2 ICLK
0008 7211h	ICU	Interrupt Request Enable Register 11	IER11	8	8	2 ICLK
0008 721Bh	ICU	Interrupt Request Enable Register 1B	IER1B	8	8	2 ICLK
0008 721Ch	ICU	Interrupt Request Enable Register 1C	IER1C	8	8	2 ICLK
0008 721Dh	ICU	Interrupt Request Enable Register 1D	IER1D	8	8	2 ICLK
0008 721Eh	ICU	Interrupt Request Enable Register 1E	IER1E	8	8	2 ICLK
0008 721Fh	ICU	Interrupt Request Enable Register 1F	IER1F	8	8	2 ICLK
0008 72E0h	ICU	Software Interrupt Activation Register	SWINTR	8	8	2 ICLK
0008 72F0h	ICU	Fast Interrupt Set Register	FIR	16	16	2 ICLK
0008 7300h	ICU	Interrupt Source Priority Register 000	IPR000	8	8	2 ICLK
0008 7303h	ICU	Interrupt Source Priority Register 003	IPR003	8	8	2 ICLK
0008 7304h	ICU	Interrupt Source Priority Register 004	IPR004	8	8	2 ICLK
0008 7305h	ICU	Interrupt Source Priority Register 005	IPR005	8	8	2 ICLK
0008 7320h	ICU	Interrupt Source Priority Register 032	IPR032	8	8	2 ICLK
0008 7321h	ICU	Interrupt Source Priority Register 033	IPR033	8	8	2 ICLK
0008 7322h	ICU	Interrupt Source Priority Register 034	IPR034	8	8	2 ICLK
0008 732Ch	ICU	Interrupt Source Priority Register 044	IPR044	8	8	2 ICLK
0008 7339h	ICU	Interrupt Source Priority Register 057	IPR057	8	8	2 ICLK
0008 733Fh	ICU	Interrupt Source Priority Register 063	IPR063	8	8	2 ICLK
0008 7340h	ICU	Interrupt Source Priority Register 064	IPR064	8	8	2 ICLK
0008 7341h	ICU	Interrupt Source Priority Register 065	IPR065	8	8	2 ICLK
0008 7342h	ICU	Interrupt Source Priority Register 066	IPR066	8	8	2 ICLK
0008 7343h	ICU	Interrupt Source Priority Register 067	IPR067	8	8	2 ICLK
0008 7344h	ICU	Interrupt Source Priority Register 068	IPR068	8	8	2 ICLK
0008 7345h	ICU	Interrupt Source Priority Register 069	IPR069	8	8	2 ICLK
0008 7346h	ICU	Interrupt Source Priority Register 070	IPR070	8	8	2 ICLK
0008 7347h	ICU	Interrupt Source Priority Register 071	IPR071	8	8	2 ICLK
0008 7358h	ICU	Interrupt Source Priority Register 088	IPR088	8	8	2 ICLK
0008 7359h	ICU	Interrupt Source Priority Register 089	IPR089	8	8	2 ICLK
0008 735Ch	ICU	Interrupt Source Priority Register 092	IPR092	8	8	2 ICLK
0008 735Dh	ICU	Interrupt Source Priority Register 093	IPR093	8	8	2 ICLK
0008 7366h	ICU	Interrupt Source Priority Register 102	IPR102	8	8	2 ICLK
0008 7367h	ICU	Interrupt Source Priority Register 103	IPR103	8	8	2 ICLK
0008 7372h	ICU	Interrupt Source Priority Register 114	IPR114	8	8	2 ICLK
0008 7376h	ICU	Interrupt Source Priority Register 118	IPR118	8	8	2 ICLK
0008 7379h	ICU	Interrupt Source Priority Register 121	IPR121	8	8	2 ICLK
0008 737Bh	ICU	Interrupt Source Priority Register 123	IPR123	8	8	2 ICLK
0008 737Dh	ICU	Interrupt Source Priority Register 125	IPR125	8	8	2 ICLK
0008 737Fh	ICU	Interrupt Source Priority Register 127	IPR127	8	8	2 ICLK
0008 738Bh	ICU	Interrupt Source Priority Register 139	IPR139	8	8	2 ICLK
0008 73DAh	ICU	Interrupt Source Priority Register 218	IPR218	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (6/13)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 830Ah	RIIC0	Timeout Internal Counter L	TMOCNTL	8	8	2 or 3 PCLKB
0008 830Bh	RIIC0	Slave Address Register U0	SARU0	8	8	2 or 3 PCLKB
0008 830Bh	RIIC0	Timeout Internal Counter U	TMOCNTU	8	8 *1	2 or 3 PCLKB
0008 830Ch	RIIC0	Slave Address Register L1	SARL1	8	8	2 or 3 PCLKB
0008 830Dh	RIIC0	Slave Address Register U1	SARU1	8	8	2 or 3 PCLKB
0008 830Eh	RIIC0	Slave Address Register L2	SARL2	8	8	2 or 3 PCLKB
0008 830Fh	RIIC0	Slave Address Register U2	SARU2	8	8	2 or 3 PCLKB
0008 8310h	RIIC0	I^2C Bus Bit Rate Low-Level Register	ICBRL	8	8	2 or 3 PCLKB
0008 8311h	RIIC0	I^2C Bus Bit Rate High-Level Register	ICBRH	8	8	2 or 3 PCLKB
0008 8312h	RIIC0	I^2C Bus Transmit Data Register	ICDRT	8	8	2 or 3 PCLKB
0008 8313h	RIIC0	I^2C Bus Receive Data Register	ICDRR	8	8	2 or 3 PCLKB
0008 8380h	RSPI0	RSPI Control Register	SPCR	8	8	2 or 3 PCLKB
0008 8381h	RSPI0	RSPI Slave Select Polarity Register	SSLP	8	8	2 or 3 PCLKB
0008 8382h	RSPI0	RSPI Pin Control Register	SPPCR	8	8	2 or 3 PCLKB
0008 8383h	RSPI0	RSPI Status Register	SPSR	8	8	2 or 3 PCLKB
0008 8384h	RSPI0	RSPI Data Register	SPDR	32	16, 32	2 or 3 PCLKB/2ICLK
0008 8388h	RSPI0	RSPI Sequence Control Register	SPSCR	8	8	2 or 3 PCLKB
0008 8389h	RSPI0	RSPI Sequence Status Register	SPSSR	8	8	2 or 3 PCLKB
0008 838Ah	RSPI0	RSPI Bit Rate Register	SPBR	8	8	2 or 3 PCLKB
0008 838Bh	RSPI0	RSPI Data Control Register	SPDCR	8	8	2 or 3 PCLKB
0008 838Ch	RSPI0	RSPI Clock Delay Register	SPCKD	8	8	2 or 3 PCLKB
0008 838Dh	RSPI0	RSPI Slave Select Negation Delay Register	SSLND	8	8	2 or 3 PCLKB
0008 838Eh	RSPI0	RSPI Next-Access Delay Register	SPND	8	8	2 or 3 PCLKB
0008 838Fh	RSPI0	RSPI Control Register 2	SPCR2	8	8	2 or 3 PCLKB
0008 8390h	RSPI0	RSPI Command Register 0	SPCMD0	16	16	2 or 3 PCLKB
0008 8392h	RSPI0	RSPI Command Register 1	SPCMD1	16	16	2 or 3 PCLKB
0008 8394h	RSPI0	RSPI Command Register 2	SPCMD2	16	16	2 or 3 PCLKB
0008 8396h	RSPI0	RSPI Command Register 3	SPCMD3	16	16	2 or 3 PCLKB
0008 8398h	RSPI0	RSPI Command Register 4	SPCMD4	16	16	2 or 3 PCLKB
0008 839Ah	RSPI0	RSPI Command Register 5	SPCMD5	16	16	2 or 3 PCLKB
0008 839Ch	RSPI0	RSPI Command Register 6	SPCMD6	16	16	2 or 3 PCLKB
0008 839Eh	RSPI0	RSPI Command Register 7	SPCMD7	16	16	2 or 3 PCLKB
0008 8680h	MTU	Timer Start Register	TSTR	8	8, 16	2 or 3 PCLKB
0008 8681h	MTU	Timer Synchronous Register	TSYR	8	8, 16	2 or 3 PCLKB
0008 8690h	MTU0	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB
0008 8691h	MTU1	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB
0008 8692h	MTU2	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB
0008 8695h	MTU5	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB
0008 8700h	MTU0	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8701h	MTU0	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB
0008 8702h	MTU0	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKB
0008 8703h	MTU0	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKB
0008 8704h	MTU0	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 8705h	MTU0	Timer Status Register	TSR	8	8	2 or 3 PCLKB
0008 8706h	MTU0	Timer Counter	TCNT	16	16	2 or 3 PCLKB
0008 8708h	MTU0	Timer General Register A	TGRA	16	16	2 or 3 PCLKB
0008 870Ah	MTU0	Timer General Register B	TGRB	16	16	2 or 3 PCLKB
0008 870Ch	MTU0	Timer General Register C	TGRC	16	16	2 or 3 PCLKB
0008 870Eh	MTU0	Timer General Register D	TGRD	16	16	2 or 3 PCLKB
0008 8720h	MTU0	Timer General Register E	TGRE	16	16	2 or 3 PCLKB
0008 8722h	MTU0	Timer General Register F	TGRF	16	16	2 or 3 PCLKB
0008 8724h	MTU0	Timer Interrupt Enable Register 2	TIER2	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (9/13)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 B082h	DOC	DOC Data Input Register	DODIR	16	16	2 or 3 PCLKB
0008 B084h	DOC	DOC Data Setting Register	DODSR	16	16	2 or 3 PCLKB
0008 B300h	SCI12	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 B301h	SCI12	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 B302h	SCI12	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 B303h	SCI12	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 B304h	SCI12	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 B305h	SCI12	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 B306h	SCI12	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 B307h	SCI12	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 B308h	SCI12	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 B309h	SCI12	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 B30Ah	SCI12	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 B30Bh	SCI12	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 B30Ch	SCI12	I^2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 B30Dh	SCI12	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 B320h	SCI12	Extended Serial Mode Enable Register	ESMER	8	8	2 or 3 PCLKB
0008 B321h	SCI12	Control Register 0	CR0	8	8	2 or 3 PCLKB
0008 B322h	SCI12	Control Register 1	CR1	8	8	2 or 3 PCLKB
0008 B323h	SCI12	Control Register 2	CR2	8	8	2 or 3 PCLKB
0008 B324h	SCI12	Control Register 3	CR3	8	8	2 or 3 PCLKB
0008 B325h	SCI12	Port Control Register	PCR	8	8	2 or 3 PCLKB
0008 B326h	SCI12	Interrupt Control Register	ICR	8	8	2 or 3 PCLKB
0008 B327h	SCI12	Status Register	STR	8	8	2 or 3 PCLKB
0008 B328h	SCI12	Status Clear Register	STCR	8	8	2 or 3 PCLKB
0008 B329h	SCI12	Control Field 0 Data Register	CF0DR	8	8	2 or 3 PCLKB
0008 B32Ah	SCI12	Control Field 0 Compare Enable Register	CF0CR	8	8	2 or 3 PCLKB
0008 B32Bh	SCI12	Control Field 0 Receive Data Register	CF0RR	8	8	2 or 3 PCLKB
0008 B32Ch	SCI12	Primary Control Field 1 Data Register	PCF1DR	8	8	2 or 3 PCLKB
0008 B32Dh	SCI12	Secondary Control Field 1 Data Register	SCF1DR	8	8	2 or 3 PCLKB
0008 B32Eh	SCI12	Control Field 1 Compare Enable Register	CF1CR	8	8	2 or 3 PCLKB
0008 B32Fh	SCI12	Control Field 1 Receive Data Register	CF1RR	8	8	2 or 3 PCLKB
0008 B330h	SCI12	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 B331h	SCI12	Timer Mode Register	TMR	8	8	2 or 3 PCLKB
0008 B332h	SCI12	Timer Prescaler Register	TPRE	8	8	2 or 3 PCLKB
0008 B333h	SCI12	Timer Count Register	TCNT	8	8	2 or 3 PCLKB
0008 C000h	PORT0	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C001h	PORT1	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C002h	PORT2	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C003h	PORT3	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C004h	PORT4	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C005h	PORT5	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Ah	PORTA	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Bh	PORTB	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Ch	PORTC	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Eh	PORTE	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C011h	PORTH	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C012h	PORTJ	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C020h	PORT0	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C021h	PORT1	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C022h	PORT2	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C023h	PORT3	Port Output Data Register	PODR	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (10/13)

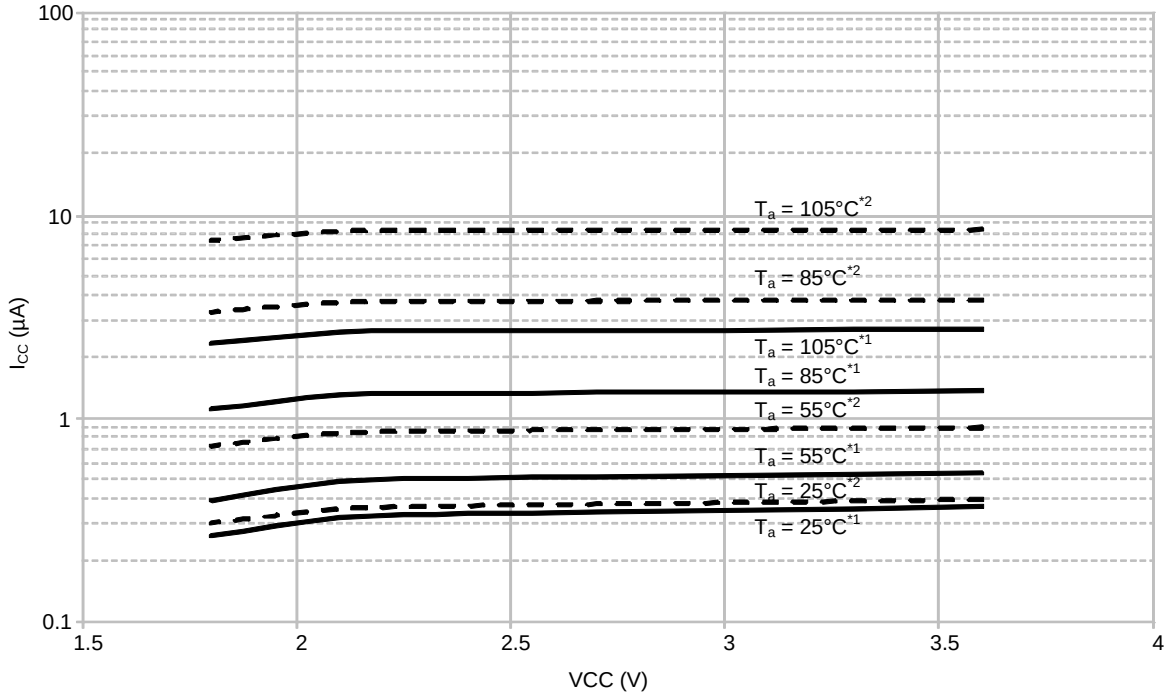
Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 C024h	PORT4	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C025h	PORT5	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C02Ah	PORTA	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C02Bh	PORTB	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C02Ch	PORTC	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C02Eh	PORTE	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C031h	PORTH	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C032h	PORTJ	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C040h	PORT0	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C041h	PORT1	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C042h	PORT2	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C043h	PORT3	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C044h	PORT4	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C045h	PORT5	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C04Ah	PORTA	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C04Bh	PORTB	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C04Ch	PORTC	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C04Eh	PORTE	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C051h	PORTH	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C052h	PORTJ	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C060h	PORT0	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C061h	PORT1	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C062h	PORT2	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C063h	PORT3	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C064h	PORT4	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C065h	PORT5	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Ah	PORTA	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Bh	PORTB	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Ch	PORTC	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Eh	PORTE	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C071h	PORTH	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C072h	PORTJ	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C083h	PORT1	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C085h	PORT2	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C086h	PORT3	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C094h	PORTA	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C095h	PORTA	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C096h	PORTB	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C097h	PORTB	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C098h	PORTC	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C099h	PORTC	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C09Ch	PORTE	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C09Dh	PORTE	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C0C0h	PORT0	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C1h	PORT1	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C2h	PORT2	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB

Table 5.8 DC Characteristics (6)

Conditions: 1.8 V ≤ VCC ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Typ.*3	Max.	Unit	Test Conditions
Supply current*1	Software standby mode*2	T_a = 25°C	I_{CC}	0.35	0.53	µA	
		T_a = 55°C		0.54	1.17		
		T_a = 85°C		1.38	5.2		
		T_a = 105°C		2.8	11.4		
	Increment for RTC operation*4			0.31	—		RCR3.RTCDV[2:0] = 010b
				1.09	—		RCR3.RTCDV[2:0] = 100b
	Increment for IWDT operation			0.37	—		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. The IWDT and LVD are stopped.
Note 3. VCC = 3.3 V.
Note 4. Includes the oscillation circuit.



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.4 Voltage Dependency in Software Standby Mode (Reference Data)

Table 5.17 Output Voltage (1)

Conditions: 2.7 V ≤ VCC ≤ 3.6 V, 2.7 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, T_a = –40 to +10°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Low-level output voltage	All output ports (except for RIIC, ports P40 to P44, P46, ports PJ6, PJ7)		V_{OL}	—	0.6	V	I_{OL} = 3.0 mA
				—	0.4		I_{OL} = 1.5 mA
	Ports P40 to P44, P46, ports PJ6, PJ7			—	0.4		I_{OL} = 0.4 mA
	RIIC pins	Standard mode		—	0.4		I_{OL} = 3.0 mA
		Fast mode		—	0.6		I_{OL} = 6.0 mA
High-level output voltage	All output ports (except for ports P40 to P44, P46, ports PJ6, PJ7)		V_{OH}	VCC – 0.5	—	V	I_{OH} = –2.0 mA
	Ports P40 to P44, P46, ports PJ6, PJ7			AVCC0 – 0.5	—		I_{OH} = –0.1 mA

Table 5.18 Output Voltage (2)

Conditions: 1.8 V ≤ VCC ≤ 2.7 V, 1.8 V ≤ AVCC0 ≤ 2.7 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Max.	Unit	Test Conditions
Low-level output voltage	All output ports (except for ports P40 to P44, P46, ports PJ6, PJ7)	V_{OL}	—	0.6	V	I_{OL} = 1.5 mA
	Ports P40 to P44, P46, ports PJ6, PJ7		—	0.4		I_{OL} = 0.4 mA
High-level output voltage	All output ports (except for ports P40 to P44, P46, ports PJ6, PJ7)	V_{OH}	VCC – 0.5	—	V	I_{OH} = –1.0 mA
	Ports P40 to P44, P46, ports PJ6, PJ7		AVCC0 – 0.5	—		I_{OH} = –0.1 mA

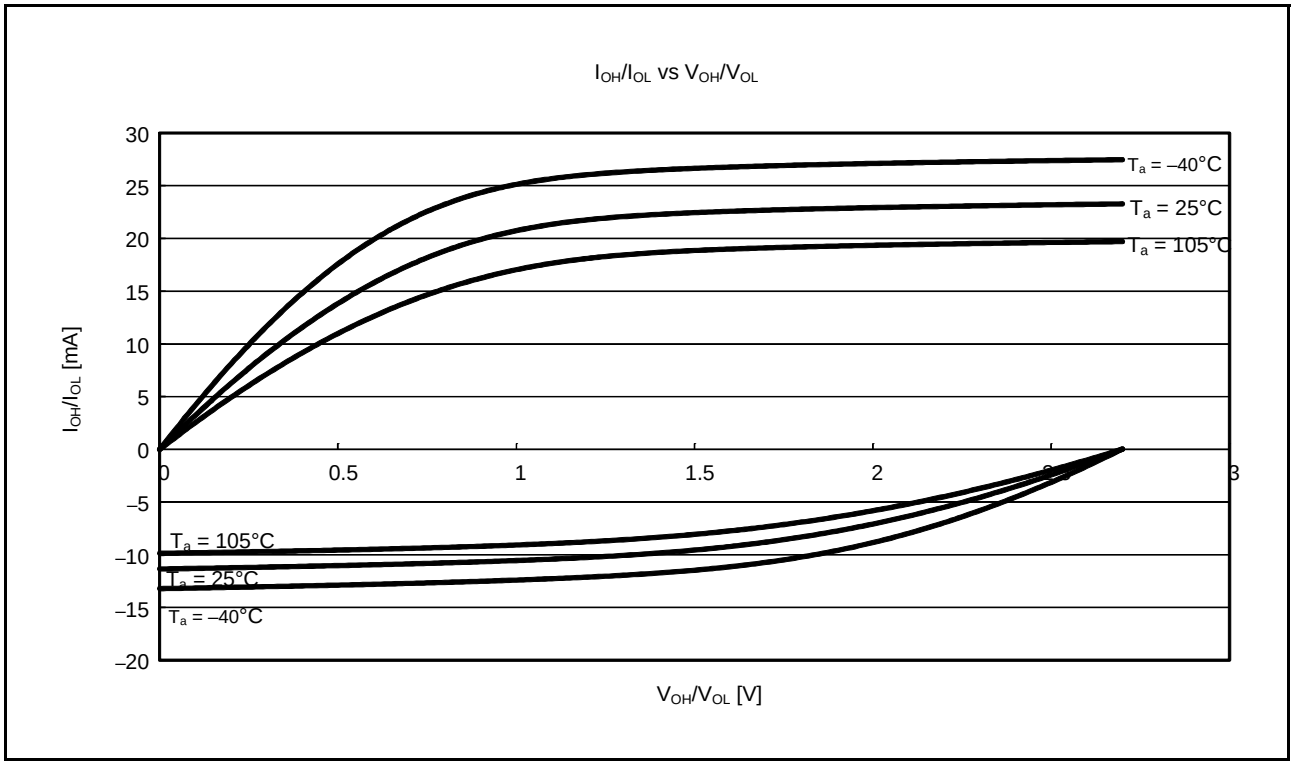


Figure 5.9 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of General Ports (Except for the RIIC Output Pin, Ports P40 to P44, P46, Ports PJ6, PJ7) at VCC = 2.7 V (Reference Data)

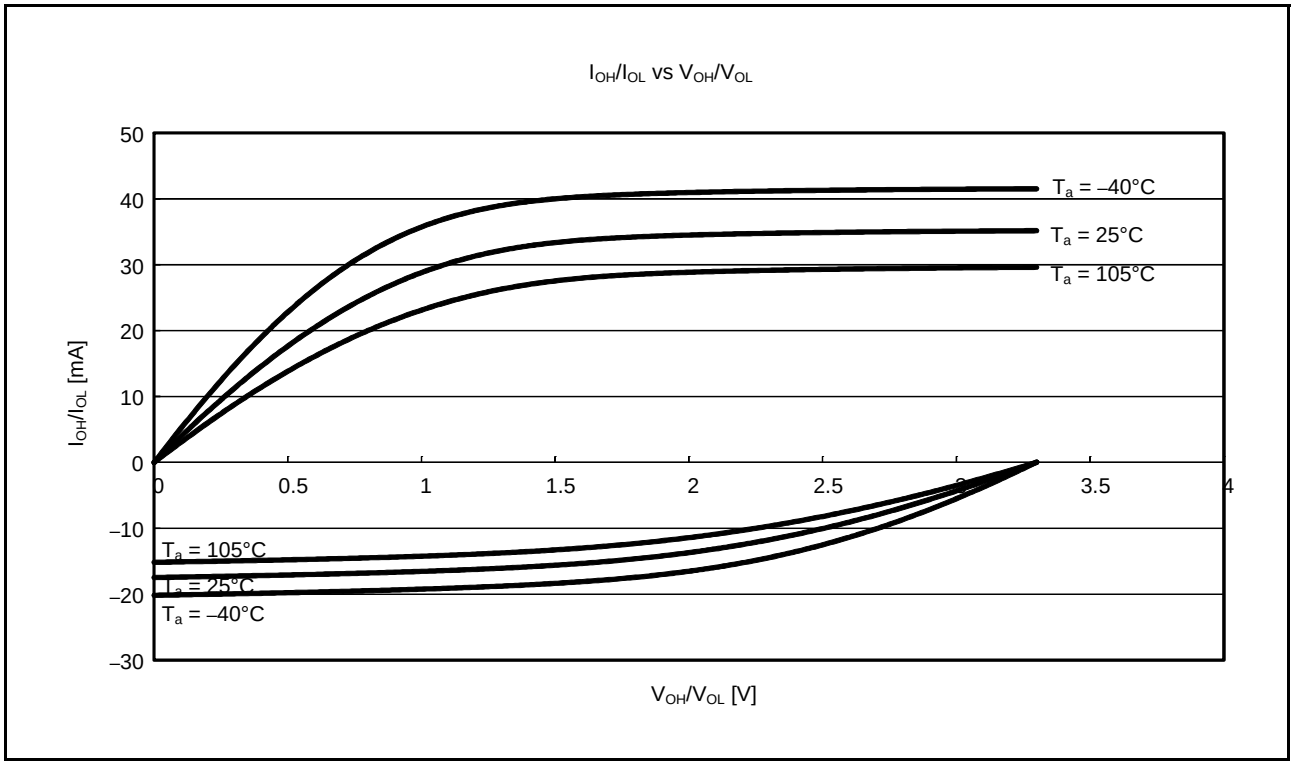


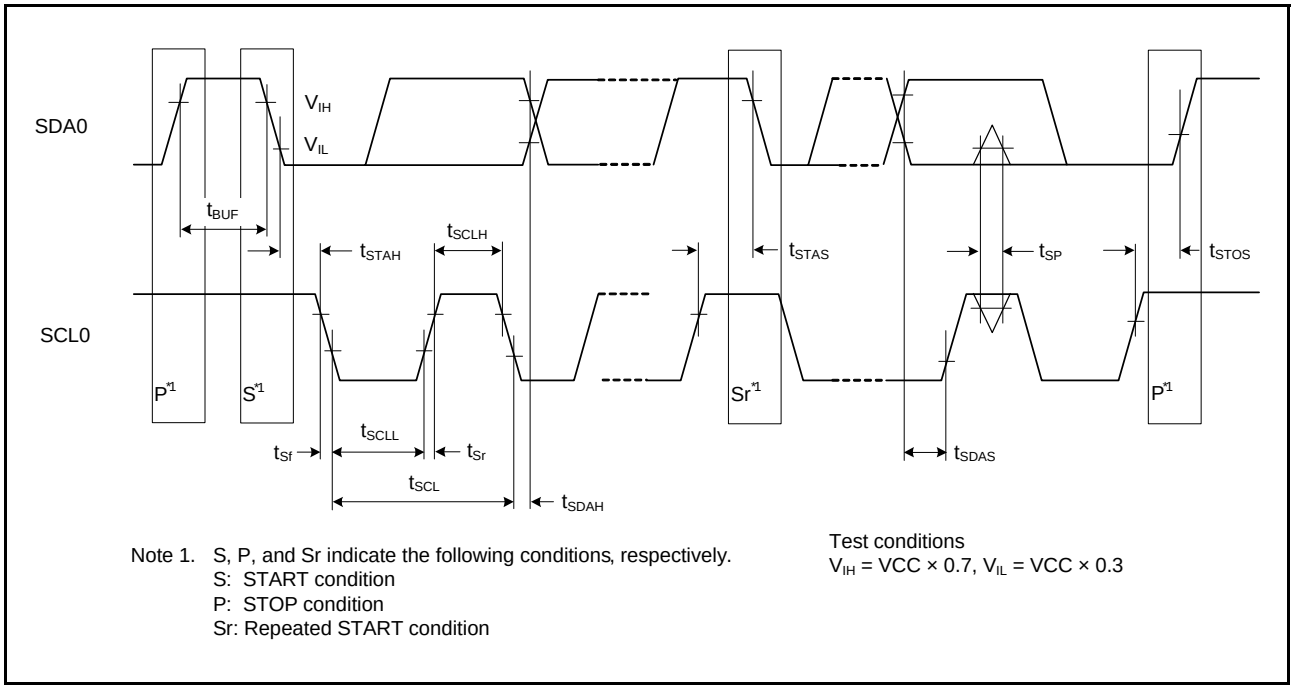
Figure 5.10 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of General Ports (Except for the RIIC Output Pin, Ports P40 to P44, P46, Ports PJ6, PJ7) at VCC = 3.3 V (Reference Data)

Table 5.32 Timing of On-Chip Peripheral Modules (3)

Conditions: 1.8 V ≤ VCC ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C, C = 30 pF

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 5.39
	SCK clock cycle input (slave)			6	65536		
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time (master)	2.7 V or above	t_{SU}	65	—	ns	Figure 5.40, Figure 5.42
		1.8 V or above		95	—		
	Data input setup time (slave)			40	—		
	Data input hold time		t_H	40	—	ns	
	SS input setup time		t_{LEAD}	3	—	t_{Pcyc}	
	SS input hold time		t_{LAG}	3	—	t_{Pcyc}	
	Data output delay time (master)		t_{OD}	—	40	ns	
	Data output delay time (slave)	2.7 V or above		—	65		
		1.8 V or above		—	85		
	Data output hold time (master)	2.7 V or above	t_{OH}	–10	—	ns	
		1.8 V or above		–20	—		
	Data output hold time (slave)			–10	—		
	Data rise/fall time		t_{Dr}, t_{Df}	—	20	ns	
	SS input rise/fall time		t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time		t_{SA}	—	6	t_{Pcyc}	Figure 5.44, Figure 5.45
	Slave output release time		t_{REL}	—	6	t_{Pcyc}	

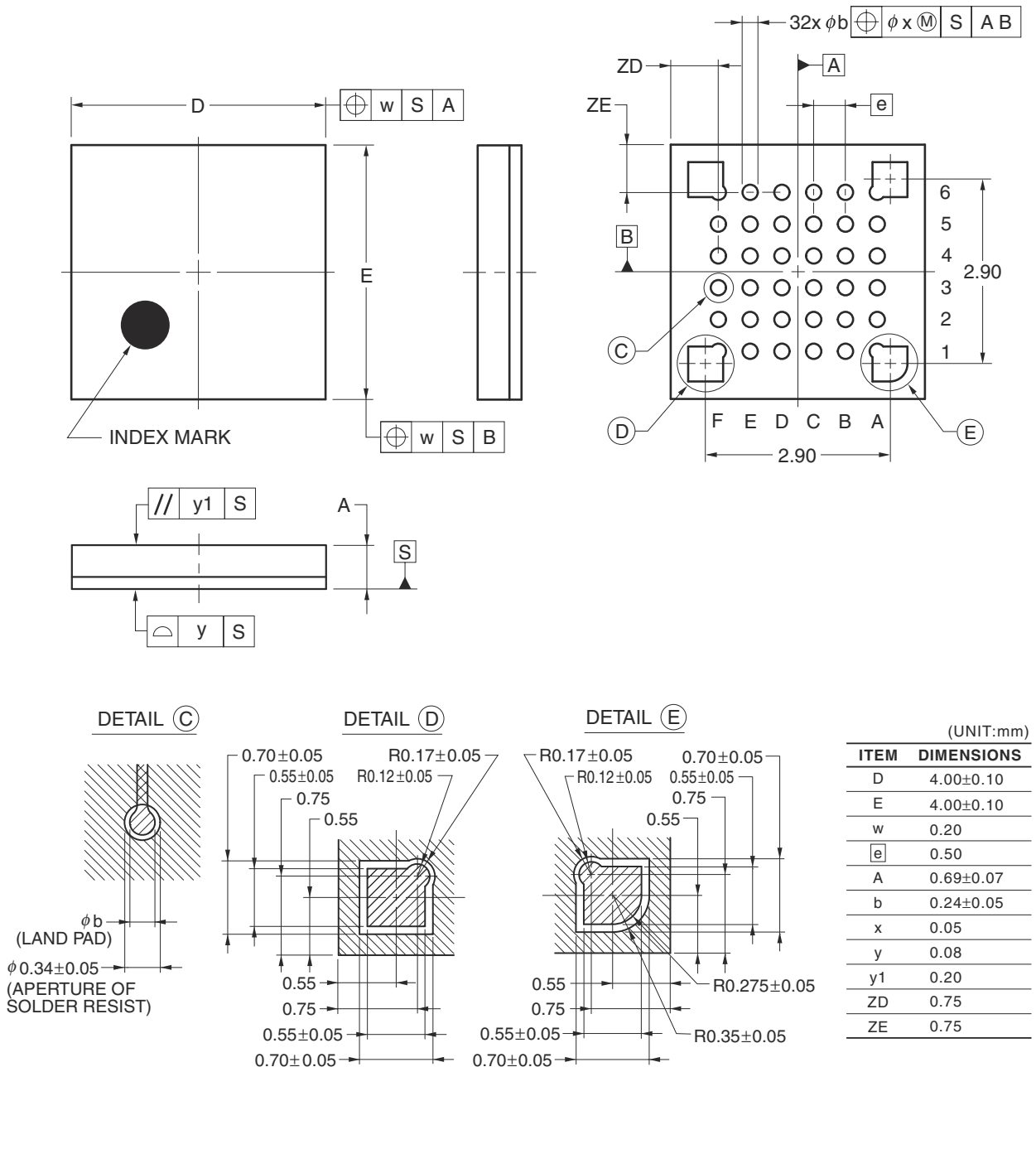
Note 1. t_{Pcyc}: PCLK cycle



Note 1. S, P, and Sr indicate the following conditions, respectively.
S: START condition
P: STOP condition
Sr: Repeated START condition

Figure 5.46 RIIC Bus Interface Input/Output Timing and Simple I²C Bus Interface Input/Output Timing

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-WFLGA36-4x4-0.50	PWLG0036KA-A	P36FC-50-AA4-2	0.023



(UNIT:mm)

ITEM	DIMENSIONS
D	4.00±0.10
E	4.00±0.10
w	0.20
e	0.50
A	0.69±0.07
b	0.24±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.75
ZE	0.75

Figure G 36-Pin WFLGA (PWLG0036KA-A)

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.20	Jul 29, 2016	1. Overview		
		18 to 25	Table 1.5 to 1.9 Note 1 regarding I/O power source is AVCC0 for the ports (P4, PJ6, and PJ7), added	
		5. Electrical Characteristics		
		45	Table 5.1 Absolute Maximum Ratings, Analog power supply voltage added	
		45	Table 5.2 Recommended Operating Conditions, VREFH0 / VREFL0 added	
		51	Table 5.8 DC Characteristics (6), Increment for IWDT operation added	
		52	Table 5.9 DC Characteristics (7) Permissible total consumption power added	TN-RX*-A135A/E
		53	Table 5.10 DC Characteristics (8), LDV1,2 added	
		54, 55	Table 5.15 Permissible Output Currents is divided into D version and G version	
		93	Table 5.45 ROM (Flash Memory for Code Storage) Characteristics (2), Erasure time - 128-Kbyte added	TN-RX*-A132A/E
		94	Table 5.46 ROM (Flash Memory for Code Storage) Characteristics (3), Temperature range for the programming/erasure operation changed and Erasure time - 128-Kbyte added	TN-RX*-A132A/E
		95, 96	5.9 Usage Notes added	