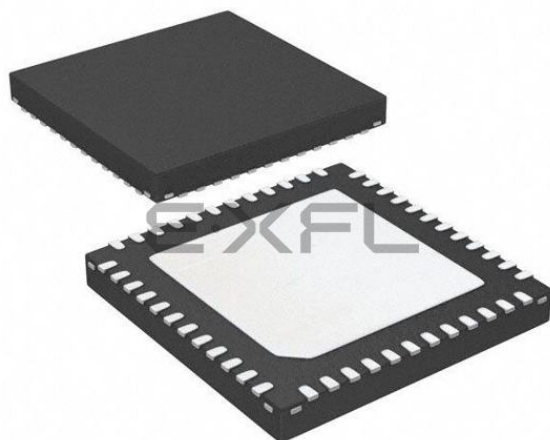




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Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-WFQFN Exposed Pad
Supplier Device Package	48-HWQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5110jadne-u0

Table 1.4 Pin Functions (2/3)

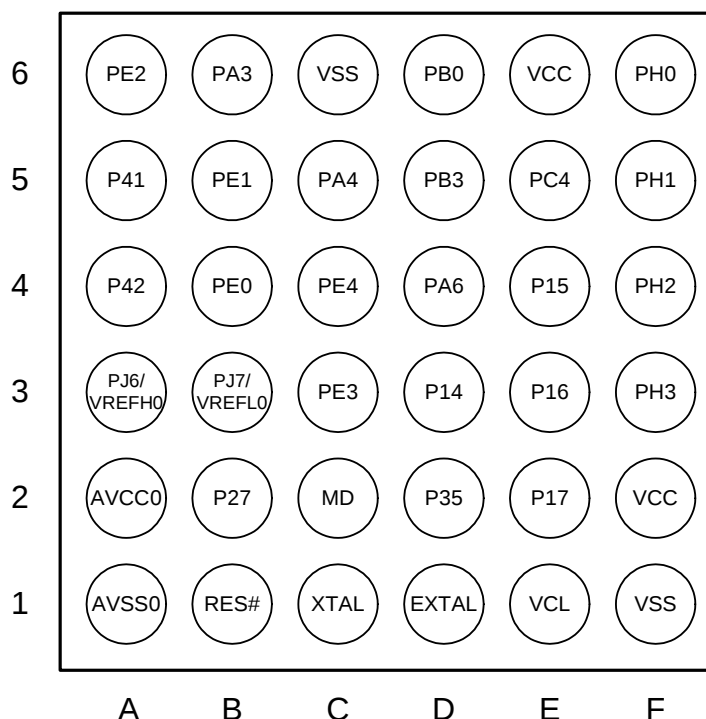
Classifications	Pin Name	I/O	Description
Serial communications interface (SCIe)	• Simple I ² C mode		
	SSCL1, SSCL5	I/O	Input/output pins for the I ² C clock.
	SSDA1, SSDA5	I/O	Input/output pins for the I ² C data.
	• Simple SPI mode		
	SCK1, SCK5	I/O	Input/output pins for the clock.
	SMISO1, SMISO5	I/O	Input/output pins for slave transmit data.
	SMOSI1, SMOSI5	I/O	Input/output pins for master transmit data.
	SS1#, SS5#	Input	Chip-select input pins.
Serial communications interface (SCI _f)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock.
	RXD12	Input	Input pin for receiving data.
	TXD12	Output	Output pin for transmitting data.
	CTS12#	Input	Input pin for controlling the start of transmission and reception.
	RTS12#	Output	Output pin for controlling the start of transmission and reception.
	• Simple I ² C mode		
	SSCL12	I/O	Input/output pin for the I ² C clock.
	SSDA12	I/O	Input/output pin for the I ² C data.
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock.
	SMISO12	I/O	Input/output pin for slave transmit data.
	SMOSI12	I/O	Input/output pin for master transmit data.
	SS12#	Input	Chip-select input pin.
	• Extended serial mode		
	RXDX12	Input	Input pin for data reception by SCI _f .
	TXDX12	Output	Output pin for data transmission by SCI _f .
	SIOX12	I/O	Input/output pin for data reception or transmission by SCI _f .
I ² C bus interface	SCL0	I/O	Input/output pin for I ² C bus interface clocks. Bus can be directly driven by the N-channel open drain output.
	SDA0	I/O	Input/output pin for I ² C bus interface data. Bus can be directly driven by the N-channel open drain output.
Serial peripheral interface	RSPCKA	I/O	Input/output pin for the RSPI clock.
	MOSIA	I/O	Input/output pin for transmitting data from the RSPI master.
	MISOA	I/O	Input/output pin for transmitting data from the RSPI slave.
	SSLA0	I/O	Input/output pin to select the slave for the RSPI.
	SSLA1 to SSLA3	Output	Output pins to select the slave for the RSPI.
12-bit A/D converter	AN000 to AN004, AN006, AN008 to AN015	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0#	Input	Input pin for the external trigger signals that start the A/D conversion.
I/O ports	P03, P05	I/O	2-bit input/output pins.
	P14 to P17	I/O	4-bit input/output pins.
	P26, P27	I/O	2-bit input/output pins.
	P30 to P32, P35	I/O	4-bit input/output pins (P35 input pin).
	P40 to P44, P46	I/O	6-bit input/output pins.
	P54, P55	I/O	2-bit input/output pins.
	PA0, PA1, PA3, PA4, PA6	I/O	5-bit input/output pins.
	PB0, PB1, PB3, PB5 to PB7	I/O	6-bit input/output pins.

Table 1.4 Pin Functions (3/3)

Classifications	Pin Name	I/O	Description
I/O ports	PC0 to PC7	I/O	8-bit input/output pins.
	PE0 to PE7	I/O	8-bit input/output pins.
	PH0 to PH3	I/O	4-bit input/output pins.
	PH7	Input	1-bit input pin.
	PJ6, PJ7	I/O	2-bit input/output pins.

Note 1. For external clock input.

RX110 Group
PWLG0036KA-A
(36-pin WFLGA)
(Upper perspective view)



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table "List of Pins and Pin Functions (36-Pin WFLGA)".

Note: For the position of A1 pin in the package, see "Package Dimensions".

Figure 1.7 Pin Assignments of the 36-Pin WFLGA

Table 1.7 List of Pins and Pin Functions (48-Pin LQFP/HWQFN) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, RTC)	Communication (SCIE, SCIF, RSPI, RIIC)	Others
1		P27	MTIOC2B	SCK1/SCK12	IRQ3/CMPA2/CACREF/ADTRG0#
2		P26	MTIOC2A	TXD1/SMOSI1/SSDA1	
3	MD				FINED
4	RES#				
5	XCOUT				
6	XCIN	PH7			
7		P35			NMI
8	XTAL				
9	EXTAL				
10	VCL				
11	VSS				
12	VCC				
13		P17	MTIOC0C	SCK1/MISOA/SDA0/RXD12/RXD12/SMISO12/SSCL12	IRQ7
14		P16	RTCOUT	TXD1/SMOSI1/SSDA1/MOSIA/SCL0	IRQ6/ADTRG0#
15		P15	MTIOC0B/MTCLKB	RXD1/SMISO1/SSCL1/RSPCKA	IRQ5/CLKOUT
16		P14	MTIOC0A/MTCLKA	CTS1#/RTS1#/SS1#/SSLA0/TXD12/TXD12/SIOX12/SMOSI12/SSDA12	IRQ4
17		PH3	MTIOC1A		
18		PH2			IRQ1
19		PH1			IRQ0
20		PH0	MTIOC1B		CACREF
21		PC7	MTCLKB	TXD1/SMOSI1/SSDA1/MISOA	CACREF
22		PC6	MTCLKA	RXD1/SMISO1/SSCL1/MOSIA	
23		PC5	MTCLKD	SCK1/RSPCKA	
24		PC4	MTCLKC	SCK5/SSLA0	IRQ2/CLKOUT
25		PB5/PC3	MTIOC2A/MTIOC1B		
26		PB3/PC2	MTIOC0A		
27		PB1/PC1	MTIOC0C		IRQ4
28	VCC				
29		PB0/PC0	MTIC5W/MTIOC0C/RTCOUT	SCL0/RSPCKA	IRQ2/ADTRG0#
30	VSS				
31		PA6	MTIC5V/MTCLKB/MTIOC2A	CTS5#/RTS5#/SS5#/SDA0/MOSIA	IRQ3
32		PA4	MTIC5U/MTCLKA/MTIOC2B	TXD5/SMOSI5/SSDA5/SSLA0	IRQ5
33		PA3	MTIOC0D/MTCLKD/MTIOC1B	RXD5/SMISO5/SSCL5/MISOA	IRQ6
34		PA1	MTIOC0B/MTCLKC/RTCOUT	SCK5/SSLA2	
35		PE4	MTIOC1A	MOSIA	IRQ4/AN012
36		PE3	MTIOC0A/MTIOC1B	CTS12#/RTS12#/SS12#/RSPCKA	IRQ3/AN011
37		PE2		RXD12/RXD12/SMISO12/SSCL12	IRQ7/AN010
38		PE1		TXD12/TXD12/SIOX12/SMOSI12/SSDA12	IRQ1/AN009
39		PE0	MTIOC2A	SCK12	IRQ0/AN008
40		PE7			IRQ7/AN015
41		P46*1			AN006
42		P42*1			AN002
43		P41*1			AN001
44	VREFL0	PJ7*1			

Table 4.1 List of I/O Registers (Address Order) (5/13)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 73DEh	ICU	Interrupt Source Priority Register 222	IPR222	8	8	2 ICLK
0008 73EEh	ICU	Interrupt Source Priority Register 238	IPR238	8	8	2 ICLK
0008 73F2h	ICU	Interrupt Source Priority Register 242	IPR242	8	8	2 ICLK
0008 73F3h	ICU	Interrupt Source Priority Register 243	IPR243	8	8	2 ICLK
0008 73F4h	ICU	Interrupt Source Priority Register 244	IPR244	8	8	2 ICLK
0008 73F5h	ICU	Interrupt Source Priority Register 245	IPR245	8	8	2 ICLK
0008 73F6h	ICU	Interrupt Source Priority Register 246	IPR246	8	8	2 ICLK
0008 73F7h	ICU	Interrupt Source Priority Register 247	IPR247	8	8	2 ICLK
0008 73F8h	ICU	Interrupt Source Priority Register 248	IPR248	8	8	2 ICLK
0008 73F9h	ICU	Interrupt Source Priority Register 249	IPR249	8	8	2 ICLK
0008 7500h	ICU	IRQ Control Register 0	IRQCR0	8	8	2 ICLK
0008 7501h	ICU	IRQ Control Register 1	IRQCR1	8	8	2 ICLK
0008 7502h	ICU	IRQ Control Register 2	IRQCR2	8	8	2 ICLK
0008 7503h	ICU	IRQ Control Register 3	IRQCR3	8	8	2 ICLK
0008 7504h	ICU	IRQ Control Register 4	IRQCR4	8	8	2 ICLK
0008 7505h	ICU	IRQ Control Register 5	IRQCR5	8	8	2 ICLK
0008 7506h	ICU	IRQ Control Register 6	IRQCR6	8	8	2 ICLK
0008 7507h	ICU	IRQ Control Register 7	IRQCR7	8	8	2 ICLK
0008 7510h	ICU	IRQ Pin Digital Filter Enable Register 0	IRQFLTE0	8	8	2 ICLK
0008 7514h	ICU	IRQ Pin Digital Filter Setting Register 0	IRQFLTC0	16	16	2 ICLK
0008 7580h	ICU	Non-Maskable Interrupt Status Register	NMISR	8	8	2 ICLK
0008 7581h	ICU	Non-Maskable Interrupt Enable Register	NMIER	8	8	2 ICLK
0008 7582h	ICU	Non-Maskable Interrupt Status Clear Register	NMICLR	8	8	2 ICLK
0008 7583h	ICU	NMI Pin Interrupt Control Register	NMICR	8	8	2 ICLK
0008 7590h	ICU	NMI Pin Digital Filter Enable Register	NMIFLTE	8	8	2 ICLK
0008 7594h	ICU	NMI Pin Digital Filter Setting Register	NMIFLTC	8	8	2 ICLK
0008 8000h	CMT	Compare Match Timer Start Register 0	CMSTR0	16	16	2 or 3 PCLKB
0008 8002h	CMT0	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB
0008 8004h	CMT0	Compare Match Timer Counter	CMCNT	16	16	2 or 3 PCLKB
0008 8006h	CMT0	Compare Match Timer Constant Register	CMCOR	16	16	2 or 3 PCLKB
0008 8008h	CMT1	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB
0008 800Ah	CMT1	Compare Match Timer Counter	CMCNT	16	16	2 or 3 PCLKB
0008 800Ch	CMT1	Compare Match Timer Constant Register	CMCOR	16	16	2 or 3 PCLKB
0008 8030h	IWDT	IWDT Refresh Register	IWDTRR	8	8	2 or 3 PCLKB
0008 8032h	IWDT	IWDT Control Register	IWDTCR	16	16	2 or 3 PCLKB
0008 8034h	IWDT	IWDT Status Register	IWDTSR	16	16	2 or 3 PCLKB
0008 8036h	IWDT	IWDT Reset Control Register	IWDTRCR	8	8	2 or 3 PCLKB
0008 8038h	IWDT	IWDT Count Stop Control Register	IWDTCSTPR	8	8	2 or 3 PCLKB
0008 8280h	CRC	CRC Control Register	CRCCR	8	8	2 or 3 PCLKB
0008 8281h	CRC	CRC Data Input Register	CRCDIR	8	8	2 or 3 PCLKB
0008 8282h	CRC	CRC Data Output Register	CRCDOR	16	16	2 or 3 PCLKB
0008 8300h	RIIC0	I ² C Bus Control Register 1	ICCR1	8	8	2 or 3 PCLKB
0008 8301h	RIIC0	I ² C Bus Control Register 2	ICCR2	8	8	2 or 3 PCLKB
0008 8302h	RIIC0	I ² C Bus Mode Register 1	ICMR1	8	8	2 or 3 PCLKB
0008 8303h	RIIC0	I ² C Bus Mode Register 2	ICMR2	8	8	2 or 3 PCLKB
0008 8304h	RIIC0	I ² C Bus Mode Register 3	ICMR3	8	8	2 or 3 PCLKB
0008 8305h	RIIC0	I ² C Bus Function Enable Register	ICFER	8	8	2 or 3 PCLKB
0008 8306h	RIIC0	I ² C Bus Status Enable Register	ICSER	8	8	2 or 3 PCLKB
0008 8307h	RIIC0	I ² C Bus Interrupt Enable Register	ICIER	8	8	2 or 3 PCLKB
0008 8308h	RIIC0	I ² C Bus Status Register 1	ICSR1	8	8	2 or 3 PCLKB
0008 8309h	RIIC0	I ² C Bus Status Register 2	ICSR2	8	8	2 or 3 PCLKB
0008 830Ah	RIIC0	Slave Address Register L0	SARL0	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (7/13)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 8726h	MTU0	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	2 or 3 PCLKB
0008 8780h	MTU1	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8781h	MTU1	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB
0008 8782h	MTU1	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKB
0008 8784h	MTU1	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 8785h	MTU1	Timer Status Register	TSR	8	8	2 or 3 PCLKB
0008 8786h	MTU1	Timer Counter	TCNT	16	16	2 or 3 PCLKB
0008 8788h	MTU1	Timer General Register A	TGRA	16	16	2 or 3 PCLKB
0008 878Ah	MTU1	Timer General Register B	TGRB	16	16	2 or 3 PCLKB
0008 8790h	MTU1	Timer Input Capture Control Register	TICCR	8	8	2 or 3 PCLKB
0008 8800h	MTU2	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8801h	MTU2	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB
0008 8802h	MTU2	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKB
0008 8804h	MTU2	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 8805h	MTU2	Timer Status Register	TSR	8	8	2 or 3 PCLKB
0008 8806h	MTU2	Timer Counter	TCNT	16	16	2 or 3 PCLKB
0008 8808h	MTU2	Timer General Register A	TGRA	16	16	2 or 3 PCLKB
0008 880Ah	MTU2	Timer General Register B	TGRB	16	16	2 or 3 PCLKB
0008 8880h	MTU5	Timer Counter U	TCNTU	16	16	2 or 3 PCLKB
0008 8882h	MTU5	Timer General Register U	TGRU	16	16	2 or 3 PCLKB
0008 8884h	MTU5	Timer Control Register U	TCRU	8	8	2 or 3 PCLKB
0008 8886h	MTU5	Timer I/O Control Register U	TIORU	8	8	2 or 3 PCLKB
0008 8890h	MTU5	Timer Counter V	TCNTV	16	16	2 or 3 PCLKB
0008 8892h	MTU5	Timer General Register V	TGRV	16	16	2 or 3 PCLKB
0008 8894h	MTU5	Timer Control Register V	TCRV	8	8	2 or 3 PCLKB
0008 8896h	MTU5	Timer I/O Control Register V	TIORV	8	8	2 or 3 PCLKB
0008 88A0h	MTU5	Timer Counter W	TCNTW	16	16	2 or 3 PCLKB
0008 88A2h	MTU5	Timer General Register W	TGRW	16	16	2 or 3 PCLKB
0008 88A4h	MTU5	Timer Control Register W	TCRW	8	8	2 or 3 PCLKB
0008 88A6h	MTU5	Timer I/O Control Register W	TIORW	8	8	2 or 3 PCLKB
0008 88B2h	MTU5	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 88B4h	MTU5	Timer Start Register	TSTR	8	8	2 or 3 PCLKB
0008 88B6h	MTU5	Timer Compare Match Clear Register	TCNTCMPCLR	8	8	2 or 3 PCLKB
0008 9000h	S12AD	A/D Control Register	ADCSR	16	16	2 or 3 PCLKB
0008 9004h	S12AD	A/D Channel Select Register A	ADANSA	16	16	2 or 3 PCLKB
0008 9008h	S12AD	A/D-Converted Value Addition Mode Select Register	ADADS	16	16	2 or 3 PCLKB
0008 900Ch	S12AD	A/D-Converted Value Addition Count Select Register	ADADC	8	8	2 or 3 PCLKB
0008 900Eh	S12AD	A/D Control Extended Register	ADCER	16	16	2 or 3 PCLKB
0008 9010h	S12AD	A/D Start Trigger Select Register	ADSTRGR	16	16	2 or 3 PCLKB
0008 9012h	S12AD	A/D Converted Extended Input Control Register	ADEXICR	16	16	2 or 3 PCLKB
0008 9014h	S12AD	A/D Channel Select Register B	ADANSB	16	16	2 or 3 PCLKB
0008 9018h	S12AD	A/D Data Duplication Register	ADDBLDR	16	16	2 or 3 PCLKB
0008 901Ah	S12AD	A/D Temperature Sensor Data Register	ADTSDR	16	16	2 or 3 PCLKB
0008 901Ch	S12AD	A/D Internal Reference Voltage Data Register	ADOCDR	16	16	2 or 3 PCLKB
0008 9020h	S12AD	A/D Data Register 0	ADDR0	16	16	2 or 3 PCLKB
0008 9022h	S12AD	A/D Data Register 1	ADDR1	16	16	2 or 3 PCLKB
0008 9024h	S12AD	A/D Data Register 2	ADDR2	16	16	2 or 3 PCLKB
0008 9026h	S12AD	A/D Data Register 3	ADDR3	16	16	2 or 3 PCLKB
0008 9028h	S12AD	A/D Data Register 4	ADDR4	16	16	2 or 3 PCLKB
0008 902Ch	S12AD	A/D Data Register 6	ADDR6	16	16	2 or 3 PCLKB
0008 9030h	S12AD	A/D Data Register 8	ADDR8	16	16	2 or 3 PCLKB
0008 9032h	S12AD	A/D Data Register 9	ADDR9	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (10/13)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 C024h	PORT4	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C025h	PORT5	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C02Ah	PORTA	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C02Bh	PORTB	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C02Ch	PORTC	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C02Eh	PORTE	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C031h	PORTH	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C032h	PORTJ	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C040h	PORT0	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C041h	PORT1	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C042h	PORT2	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C043h	PORT3	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C044h	PORT4	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C045h	PORT5	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C04Ah	PORTA	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C04Bh	PORTB	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C04Ch	PORTC	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C04Eh	PORTE	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C051h	PORTH	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C052h	PORTJ	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C060h	PORT0	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C061h	PORT1	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C062h	PORT2	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C063h	PORT3	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C064h	PORT4	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C065h	PORT5	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Ah	PORTA	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Bh	PORTB	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Ch	PORTC	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Eh	PORTE	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C071h	PORTH	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C072h	PORTJ	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C083h	PORT1	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C085h	PORT2	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C086h	PORT3	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C094h	PORTA	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C095h	PORTA	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C096h	PORTB	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C097h	PORTB	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C098h	PORTC	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C099h	PORTC	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C09Ch	PORTE	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C09Dh	PORTE	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C0C0h	PORT0	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C1h	PORT1	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C2h	PORT2	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (12/13)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 C1CAh	MPC	PH2 Pin Function Control Register	PH2PFS	8	8	2 or 3 PCLKB
0008 C1CBh	MPC	PH3 Pin Function Control Register	PH3PFS	8	8	2 or 3 PCLKB
0008 C1D6h	MPC	PJ6 Pin Function Control Register	PJ6PFS	8	8	2 or 3 PCLKB
0008 C1D7h	MPC	PJ7 Pin Function Control Register	PJ7PFS	8	8	2 or 3 PCLKB
0008 C290h	SYSTEM	Reset Status Register 0	RSTSR0	8	8	4 or 5 PCLKB
0008 C291h	SYSTEM	Reset Status Register 1	RSTSR1	8	8	4 or 5 PCLKB
0008 C293h	SYSTEM	Main Clock Oscillator Forced Oscillation Control Register	MOFCR	8	8	4 or 5 PCLKB
0008 C297h	SYSTEM	Voltage Monitoring Circuit Control Register	LVCMPCR	8	8	4 or 5 PCLKB
0008 C298h	SYSTEM	Voltage Detection Level Select Register	LVDLVL	8	8	4 or 5 PCLKB
0008 C29Ah	SYSTEM	Voltage Monitoring 1 Circuit Control Register 0	LVD1CR0	8	8	4 or 5 PCLKB
0008 C29Bh	SYSTEM	Voltage Monitoring 2 Circuit Control Register 0	LVD2CR0	8	8	4 or 5 PCLKB
0008 C400h	RTC	64-Hz Counter	R64CNT	8	8	2 or 3 PCLKB
0008 C402h	RTC	Second Counter	RSECCNT	8	8	2 or 3 PCLKB
0008 C402h	RTC	Binary Counter 0	BCNT0	8	8	2 or 3 PCLKB
0008 C404h	RTC	Minute Counter	RMINCNT	8	8	2 or 3 PCLKB
0008 C404h	RTC	Binary Counter 1	BCNT1	8	8	2 or 3 PCLKB
0008 C406h	RTC	Hour Counter	RHRCNT	8	8	2 or 3 PCLKB
0008 C406h	RTC	Binary Counter 2	BCNT2	8	8	2 or 3 PCLKB
0008 C408h	RTC	Day-Of-Week Counter	RWKCNT	8	8	2 or 3 PCLKB
0008 C408h	RTC	Binary Counter 3	BCNT3	8	8	2 or 3 PCLKB
0008 C40Ah	RTC	Date Counter	RDAYCNT	8	8	2 or 3 PCLKB
0008 C40Ch	RTC	Month Counter	RMONCNT	8	8	2 or 3 PCLKB
0008 C40Eh	RTC	Year Counter	RYRCNT	16	16	2 or 3 PCLKB
0008 C410h	RTC	Second Alarm Register	RSECAR	8	8	2 or 3 PCLKB
0008 C410h	RTC	Binary Counter 0 Alarm Register	BCNT0AR	8	8	2 or 3 PCLKB
0008 C412h	RTC	Minute Alarm Register	RMINAR	8	8	2 or 3 PCLKB
0008 C412h	RTC	Binary Counter 1 Alarm Register	BCNT1AR	8	8	2 or 3 PCLKB
0008 C414h	RTC	Hour Alarm Register	RHRAR	8	8	2 or 3 PCLKB
0008 C414h	RTC	Binary Counter 2 Alarm Register	BCNT2AR	8	8	2 or 3 PCLKB
0008 C416h	RTC	Day-of-Week Alarm Register	RWKAR	8	8	2 or 3 PCLKB
0008 C416h	RTC	Binary Counter 3 Alarm Register	BCNT3AR	8	8	2 or 3 PCLKB
0008 C418h	RTC	Date Alarm Register	RDAYAR	8	8	2 or 3 PCLKB
0008 C418h	RTC	Binary Counter 0 Alarm Enable Register	BCNT0AER	8	8	2 or 3 PCLKB
0008 C41Ah	RTC	Month Alarm Register	RMONAR	8	8	2 or 3 PCLKB
0008 C41Ah	RTC	Binary Counter 1 Alarm Enable Register	BCNT1AER	8	8	2 or 3 PCLKB
0008 C41Ch	RTC	Year Alarm Register	RYRAR	16	16	2 or 3 PCLKB
0008 C41Ch	RTC	Binary Counter 2 Alarm Enable Register	BCNT2AER	16	16	2 or 3 PCLKB
0008 C41Eh	RTC	Year Alarm Enable Register	RYRAREN	8	8	2 or 3 PCLKB
0008 C41Eh	RTC	Binary Counter 3 Alarm Enable Register	BCNT3AER	8	8	2 or 3 PCLKB
0008 C422h	RTC	RTC Control Register 1	RCR1	8	8	2 or 3 PCLKB
0008 C424h	RTC	RTC Control Register 2	RCR2	8	8	2 or 3 PCLKB
0008 C426h	RTC	RTC Control Register 3	RCR3	8	8	2 or 3 PCLKB
0008 C42Eh	RTC	Time Error Adjustment Register	RADJ	8	8	2 or 3 PCLKB
007F C0ACh	TEMPS	Temperature Sensor Calibration Data Register	TSCDRL	8	8	1 or 2 PCLKB
007F C0ADh	TEMPS	Temperature Sensor Calibration Data Register	TSCDRH	8	8	1 or 2 PCLKB
007F C0B0h	FLASH	Flash Start-Up Setting Monitor Register	FSCMR	16	16	2 or 3 FCLK
007F C0B2h	FLASH	Flash Access Window Start Address Monitor	FAWSMR	16	16	2 or 3 FCLK
007F C0B4h	FLASH	Flash Access Window End Address Monitor Register	FAWEMR	16	16	2 or 3 FCLK
007F C0B6h	FLASH	Flash Initial Setting Register	FISR	8	8	2 or 3 FCLK
007F C0B7h	FLASH	Flash Extra Area Control Register	FEXCR	8	8	2 or 3 FCLK
007F C0B8h	FLASH	Flash Error Address Monitor Register L	FEAML	16	16	2 or 3 FCLK
007F C0BAh	FLASH	Flash Error Address Monitor Register H	FEAMH	8	8	2 or 3 FCLK

Table 4.1 List of I/O Registers (Address Order) (13/13)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
007F C0C0h	FLASH	Protection Unlock Register	FPR	8	8	2 or 3 FCLK
007F C0C1h	FLASH	Protection Unlock Status Register	FPSR	8	8	2 or 3 FCLK
007F C0C2h	FLASH	Flash Read Buffer Register L	FRBL	16	16	2 or 3 FCLK
007F C0C4h	FLASH	Flash Read Buffer Register H	FRBH	16	16	2 or 3 FCLK
007F FF80h	FLASH	Flash P/E Mode Control Register	FPMCR	8	8	2 or 3 FCLK
007F FF81h	FLASH	Flash Area Select Register	FASR	8	8	2 or 3 FCLK
007F FF82h	FLASH	Flash Processing Start Address Register L	FSARL	16	16	2 or 3 FCLK
007F FF84h	FLASH	Flash Processing Start Address Register H	FSARH	8	8	2 or 3 FCLK
007F FF85h	FLASH	Flash Control Register	FCR	8	8	2 or 3 FCLK
007F FF86h	FLASH	Flash Processing End Address Register L	FEARL	16	16	2 or 3 FCLK
007F FF88h	FLASH	Flash Processing End Address Register H	FEARH	8	8	2 or 3 FCLK
007F FF89h	FLASH	Flash Reset Register	FRESETR	8	8	2 or 3 FCLK
007F FF8Ah	FLASH	Flash Status Register 0	FSTATR0	8	8	2 or 3 FCLK
007F FF8Bh	FLASH	Flash Status Register 1	FSTATR1	8	8	2 or 3 FCLK
007F FF8Ch	FLASH	Flash Write Buffer Register L	FWBL	16	16	2 or 3 FCLK
007F FF8Eh	FLASH	Flash Write Buffer Register H	FWBH	16	16	2 or 3 FCLK
007F FFB2h	FLASH	Flash P/E Mode Entry Register	FENTRYR	16	16	2 or 3 FCLK

Note 1. Odd addresses cannot be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMOCNLT register. Table 24.6 lists register allocation for 16-bit access in the User's Manual: Hardware.

Table 5.4 DC Characteristics (2)Conditions: $1.8\text{ V} \leq \text{VCC} < 2.7\text{ V}$, $1.8\text{ V} \leq \text{AVCC0} < 2.7\text{ V}$, $\text{VSS} = \text{AVSS0} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	Ports P16, P17, port PA6, port PB0 (5 V tolerant)	V_{IH}	$\text{VCC} \times 0.8$	—	5.8	V
	Ports P03, P05, ports P14, P15, ports P26, P27, ports P30 to P32, P35, ports P54, P55, ports PA0, PA1, PA3, PA4, ports PB1, PB3, PB5 to PB7, ports PC0 to PC7, ports PE0 to PE7, ports PH0 to PH3, PH7, RES#	V_{IH}	$\text{VCC} \times 0.8$	—	$\text{VCC} + 0.3$	
	All pins		-0.3	—	$\text{VCC} \times 0.2$	
	All pins	ΔV_T	$\text{VCC} \times 0.01$	—	—	
Input voltage (except for Schmitt trigger input pins)	MD	V_{IH}	$\text{VCC} \times 0.9$	—	$\text{VCC} + 0.3$	V
	XTAL (external clock input)	V_{IH}	$\text{VCC} \times 0.8$	—	$\text{VCC} + 0.3$	
	Ports P40 to P44, P46, ports PJ6, PJ7	V_{IH}	$\text{AVCC0} \times 0.7$	—	$\text{AVCC0} + 0.3$	
	MD	V_{IL}	-0.3	—	$\text{VCC} \times 0.1$	
	XTAL (external clock input)	V_{IL}	-0.3	—	$\text{VCC} \times 0.2$	
	Ports P40 to P44, P46, ports PJ6, PJ7	V_{IL}	-0.3	—	$\text{AVCC0} \times 0.3$	

Table 5.5 DC Characteristics (3)Conditions: $1.8\text{ V} \leq \text{VCC} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVCC0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	RES#, MD, port P35, port PH7	$ I_{\text{in}} $	—	1.0	μA	$V_{\text{in}} = 0\text{ V}$, VCC
Three-state leakage current (off-state)	Ports for 5 V tolerant	$ I_{\text{TSI}} $	—	1.0	μA	$V_{\text{in}} = 0\text{ V}$, 5.8 V
	Pins other than above	$ I_{\text{TSI}} $	—	1.0	μA	$V_{\text{in}} = 0\text{ V}$, VCC
Input capacitance	All input pins (except for port P16, port P35)	C_{in}	—	15	pF	$V_{\text{in}} = 0\text{ mV}$, Frequency: 1 MHz, $T_a = 25^\circ\text{C}$
	Port P16, port P35	C_{in}	—	30	pF	

Table 5.6 DC Characteristics (4)Conditions: $1.8\text{ V} \leq \text{VCC} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVCC0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input pull-up resistor	All ports (except for port P35, port PH7)	R_{U}	10	20	100	k Ω , $V_{\text{in}} = 0\text{ V}$

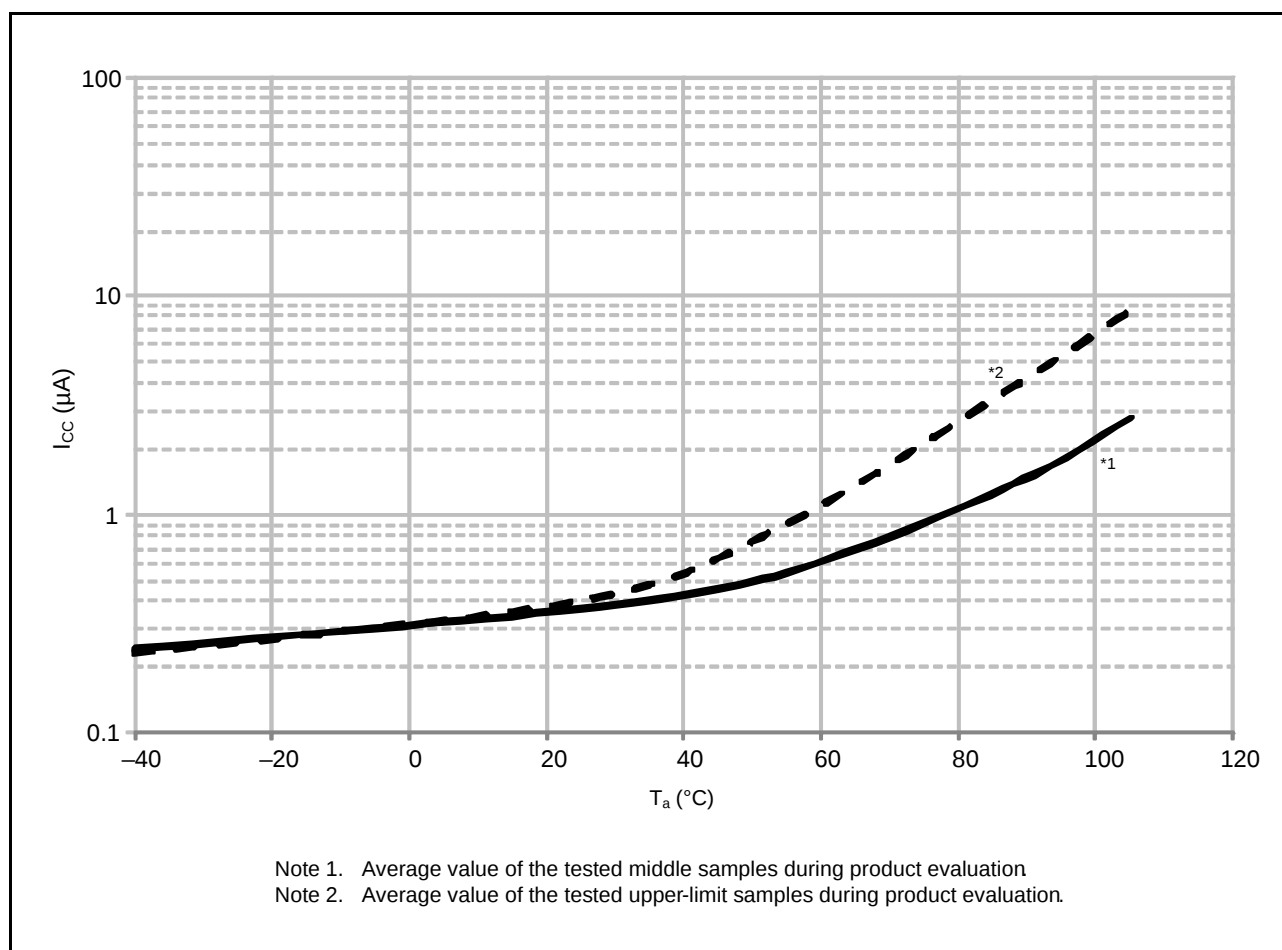


Figure 5.5 Temperature Dependency in Software Standby Mode (Reference Data)

Table 5.9 DC Characteristics (7)

Conditions: $1.8\text{ V} \leq V_{CC} \leq 3.6\text{ V}$, $1.8\text{ V} \leq AV_{CC0} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS0} = 0\text{ V}$

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Permissible total consumption power*1	Pd	—	300	mW	D version ($T_a = -40\text{ to }85^\circ\text{C}$)
		—	105		G version ($T_a = -40\text{ to }105^\circ\text{C}$)*2

Note 1. Total power dissipated by the entire chip (including output currents).

Note 2. Please contact Renesas Electronics sales office for derating under $T_a = +85^\circ\text{C}$ to 105°C . Derating is the systematic reduction of load for the sake of improved reliability.

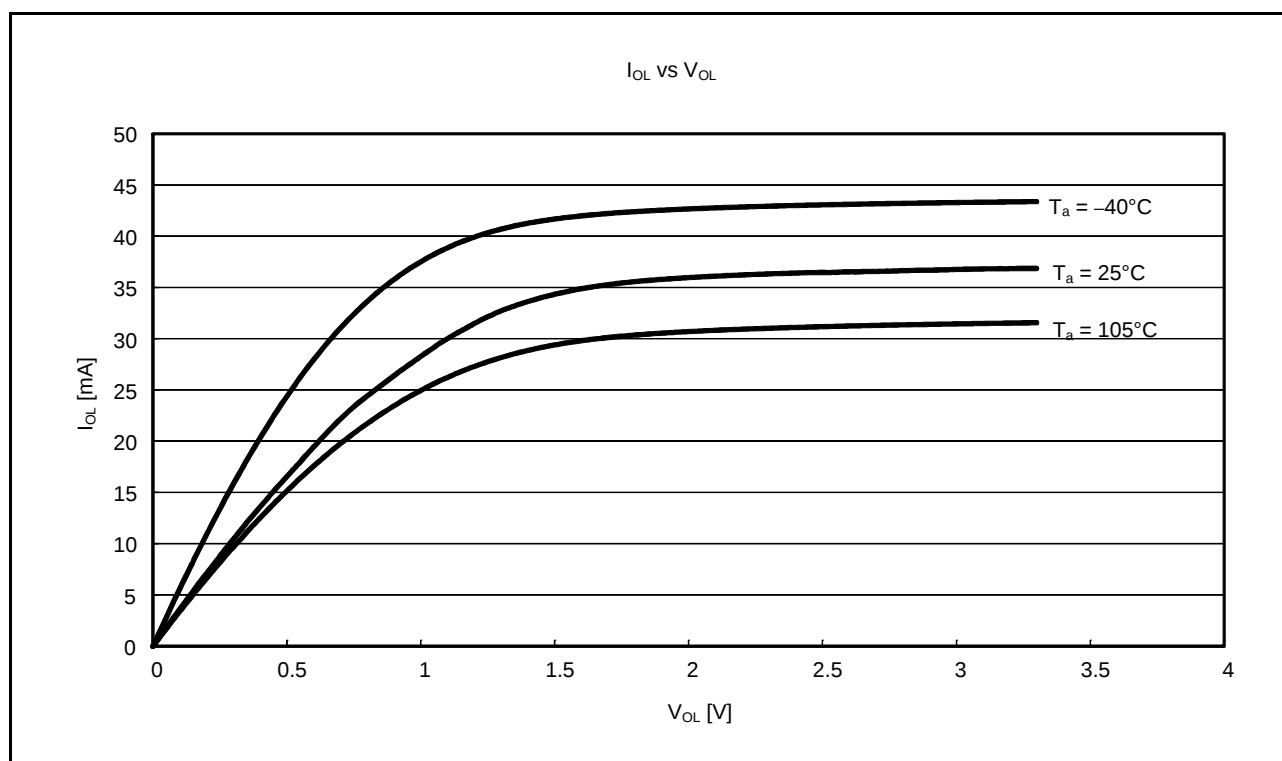


Figure 5.13 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at $V_{CC} = 3.3$ V (Reference Data)

5.3.3 Timing of Recovery from Low Power Consumption Modes

Table 5.24 Timing of Recovery from Low Power Consumption Modes (1)

Conditions: $1.8\text{ V} \leq \text{VCC} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVCC0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	High-speed mode	Crystal connected to main clock oscillator	Main clock oscillator operating*2	t_{SBYMC}	—	2	3	ms	Figure 5.28
		External clock input to main clock oscillator	Main clock oscillator operating*3	t_{SBYEX}	—	35	50	μs	
		Sub-clock oscillator operating		t_{SBYSC}	—	650	800	μs	
		HOCO clock oscillator operating*4		t_{SBYHO}	—	40	55	μs	
		LOCO clock oscillator operating		t_{SBYLO}	—	40	55	μs	

Note: When the division ratios of PCLKB, PCLKD, FCLK, and ICLK are all set to 1.

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. The recovery time when multiple oscillators are operating varies depending on the operating state of the oscillators that are not selected as the system clock source. This applies when only the oscillator listed in each item is operating and the other oscillators are stopped.

Note 2. When the frequency of the crystal is 20 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.

Note 3. When the frequency of the external clock is 20 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.

Note 4. When the frequency of HOCO is 32 MHz.

When the high-speed clock oscillator wait control register (HOCOWTCR) is set to 05h.

Table 5.25 Timing of Recovery from Low Power Consumption Modes (2)

Conditions: $1.8\text{ V} \leq \text{VCC} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVCC0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	Middle-speed mode	Crystal connected to main clock oscillator	Main clock oscillator operating*2	t_{SBYMC}	—	2	3	ms	Figure 5.28
		External clock input to main clock oscillator	Main clock oscillator operating*3	t_{SBYEX}	—	3	4	μs	
		Sub-clock oscillator operating		t_{SBYSC}	—	600	750	μs	
		HOCO clock oscillator operating*4		t_{SBYHO}	—	40	50	μs	
		LOCO clock oscillator operating		t_{SBYLO}	—	4.8	7	μs	

Note: When the division ratios of PCLKB, PCLKD, FCLK, and ICLK are all set to 1.

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. The recovery time when multiple oscillators are operating varies depending on the operating state of the oscillators that are not selected as the system clock source. This applies when only the oscillator listed in each item is operating and the other oscillators are stopped.

Note 2. When the frequency of the crystal is 12 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.

Note 3. When the frequency of the external clock is 12 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.

Note 4. When the frequency of HOCO is 8 MHz.

When the high-speed clock oscillator wait control register (HOCOWTCR) is set to 05h.

Table 5.27 Timing of Recovery from Low Power Consumption Modes (4)Conditions: $1.8\text{ V} \leq V_{CC} \leq 3.6\text{ V}$, $1.8\text{ V} \leq AV_{CC0} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS0} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from deep sleep mode*1	High-speed mode*2	$t_{DSL P}$	—	2	μs	
	Middle-speed mode*3	$t_{DSL P}$	—	3	μs	
	Low-speed mode*4	$t_{DSL P}$	—	400	μs	

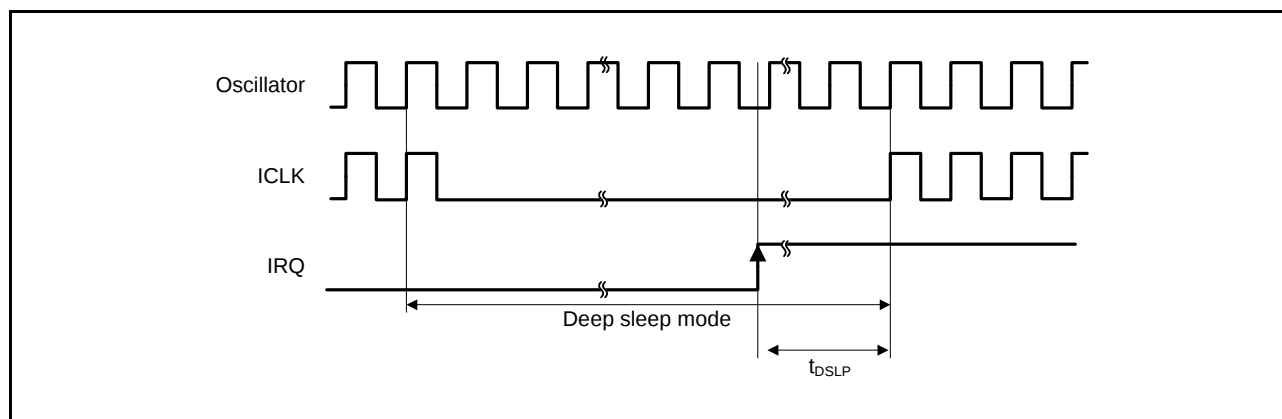
Note: When the division ratios of PCLKB, PCLKD, FCLK, and ICLK are all set to 1.

Note 1. Oscillators continue oscillating in deep sleep mode.

Note 2. When the frequency of the system clock is 32 MHz.

Note 3. When the frequency of the system clock is 12 MHz.

Note 4. When the frequency of the system clock is 32.768 kHz.

**Figure 5.29 Deep Sleep Mode Cancellation Timing****Table 5.28 Timing of Recovery from Low Power Consumption Modes (5)
Operating Mode Transition Time**Conditions: $1.8\text{ V} \leq V_{CC} \leq 3.6\text{ V}$, $1.8\text{ V} \leq AV_{CC0} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS0} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Mode before Transition	Mode after Transition	ICLK Frequency	Transition Time			Unit
			Min.	Typ.	Max.	
High-speed operating mode	Middle-speed operating mode	8 MHz	—	10	—	μs
Middle-speed operating mode	High-speed operating mode	8 MHz	—	37.5	—	μs
Low-speed operating mode	Middle-speed operating mode, high-speed operating mode	32.768 kHz	—	213.62	—	μs
Middle-speed operating mode, high-speed operating mode	Low-speed operating mode	32.768 kHz	—	183.11	—	μs

Note: When the division ratios of PCLKB, PCLKD, FCLK, and ICLK are all set to 1.

5.3.5 Timing of On-Chip Peripheral Modules

Table 5.30 Timing of On-Chip Peripheral Modules (1)Conditions: $1.8\text{ V} \leq V_{CC} \leq 3.6\text{ V}$, $1.8\text{ V} \leq AV_{CC0} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS0} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item			Symbol	Min.	Max.	Unit*1	Test Conditions	
I/O ports	Input data pulse width		t _{PRW}	1.5	—	t _{Pcyc}	Figure 5.32	
MTU2	Input capture input pulse width	Single-edge setting	t _{TICW}	1.5	—	t _{Pcyc}	Figure 5.33	
		Both-edge setting		2.5	—			
	Timer clock pulse width	Single-edge setting	t _{TCKWH} , t _{TCKWL}	1.5	—	t _{Pcyc}	Figure 5.34	
		Both-edge setting		2.5	—			
		Phase counting mode		2.5	—			
SCI	Input clock cycle	Asynchronous	t _{Scyc}	4	—	t _{Pcyc}	Figure 5.35	
		Clock synchronous		6	—			
	Input clock pulse width		t _{SCKW}	0.4	0.6	t _{Scyc}	Figure 5.36 C = 30 pF	
	Input clock rise time		t _{SCKr}	—	20	ns		
	Input clock fall time		t _{SCKf}	—	20	ns		
	Output clock cycle	Asynchronous	t _{Scyc}	16	—	t _{Pcyc}		
		Clock synchronous		4	—			
	Output clock pulse width		t _{SCKW}	0.4	0.6	t _{Scyc}		
	Output clock rise time		t _{SCKr}	—	20	ns		
	Output clock fall time		t _{SCKf}	—	20	ns		
	Transmit data delay time (master)	Clock synchronous		t _{TXD}	—	40		ns
	Transmit data delay time (slave)	Clock synchronous	2.7 V or above		—	65		ns
			1.8 V or above		—	100		ns
	Receive data setup time (master)	Clock synchronous	2.7 V or above	t _{RXS}	65	—		ns
			1.8 V or above		90	—		ns
	Receive data setup time (slave)	Clock synchronous			40	—		ns
	Receive data hold time	Clock synchronous		t _{RXH}	40	—		ns
A/D converter	Trigger input pulse width		t _{TRGW}	1.5	—	t _{Pcyc}	Figure 5.37	
CAC	CACREF input pulse width	t _{Pcyc} ≤ t _{cac} *2	t _{CACREF}	4.5 t _{cac} + 3 t _{Pcyc}	—	ns		
		t _{Pcyc} > t _{cac} *2		5 t _{cac} + 6.5 t _{Pcyc}				
CLKOUT	CLKOUT pin output cycle*4	VCC = 2.7 V or above	t _{Ccyc}	125	—	ns		
		VCC = 1.8 V or above		250				
	CLKOUT pin high pulse width*3	VCC = 2.7 V or above	t _{CH}	35	—	ns		
		VCC = 1.8 V or above		70				
	CLKOUT pin low pulse width*3	VCC = 2.7 V or above	t _{CL}	35	—	ns		
		VCC = 1.8 V or above		70				
	CLKOUT pin output rise time	VCC = 2.7 V or above	t _{Cr}	—	15	ns		
		VCC = 1.8 V or above		30				
	CLKOUT pin output fall time	VCC = 2.7 V or above	t _{Cf}	—	15	ns		
		VCC = 1.8 V or above		30				

Note 1. t_{Pcyc} : PCLK cycleNote 2. t_{cac} : CAC count clock source cycle

Note 3. When the LOCO is selected as the clock output source (CKOCR.CKOSSEL[2:0] bits = 000b), set the clock output division ratio selection to divided by 2 (CKOCR.CKODIV[2:0] bits = 001b).

Note 4. When the XTAL external clock input or an oscillator is used with divided by 1 (CKOCR.CKOSSEL[2:0] bits = 010b and CKOCR.CKODIV[2:0] bits = 000b) to output from CLKOUT, the above should be satisfied with an input duty cycle of 45 to 55%.

Table 5.33 Timing of On-Chip Peripheral Modules (4)Conditions: $2.7\text{ V} \leq \text{VCC} \leq 3.6\text{ V}$, $2.7\text{ V} \leq \text{AVCC0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = 0\text{ V}$, $f_{\text{PCLKB}} \leq 32\text{ MHz}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.*1	Max.	Unit	Test Conditions
RIIC (Standard mode, SMBus)	SCL0 input cycle time	t_{SCL}	$6(12) \times t_{\text{IICcyc}} + 1300$	—	ns	Figure 5.46
	SCL0 input high pulse width	t_{SCLH}	$3(6) \times t_{\text{IICcyc}} + 300$	—	ns	
	SCL0 input low pulse width	t_{SCLL}	$3(6) \times t_{\text{IICcyc}} + 300$	—	ns	
	SCL0, SDA0 input rise time	t_{Sr}	—	1000	ns	
	SCL0, SDA0 input fall time	t_{Sf}	—	300	ns	
	SCL0, SDA0 input spike pulse removal time	t_{SP}	0	$1(4) \times t_{\text{IICcyc}}$	ns	
	SDA0 input bus free time	t_{BUF}	$3(6) \times t_{\text{IICcyc}} + 300$	—	ns	
	START condition input hold time	t_{STAH}	$t_{\text{IICcyc}} + 300$	—	ns	
	Repeated START condition input setup time	t_{STAS}	1000	—	ns	
	STOP condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	$t_{\text{IICcyc}} + 50$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL0, SDA0 capacitive load	C_b	—	400	pF	
RIIC (Fast mode)	SCL0 input cycle time	t_{SCL}	$6(12) \times t_{\text{IICcyc}} + 600$	—	ns	Figure 5.46
	SCL0 input high pulse width	t_{SCLH}	$3(6) \times t_{\text{IICcyc}} + 300$	—	ns	
	SCL0 input low pulse width	t_{SCLL}	$3(6) \times t_{\text{IICcyc}} + 300$	—	ns	
	SCL0, SDA0 input rise time	t_{Sr}	—*2	300	ns	
	SCL0, SDA0 input fall time	t_{Sf}	—*2	300	ns	
	SCL0, SDA0 input spike pulse removal time	t_{SP}	0	$1(4) \times t_{\text{IICcyc}}$	ns	
	SDA0 input bus free time	t_{BUF}	$3(6) \times t_{\text{IICcyc}} + 300$	—	ns	
	START condition input hold time	t_{STAH}	$t_{\text{IICcyc}} + 300$	—	ns	
	Repeated START condition input setup time	t_{STAS}	300	—	ns	
	STOP condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	$t_{\text{IICcyc}} + 50$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL0, SDA0 capacitive load	C_b	—	400	pF	

Note: t_{IICcyc} : RIIC internal reference count clock (IIC ϕ) cycle

Note 1. The value in parentheses is used when the ICMR3.NF[1:0] bits are set to 11b while a digital filter is enabled with the ICFER.NFE bit = 1.

Note 2. The minimum t_{sr} and t_{sf} specifications for fast mode are not set.

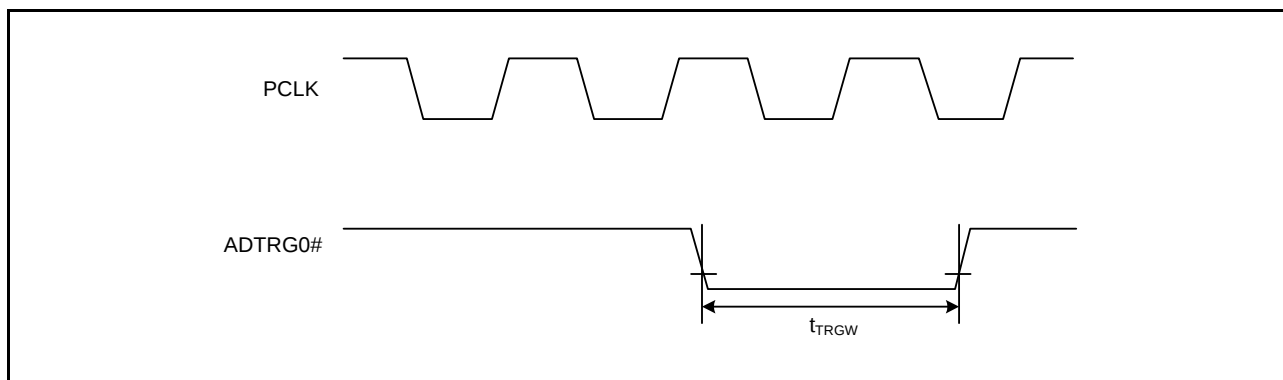


Figure 5.37 A/D Converter External Trigger Input Timing

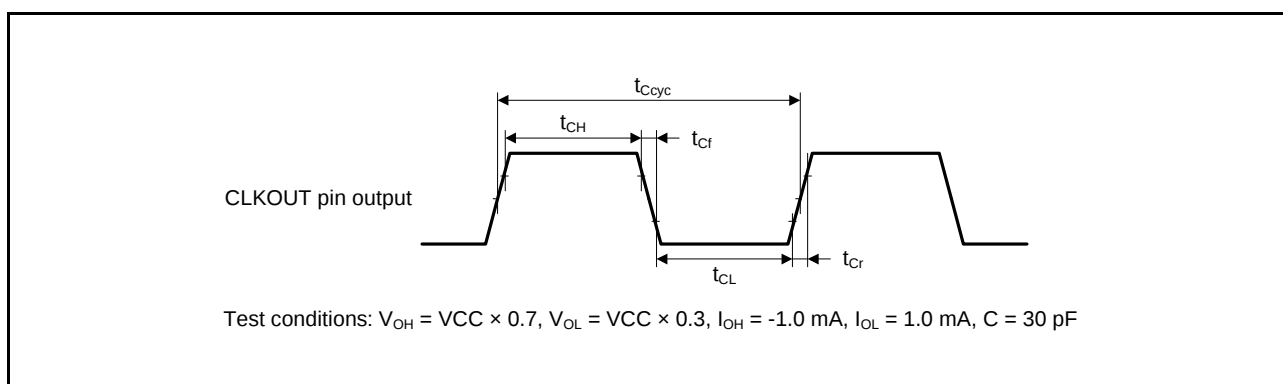


Figure 5.38 CLKOUT Output Timing

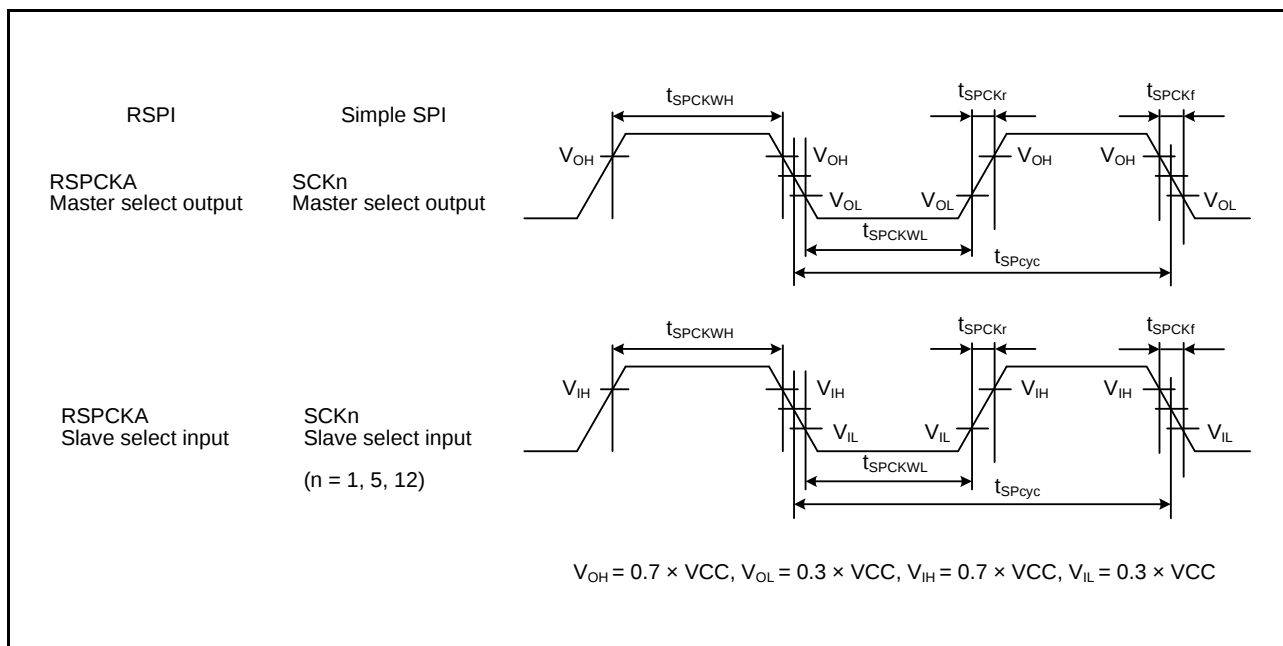


Figure 5.39 RSPI Clock Timing and Simple SPI Clock Timing

Table 5.38 A/D Converter Channel Classification

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN004, AN006	AVCC0 = 1.8 to 3.6 V	Pins AN000 to AN004 and AN006 cannot be used as digital outputs when the A/D converter is in use.
Normal-precision channel	AN008 to AN015		
Internal reference voltage input channel	Internal reference voltage	AVCC0 = 2.0 to 3.6 V	
Temperature sensor input channel	Temperature sensor output	AVCC0 = 2.0 to 3.6 V	

Table 5.39 A/D Internal Reference Voltage Characteristics

Conditions: $2.0\text{ V} \leq V_{CC} \leq 3.6\text{ V}$, $2.0\text{ V} \leq AV_{CC0} \leq 3.6\text{ V}^{*1}$, $V_{SS} = AV_{SS0} = V_{REFL0} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
Internal reference voltage input channel*2	1.36	1.43	1.50	V	

Note 1. The internal reference voltage cannot be selected for input channels when $AV_{CC0} < 2.0\text{ V}$.

Note 2. The A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the A/D converter.

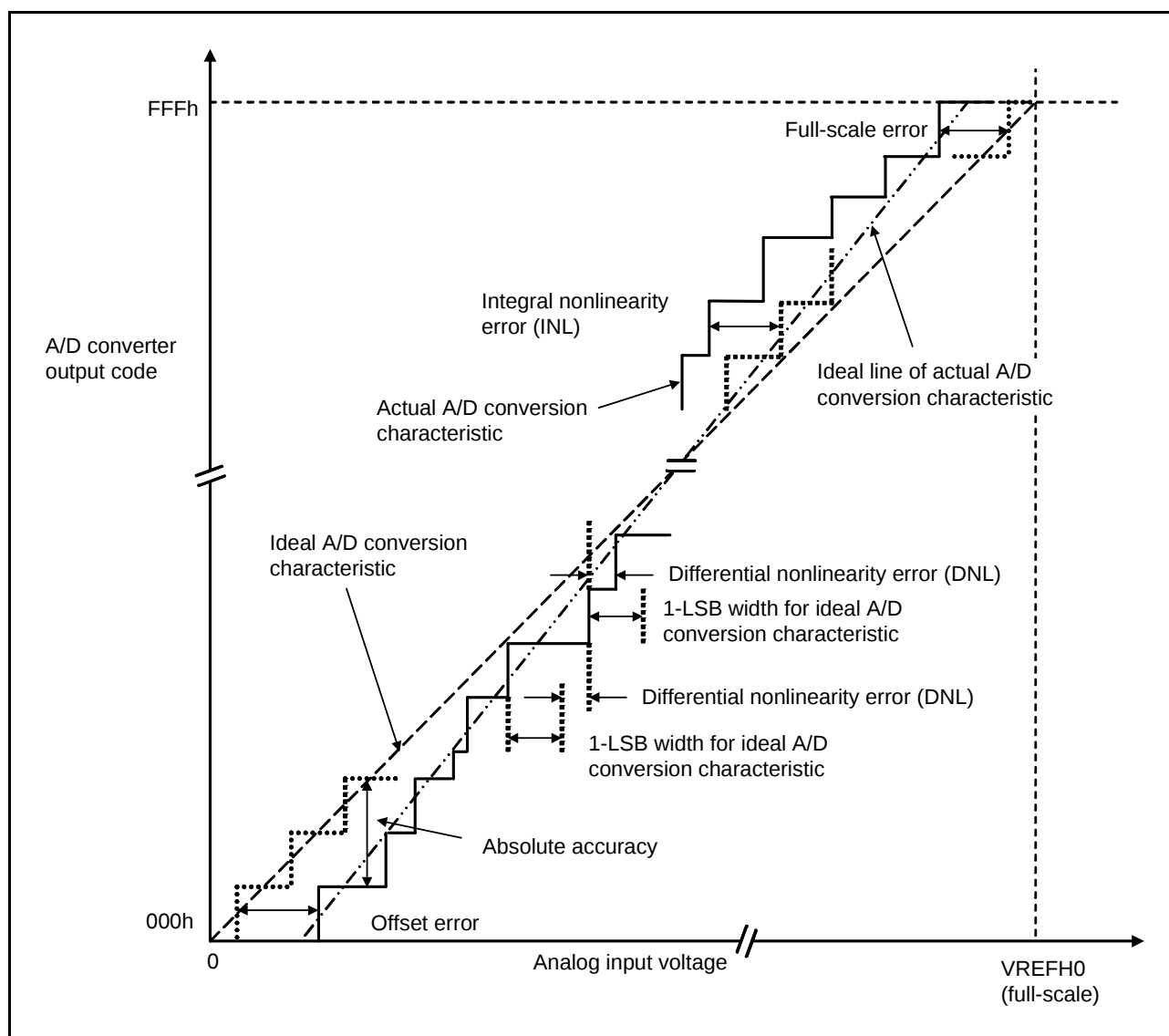


Figure 5.48 Illustration of A/D Converter Characteristic Terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage ($V_{REFH0} = 3.072\text{ V}$), then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, 1.5 mV, ... are used as analog input voltages.

If analog input voltage is 6 mV, absolute accuracy = $\pm 5\text{ LSB}$ means that the actual A/D conversion result is in the range of 003h to 00Dh though an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

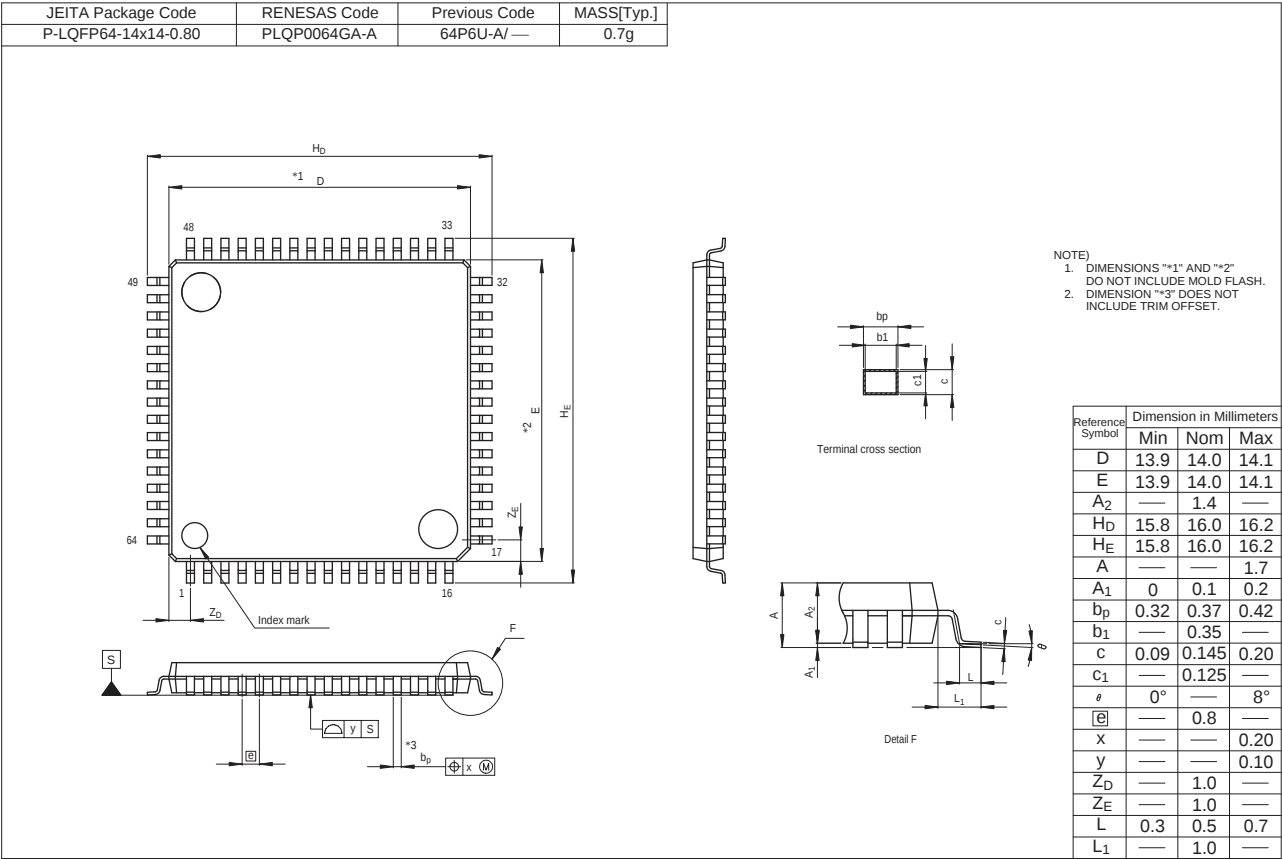


Figure B 64-Pin LQFP (PLQP0064GA-A)