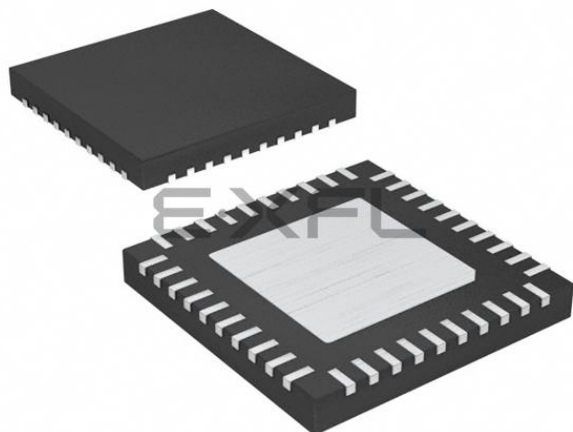




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	28
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-WFQFN Exposed Pad
Supplier Device Package	40-HWQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5110jadnf-u0

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications, and Table 1.2 gives a comparison of the functions of the products in different packages.

Table 1.1 is for products with the greatest number of functions, so the number of peripheral modules and channels will differ in accordance with the package type. For details, see Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/3)

Classification	Module/Function	Description
CPU	CPU	- Maximum operating frequency: 32 MHz 32-bit RX CPU - Minimum instruction execution time: One instruction per one clock cycle - Address space: 4-Gbyte linear - Register set - General purpose: Sixteen 32-bit registers - Control: Eight 32-bit registers - Accumulator: One 64-bit register - Basic instructions: 73 - DSP instructions: 9 - Addressing modes: 10 - Data arrangement - Instructions: Little endian - Data: Selectable as little endian or big endian - On-chip 32-bit multiplier: 32-bit × 32-bit → 64-bit - On-chip divider: 32-bit ÷ 32-bit → 32 bits - Barrel shifter: 32 bits
Memory	ROM	- Capacity: 8 K /16 K /32 K /64 K /96 K /128 Kbytes 32 MHz, no-wait memory access - Programming/erasing method: - Serial programming (asynchronous serial communication), self-programming
	RAM	- Capacity: 8 K /10 K /16 Kbytes 32 MHz, no-wait memory access
MCU operating mode		Single-chip mode
Clock	Clock generation circuit	- Main clock oscillator, sub-clock oscillator, low-speed on-chip oscillator, high-speed on-chip oscillator, and IWDG-dedicated on-chip oscillator - Oscillation stop detection: Available - Clock frequency accuracy measurement circuit (CAC) - Independent settings for the system clock (ICK), peripheral module clock (PCLK), and FlashIF clock (FCLK) - The CPU and system sections such as other bus masters run in synchronization with the system clock (ICK): 32 MHz (at max.) - Peripheral modules run in synchronization with the PCLK: 32 MHz (at max.) - The flash peripheral circuit runs in synchronization with the FCLK: 32 MHz (at max.) - The ICK frequency can only be set to FCLK, PCLKB, or PCLKD multiplied by n (n: 1, 2, 4, 8, 16, 32, 64).
Resets		RES# pin reset, power-on reset, voltage monitoring reset, independent watchdog timer reset, and software reset
Voltage detection	Voltage detection circuit (LVDAa)	- When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. - Voltage detection circuit 1 is capable of selecting the detection voltage from 10 levels - Voltage detection circuit 2 is capable of selecting the detection voltage from 4 levels
Low power consumption	Low power consumption functions	- Module stop function - Three low power consumption modes - Sleep mode, deep sleep mode, and software standby mode
	Function for lower operating power consumption	- Operating power control modes - High-speed operating mode, middle-speed operating mode, and low-speed operating mode
Interrupt	Interrupt controller (ICUb)	- Interrupt vectors: 65 - External interrupts: 9 (NMI, IRQ0 to IRQ7 pins) - Non-maskable interrupts: 4 (NMI pin, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, and IWDG interrupt) 16 levels specifiable for the order of priority
DMA	Data transfer controller (DTCa)	- Transfer modes: Normal transfer, repeat transfer, and block transfer - Activation sources: Interrupts - Chain transfer function

Table 1.3 List of Products (2/2)

Group	Part No.	Orderable Part No.	Package	ROM Capacity	RAM Capacity	Maximum Operating Frequency	Operating Temperature
RX110	R5F51105ADFM	R5F51105ADFM#30	PLQP0064KB-A				
	R5F51105ADFK	R5F51105ADFK#30	PLQP0064GA-A				
	R5F51105ADLF	R5F51105ADLF#U0	PWLG0064KA-A	128 Kbytes			
	R5F51105ADFL	R5F51105ADFL#30	PLQP0048KB-A				
	R5F51105ADNE	R5F51105ADNE#U0	PWQN0048KB-A				
	R5F51104ADFM	R5F51104ADFM#30	PLQP0064KB-A		16 Kbytes		
	R5F51104ADFK	R5F51104ADFK#30	PLQP0064GA-A				
	R5F51104ADLF	R5F51104ADLF#U0	PWLG0064KA-A	96 Kbytes			
	R5F51104ADFL	R5F51104ADFL#30	PLQP0048KB-A				
	R5F51104ADNE	R5F51104ADNE#U0	PWQN0048KB-A				
	R5F51103ADFM	R5F51103ADFM#30	PLQP0064KB-A				
	R5F51103ADFK	R5F51103ADFK#30	PLQP0064GA-A				
	R5F51103ADLF	R5F51103ADLF#U0	PWLG0064KA-A				
	R5F51103ADFL	R5F51103ADFL#30	PLQP0048KB-A	64 Kbytes			
	R5F51103ADNE	R5F51103ADNE#U0	PWQN0048KB-A				
	R5F51103ADLM	R5F51103ADLM#U0	PWLG0036KA-A				
	R5F51103ADNF	R5F51103ADNF#U0	PWQN0040KC-A				
	R5F51101ADFM	R5F51101ADFM#30	PLQP0064KB-A		10 Kbytes	32MHz	–40 to +85°C
	R5F51101ADFK	R5F51101ADFK#30	PLQP0064GA-A				
	R5F51101ADLF	R5F51101ADLF#U0	PWLG0064KA-A				
	R5F51101ADFL	R5F51101ADFL#30	PLQP0048KB-A	32 Kbytes			
	R5F51101ADNE	R5F51101ADNE#U0	PWQN0048KB-A				
	R5F51101ADLM	R5F51101ADLM#U0	PWLG0036KA-A				
	R5F51101ADNF	R5F51101ADNF#U0	PWQN0040KC-A				
	R5F5110JADFM	R5F5110JADFM#30	PLQP0064KB-A				
	R5F5110JADFK	R5F5110JADFK#30	PLQP0064GA-A				
	R5F5110JADLF	R5F5110JADLF#U0	PWLG0064KA-A				
	R5F5110JADFL	R5F5110JADFL#30	PLQP0048KB-A	16 Kbytes			
	R5F5110JADNE	R5F5110JADNE#U0	PWQN0048KB-A		8 Kbytes		
	R5F5110JADLM	R5F5110JADLM#U0	PWLG0036KA-A				
	R5F5110JADNF	R5F5110JADNF#U0	PWQN0040KC-A				
	R5F5110HADLM	R5F5110HADLM#U0	PWLG0036KA-A	8 Kbytes			
	R5F5110HADNF	R5F5110HADNF#U0	PWQN0040KC-A				

Note: Orderable part numbers are current as of when this manual was published. Please make sure to refer to the relevant product page on the Renesas website for the latest part numbers.

Table 1.4 Pin Functions (2/3)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIe)	• Simple I ² C mode		
	SSCL1, SSCL5	I/O	Input/output pins for the I ² C clock.
	SSDA1, SSDA5	I/O	Input/output pins for the I ² C data.
	• Simple SPI mode		
	SCK1, SCK5	I/O	Input/output pins for the clock.
	SMISO1, SMISO5	I/O	Input/output pins for slave transmit data.
	SMOSI1, SMOSI5	I/O	Input/output pins for master transmit data.
	SS1#, SS5#	Input	Chip-select input pins.
Serial communications interface (SCI _f)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock.
	RXD12	Input	Input pin for receiving data.
	TXD12	Output	Output pin for transmitting data.
	CTS12#	Input	Input pin for controlling the start of transmission and reception.
	RTS12#	Output	Output pin for controlling the start of transmission and reception.
	• Simple I ² C mode		
	SSCL12	I/O	Input/output pin for the I ² C clock.
	SSDA12	I/O	Input/output pin for the I ² C data.
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock.
	SMISO12	I/O	Input/output pin for slave transmit data.
	SMOSI12	I/O	Input/output pin for master transmit data.
	SS12#	Input	Chip-select input pin.
	• Extended serial mode		
	RXDX12	Input	Input pin for data reception by SCI _f .
	TXDX12	Output	Output pin for data transmission by SCI _f .
	SIOX12	I/O	Input/output pin for data reception or transmission by SCI _f .
I ² C bus interface	SCL0	I/O	Input/output pin for I ² C bus interface clocks. Bus can be directly driven by the N-channel open drain output.
	SDA0	I/O	Input/output pin for I ² C bus interface data. Bus can be directly driven by the N-channel open drain output.
Serial peripheral interface	RSPCKA	I/O	Input/output pin for the RSPI clock.
	MOSIA	I/O	Input/output pin for transmitting data from the RSPI master.
	MISOA	I/O	Input/output pin for transmitting data from the RSPI slave.
	SSLA0	I/O	Input/output pin to select the slave for the RSPI.
	SSLA1 to SSLA3	Output	Output pins to select the slave for the RSPI.
12-bit A/D converter	AN000 to AN004, AN006, AN008 to AN015	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0#	Input	Input pin for the external trigger signals that start the A/D conversion.
I/O ports	P03, P05	I/O	2-bit input/output pins.
	P14 to P17	I/O	4-bit input/output pins.
	P26, P27	I/O	2-bit input/output pins.
	P30 to P32, P35	I/O	4-bit input/output pins (P35 input pin).
	P40 to P44, P46	I/O	6-bit input/output pins.
	P54, P55	I/O	2-bit input/output pins.
	PA0, PA1, PA3, PA4, PA6	I/O	5-bit input/output pins.
	PB0, PB1, PB3, PB5 to PB7	I/O	6-bit input/output pins.

Table 1.5 List of Pins and Pin Functions (64-Pin LFQFP/LQFP) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, RTC)	Communication (SCle, SCIf, RSPI, RIIC)	Others
1		P03			
2		P27	MTIOC2B	SCK1/SCK12	IRQ3/CMPA2/ CACREF/ADTRG0#
3		P26	MTIOC2A	TXD1/SMOSI1/SSDA1	
4		P30		RXD1/SMISO1/SSCL1	IRQ0
5		P31		CTS1#/RTS1#/SS1#	IRQ1
6	MD				FINED
7	RES#				
8	XCOUT				
9	XCIN	PH7			
10		P35			NMI
11	XTAL				
12	EXTAL				
13	VCL				
14	VSS				
15	VCC				
16		P32	MTIOC0C/RTCOUT		IRQ2
17		P17	MTIOC0C	SCK1/MISOA/SDA0/RXD12/RXD12/ SMISO12/SSCL12	IRQ7
18		P16	RTCOUT	TXD1/SMOSI1/SSDA1/MOSIA/SCL0	IRQ6/ADTRG0#
19		P15	MTIOC0B/MTCLKB	RXD1/SMISO1/SSCL1/RSPCKA	IRQ5/CLKOUT
20		P14	MTIOC0A/MTCLKA	CTS1#/RTS1#/SS1#/SSLA0/TXD12/ TXDX12/SIOX12/SMOSI12/SSDA12	IRQ4
21		PH3	MTIOC1A		
22		PH2			IRQ1
23		PH1			IRQ0
24		PH0	MTIOC1B		CACREF
25		P55			
26		P54			
27		PC7	MTCLKB	TXD1/SMOSI1/SSDA1/MISOA	CACREF
28		PC6	MTCLKA	RXD1/SMISO1/SSCL1/MOSIA	
29		PC5	MTCLKD	SCK1/RSPCKA	
30		PC4	MTCLKC	SCK5/SSLA0	IRQ2/CLKOUT
31		PC3		TXD5/SMOSI5/SSDA5	
32		PC2		RXD5/SMISO5/SSCL5/SSLA3	
33		PB7/PC1			
34		PB6/PC0			
35		PB5	MTIOC2A/MTIOC1B		
36		PB3	MTIOC0A		
37		PB1	MTIOC0C		IRQ4
38	VCC				
39		PB0	MTIC5W/MTIOC0C/ RTCOUT	SCL0/RSPCKA	IRQ2/ADTRG0#
40	VSS				
41		PA6	MTIC5V/MTCLKB/MTIOC2A	CTS5#/RTS5#/SS5#/SDA0/MOSIA	IRQ3
42		PA4	MTIC5U/MTCLKA/MTIOC2B	TXD5/SMOSI5/SSDA5/SSLA0	IRQ5
43		PA3	MTIOC0D/MTCLKD/ MTIOC1B	RXD5/SMISO5/SSCL5/MISOA	IRQ6
44		PA1	MTIOC0B/MTCLKC/ RTCOUT	SCK5/SSLA2	

Table 1.5 List of Pins and Pin Functions (64-Pin LFQFP/LQFP) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, RTC)	Communication (SCle, SCIf, RSPI, RIIC)	Others
45		PA0		SSLA1	CACREF
46		PE5	MTIOC2B		IRQ5/AN013
47		PE4	MTIOC1A	MOSIA	IRQ4/AN012
48		PE3	MTIOC0A/MTIOC1B	CTS12#/RTS12#/SS12#/RSPCKA	IRQ3/AN011
49		PE2		RXD12/RXDX12/SMISO12/SSCL12	IRQ7/AN010
50		PE1		TXD12/TXDX12/SIOX12/SMOSI12/SSDA12	IRQ1/AN009
51		PE0	MTIOC2A	SCK12	IRQ0/AN008
52		PE7			IRQ7/AN015
53		PE6			IRQ6/AN014
54		P46*1			AN006
55		P44*1			AN004
56		P43*1			AN003
57		P42*1			AN002
58		P41*1			AN001
59	VREFL0	PJ7*1			
60		P40*1			AN000
61	VREFH0	PJ6*1			
62	AVSS0				
63	AVCC0				
64		P05			

Note 1. The power source of the I/O buffer for these pins is AVCC0.

Table 1.7 List of Pins and Pin Functions (48-Pin LFQFP/HWQFN) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, RTC)	Communication (SCIE, SCIF, RSPI, RIIC)	Others
1		P27	MTIOC2B	SCK1/SCK12	IRQ3/CMPA2/CACREF/ADTRG0#
2		P26	MTIOC2A	TXD1/SMOSI1/SSDA1	
3	MD				FINED
4	RES#				
5	XCOUT				
6	XCIN	PH7			
7		P35			NMI
8	XTAL				
9	EXTAL				
10	VCL				
11	VSS				
12	VCC				
13		P17	MTIOC0C	SCK1/MISOA/SDA0/RXD12/RXD12/SMISO12/SSCL12	IRQ7
14		P16	RTCOUT	TXD1/SMOSI1/SSDA1/MOSIA/SCL0	IRQ6/ADTRG0#
15		P15	MTIOC0B/MTCLKB	RXD1/SMISO1/SSCL1/RSPCKA	IRQ5/CLKOUT
16		P14	MTIOC0A/MTCLKA	CTS1#/RTS1#/SS1#/SSLA0/TXD12/TXD12/SIOX12/SMOSI12/SSDA12	IRQ4
17		PH3	MTIOC1A		
18		PH2			IRQ1
19		PH1			IRQ0
20		PH0	MTIOC1B		CACREF
21		PC7	MTCLKB	TXD1/SMOSI1/SSDA1/MISOA	CACREF
22		PC6	MTCLKA	RXD1/SMISO1/SSCL1/MOSIA	
23		PC5	MTCLKD	SCK1/RSPCKA	
24		PC4	MTCLKC	SCK5/SSLA0	IRQ2/CLKOUT
25		PB5/PC3	MTIOC2A/MTIOC1B		
26		PB3/PC2	MTIOC0A		
27		PB1/PC1	MTIOC0C		IRQ4
28	VCC				
29		PB0/PC0	MTIC5W/MTIOC0C/RTCOUT	SCL0/RSPCKA	IRQ2/ADTRG0#
30	VSS				
31		PA6	MTIC5V/MTCLKB/MTIOC2A	CTS5#/RTS5#/SS5#/SDA0/MOSIA	IRQ3
32		PA4	MTIC5U/MTCLKA/MTIOC2B	TXD5/SMOSI5/SSDA5/SSLA0	IRQ5
33		PA3	MTIOC0D/MTCLKD/MTIOC1B	RXD5/SMISO5/SSCL5/MISOA	IRQ6
34		PA1	MTIOC0B/MTCLKC/RTCOUT	SCK5/SSLA2	
35		PE4	MTIOC1A	MOSIA	IRQ4/AN012
36		PE3	MTIOC0A/MTIOC1B	CTS12#/RTS12#/SS12#/RSPCKA	IRQ3/AN011
37		PE2		RXD12/RXD12/SMISO12/SSCL12	IRQ7/AN010
38		PE1		TXD12/TXD12/SIOX12/SMOSI12/SSDA12	IRQ1/AN009
39		PE0	MTIOC2A	SCK12	IRQ0/AN008
40		PE7			IRQ7/AN015
41		P46*1			AN006
42		P42*1			AN002
43		P41*1			AN001
44	VREFL0	PJ7*1			

Table 1.7 List of Pins and Pin Functions (48-Pin LFQFP/HWQFN) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, RTC)	Communication (SCle, SCIf, RSPI, RIIC)	Others
45		P40*1			AN000
46	VREFH0	PJ6*1			
47	AVSS0				
48	AVCC0				

Note 1. The power source of the I/O buffer for these pins is AVCC0.

Table 1.9 List of Pins and Pin Functions (36-Pin WFLGA)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, RTC)	Communication (SCle, SCIf, RSPI, RIIC)	Others
A1	AVSS0				
A2	AVCC0				
A3	VREFH0	PJ6*1			
A4		P42*1			AN002
A5		P41*1			AN001
A6		PE2		RXD12/RXDX12/SMISO12/SSCL12	IRQ7/AN010
B1	RES#				
B2		P27	MTIOC2B	SCK1/SCK12	IRQ3/CMPA2/CACREF/ADTRG0#
B3	VREFL0	PJ7*1			
B4		PE0	MTIOC2A	SCK12	IRQ0/AN008
B5		PE1		TXD12/TXDX12/SIOX12/SMOSI12/SSDA12	IRQ1/AN009
B6		PA3	MTIOC0D/MTCLKD/MTIOC1B	RXD5/SMISO5/SSCL5/MISOA	IRQ6
C1	XTAL				
C2	MD				FINED
C3		PE3	MTIOC0A/MTIOC1B	CTS12#/RTS12#/SS12#/RSPCKA	IRQ3/AN011
C4		PE4	MTIOC1A	MOSIA	IRQ4/AN012
C5		PA4	MTIOC2B/MTIC5U/MTCLKA	TXD5/SMOSI5/SSDA5/SSLA0	IRQ5
C6	VSS				
D1	EXTAL				
D2		P35			NMI
D3		P14	MTIOC0A/MTCLKA	CTS1#/RTS1#/SS1#/SSLA0/TXD12/TXDX12/SIOX12/SMOSI12/SSDA12	IRQ4
D4		PA6	MTIC5V/MTCLKB/MTIOC2A	CTS5#/RTS5#/SS5#/SDA0/MOSIA	IRQ3
D5		PB3	MTIOC0A		
D6		PB0	MTIOC0C/MTIC5W	SCL0/RSPCKA	IRQ2/ADTRG0#
E1	VCL				
E2		P17	MTIOC0C	SCK1/MISOA/SDA0/RXD12/RXDX12/SMISO12/SSCL12	IRQ7
E3		P16		TXD1/SMOSI1/SSDA1/SCL0/MOSIA	IRQ6/ADTRG0#
E4		P15	MTIOC0B/MTCLKB	RXD1/SMISO1/SSCL1/RSPCKA	IRQ5/CLKOUT
E5		PC4	MTCLKC	SCK5/SSLA0	IRQ2/CLKOUT
E6	VCC				
F1	VSS				
F2	VCC				
F3		PH3	MTIOC1A		
F4		PH2			IRQ1
F5		PH1			IRQ0
F6		PH0	MTIOC1B		CACREF

Note 1. The power source of the I/O buffer for these pins is AVCC0.

Table 4.1 List of I/O Registers (Address Order) (2/13)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 702Dh	ICU	Interrupt Request Register 045	IR045	8	8	2 ICLK
0008 702Eh	ICU	Interrupt Request Register 046	IR046	8	8	2 ICLK
0008 702Fh	ICU	Interrupt Request Register 047	IR047	8	8	2 ICLK
0008 7039h	ICU	Interrupt Request Register 057	IR057	8	8	2 ICLK
0008 703Fh	ICU	Interrupt Request Register 063	IR063	8	8	2 ICLK
0008 7040h	ICU	Interrupt Request Register 064	IR064	8	8	2 ICLK
0008 7041h	ICU	Interrupt Request Register 065	IR065	8	8	2 ICLK
0008 7042h	ICU	Interrupt Request Register 066	IR066	8	8	2 ICLK
0008 7043h	ICU	Interrupt Request Register 067	IR067	8	8	2 ICLK
0008 7044h	ICU	Interrupt Request Register 068	IR068	8	8	2 ICLK
0008 7045h	ICU	Interrupt Request Register 069	IR069	8	8	2 ICLK
0008 7046h	ICU	Interrupt Request Register 070	IR070	8	8	2 ICLK
0008 7047h	ICU	Interrupt Request Register 071	IR071	8	8	2 ICLK
0008 7058h	ICU	Interrupt Request Register 088	IR088	8	8	2 ICLK
0008 7059h	ICU	Interrupt Request Register 089	IR089	8	8	2 ICLK
0008 705Ah	ICU	Interrupt Request Register 090	IR090	8	8	2 ICLK
0008 705Ch	ICU	Interrupt Request Register 092	IR092	8	8	2 ICLK
0008 705Dh	ICU	Interrupt Request Register 093	IR093	8	8	2 ICLK
0008 7066h	ICU	Interrupt Request Register 102	IR102	8	8	2 ICLK
0008 7067h	ICU	Interrupt Request Register 103	IR103	8	8	2 ICLK
0008 706Ah	ICU	Interrupt Request Register 106	IR106	8	8	2 ICLK
0008 7072h	ICU	Interrupt Request Register 114	IR114	8	8	2 ICLK
0008 7073h	ICU	Interrupt Request Register 115	IR115	8	8	2 ICLK
0008 7074h	ICU	Interrupt Request Register 116	IR116	8	8	2 ICLK
0008 7075h	ICU	Interrupt Request Register 117	IR117	8	8	2 ICLK
0008 7076h	ICU	Interrupt Request Register 118	IR118	8	8	2 ICLK
0008 7077h	ICU	Interrupt Request Register 119	IR119	8	8	2 ICLK
0008 7078h	ICU	Interrupt Request Register 120	IR120	8	8	2 ICLK
0008 7079h	ICU	Interrupt Request Register 121	IR121	8	8	2 ICLK
0008 707Ah	ICU	Interrupt Request Register 122	IR122	8	8	2 ICLK
0008 707Bh	ICU	Interrupt Request Register 123	IR123	8	8	2 ICLK
0008 707Ch	ICU	Interrupt Request Register 124	IR124	8	8	2 ICLK
0008 707Dh	ICU	Interrupt Request Register 125	IR125	8	8	2 ICLK
0008 707Eh	ICU	Interrupt Request Register 126	IR126	8	8	2 ICLK
0008 707Fh	ICU	Interrupt Request Register 127	IR127	8	8	2 ICLK
0008 7080h	ICU	Interrupt Request Register 128	IR128	8	8	2 ICLK
0008 7081h	ICU	Interrupt Request Register 129	IR129	8	8	2 ICLK
0008 7082h	ICU	Interrupt Request Register 130	IR130	8	8	2 ICLK
0008 7083h	ICU	Interrupt Request Register 131	IR131	8	8	2 ICLK
0008 7084h	ICU	Interrupt Request Register 132	IR132	8	8	2 ICLK
0008 7085h	ICU	Interrupt Request Register 133	IR133	8	8	2 ICLK
0008 7086h	ICU	Interrupt Request Register 134	IR134	8	8	2 ICLK
0008 7087h	ICU	Interrupt Request Register 135	IR135	8	8	2 ICLK
0008 7088h	ICU	Interrupt Request Register 136	IR136	8	8	2 ICLK
0008 7089h	ICU	Interrupt Request Register 137	IR137	8	8	2 ICLK
0008 708Ah	ICU	Interrupt Request Register 138	IR138	8	8	2 ICLK
0008 708Bh	ICU	Interrupt Request Register 139	IR139	8	8	2 ICLK
0008 708Ch	ICU	Interrupt Request Register 140	IR140	8	8	2 ICLK
0008 708Dh	ICU	Interrupt Request Register 141	IR141	8	8	2 ICLK
0008 70AAh	ICU	Interrupt Request Register 170	IR170	8	8	2 ICLK
0008 70ABh	ICU	Interrupt Request Register 171	IR171	8	8	2 ICLK
0008 70DAh	ICU	Interrupt Request Register 218	IR218	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (3/13)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 70DBh	ICU	Interrupt Request Register 219	IR219	8	8	2 ICLK
0008 70DCh	ICU	Interrupt Request Register 220	IR220	8	8	2 ICLK
0008 70DDh	ICU	Interrupt Request Register 221	IR221	8	8	2 ICLK
0008 70DEh	ICU	Interrupt Request Register 222	IR222	8	8	2 ICLK
0008 70DFh	ICU	Interrupt Request Register 223	IR223	8	8	2 ICLK
0008 70E0h	ICU	Interrupt Request Register 224	IR224	8	8	2 ICLK
0008 70E1h	ICU	Interrupt Request Register 225	IR225	8	8	2 ICLK
0008 70EEh	ICU	Interrupt Request Register 238	IR238	8	8	2 ICLK
0008 70EFh	ICU	Interrupt Request Register 239	IR239	8	8	2 ICLK
0008 70F0h	ICU	Interrupt Request Register 240	IR240	8	8	2 ICLK
0008 70F1h	ICU	Interrupt Request Register 241	IR241	8	8	2 ICLK
0008 70F2h	ICU	Interrupt Request Register 242	IR242	8	8	2 ICLK
0008 70F3h	ICU	Interrupt Request Register 243	IR243	8	8	2 ICLK
0008 70F4h	ICU	Interrupt Request Register 244	IR244	8	8	2 ICLK
0008 70F5h	ICU	Interrupt Request Register 245	IR245	8	8	2 ICLK
0008 70F6h	ICU	Interrupt Request Register 246	IR246	8	8	2 ICLK
0008 70F7h	ICU	Interrupt Request Register 247	IR247	8	8	2 ICLK
0008 70F8h	ICU	Interrupt Request Register 248	IR248	8	8	2 ICLK
0008 70F9h	ICU	Interrupt Request Register 249	IR249	8	8	2 ICLK
0008 711Bh	ICU	DTC Activation Enable Register 027	DTCER027	8	8	2 ICLK
0008 711Ch	ICU	DTC Activation Enable Register 028	DTCER028	8	8	2 ICLK
0008 711Dh	ICU	DTC Activation Enable Register 029	DTCER029	8	8	2 ICLK
0008 712Dh	ICU	DTC Activation Enable Register 045	DTCER045	8	8	2 ICLK
0008 712Eh	ICU	DTC Activation Enable Register 046	DTCER046	8	8	2 ICLK
0008 7140h	ICU	DTC Activation Enable Register 064	DTCER064	8	8	2 ICLK
0008 7141h	ICU	DTC Activation Enable Register 065	DTCER065	8	8	2 ICLK
0008 7142h	ICU	DTC Activation Enable Register 066	DTCER066	8	8	2 ICLK
0008 7143h	ICU	DTC Activation Enable Register 067	DTCER067	8	8	2 ICLK
0008 7144h	ICU	DTC Activation Enable Register 068	DTCER068	8	8	2 ICLK
0008 7145h	ICU	DTC Activation Enable Register 069	DTCER069	8	8	2 ICLK
0008 7146h	ICU	DTC Activation Enable Register 070	DTCER070	8	8	2 ICLK
0008 7147h	ICU	DTC Activation Enable Register 071	DTCER071	8	8	2 ICLK
0008 7166h	ICU	DTC Activation Enable Register 102	DTCER102	8	8	2 ICLK
0008 7167h	ICU	DTC Activation Enable Register 103	DTCER103	8	8	2 ICLK
0008 7172h	ICU	DTC Activation Enable Register 114	DTCER114	8	8	2 ICLK
0008 7173h	ICU	DTC Activation Enable Register 115	DTCER115	8	8	2 ICLK
0008 7174h	ICU	DTC Activation Enable Register 116	DTCER116	8	8	2 ICLK
0008 7175h	ICU	DTC Activation Enable Register 117	DTCER117	8	8	2 ICLK
0008 7179h	ICU	DTC Activation Enable Register 121	DTCER121	8	8	2 ICLK
0008 717Ah	ICU	DTC Activation Enable Register 122	DTCER122	8	8	2 ICLK
0008 717Dh	ICU	DTC Activation Enable Register 125	DTCER125	8	8	2 ICLK
0008 717Eh	ICU	DTC Activation Enable Register 126	DTCER126	8	8	2 ICLK
0008 718Bh	ICU	DTC Activation Enable Register 139	DTCER139	8	8	2 ICLK
0008 718Ch	ICU	DTC Activation Enable Register 140	DTCER140	8	8	2 ICLK
0008 718Dh	ICU	DTC Activation Enable Register 141	DTCER141	8	8	2 ICLK
0008 71DBh	ICU	DTC Activation Enable Register 219	DTCER219	8	8	2 ICLK
0008 71DCh	ICU	DTC Activation Enable Register 220	DTCER220	8	8	2 ICLK
0008 71DFh	ICU	DTC Activation Enable Register 223	DTCER223	8	8	2 ICLK
0008 71E0h	ICU	DTC Activation Enable Register 224	DTCER224	8	8	2 ICLK
0008 71EFh	ICU	DTC Activation Enable Register 239	DTCER239	8	8	2 ICLK
0008 71F0h	ICU	DTC Activation Enable Register 240	DTCER240	8	8	2 ICLK
0008 71F7h	ICU	DTC Activation Enable Register 247	DTCER247	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (7/13)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 8726h	MTU0	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	2 or 3 PCLKB
0008 8780h	MTU1	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8781h	MTU1	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB
0008 8782h	MTU1	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKB
0008 8784h	MTU1	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 8785h	MTU1	Timer Status Register	TSR	8	8	2 or 3 PCLKB
0008 8786h	MTU1	Timer Counter	TCNT	16	16	2 or 3 PCLKB
0008 8788h	MTU1	Timer General Register A	TGRA	16	16	2 or 3 PCLKB
0008 878Ah	MTU1	Timer General Register B	TGRB	16	16	2 or 3 PCLKB
0008 8790h	MTU1	Timer Input Capture Control Register	TICCR	8	8	2 or 3 PCLKB
0008 8800h	MTU2	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8801h	MTU2	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB
0008 8802h	MTU2	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKB
0008 8804h	MTU2	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 8805h	MTU2	Timer Status Register	TSR	8	8	2 or 3 PCLKB
0008 8806h	MTU2	Timer Counter	TCNT	16	16	2 or 3 PCLKB
0008 8808h	MTU2	Timer General Register A	TGRA	16	16	2 or 3 PCLKB
0008 880Ah	MTU2	Timer General Register B	TGRB	16	16	2 or 3 PCLKB
0008 8880h	MTU5	Timer Counter U	TCNTU	16	16	2 or 3 PCLKB
0008 8882h	MTU5	Timer General Register U	TGRU	16	16	2 or 3 PCLKB
0008 8884h	MTU5	Timer Control Register U	TCRU	8	8	2 or 3 PCLKB
0008 8886h	MTU5	Timer I/O Control Register U	TIORU	8	8	2 or 3 PCLKB
0008 8890h	MTU5	Timer Counter V	TCNTV	16	16	2 or 3 PCLKB
0008 8892h	MTU5	Timer General Register V	TGRV	16	16	2 or 3 PCLKB
0008 8894h	MTU5	Timer Control Register V	TCRV	8	8	2 or 3 PCLKB
0008 8896h	MTU5	Timer I/O Control Register V	TIORV	8	8	2 or 3 PCLKB
0008 88A0h	MTU5	Timer Counter W	TCNTW	16	16	2 or 3 PCLKB
0008 88A2h	MTU5	Timer General Register W	TGRW	16	16	2 or 3 PCLKB
0008 88A4h	MTU5	Timer Control Register W	TCRW	8	8	2 or 3 PCLKB
0008 88A6h	MTU5	Timer I/O Control Register W	TIORW	8	8	2 or 3 PCLKB
0008 88B2h	MTU5	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 88B4h	MTU5	Timer Start Register	TSTR	8	8	2 or 3 PCLKB
0008 88B6h	MTU5	Timer Compare Match Clear Register	TCNTCMPCLR	8	8	2 or 3 PCLKB
0008 9000h	S12AD	A/D Control Register	ADCSR	16	16	2 or 3 PCLKB
0008 9004h	S12AD	A/D Channel Select Register A	ADANSA	16	16	2 or 3 PCLKB
0008 9008h	S12AD	A/D-Converted Value Addition Mode Select Register	ADADS	16	16	2 or 3 PCLKB
0008 900Ch	S12AD	A/D-Converted Value Addition Count Select Register	ADADC	8	8	2 or 3 PCLKB
0008 900Eh	S12AD	A/D Control Extended Register	ADCER	16	16	2 or 3 PCLKB
0008 9010h	S12AD	A/D Start Trigger Select Register	ADSTRGR	16	16	2 or 3 PCLKB
0008 9012h	S12AD	A/D Converted Extended Input Control Register	ADEXICR	16	16	2 or 3 PCLKB
0008 9014h	S12AD	A/D Channel Select Register B	ADANSB	16	16	2 or 3 PCLKB
0008 9018h	S12AD	A/D Data Duplication Register	ADDBLDR	16	16	2 or 3 PCLKB
0008 901Ah	S12AD	A/D Temperature Sensor Data Register	ADTSDR	16	16	2 or 3 PCLKB
0008 901Ch	S12AD	A/D Internal Reference Voltage Data Register	ADOCDR	16	16	2 or 3 PCLKB
0008 9020h	S12AD	A/D Data Register 0	ADDR0	16	16	2 or 3 PCLKB
0008 9022h	S12AD	A/D Data Register 1	ADDR1	16	16	2 or 3 PCLKB
0008 9024h	S12AD	A/D Data Register 2	ADDR2	16	16	2 or 3 PCLKB
0008 9026h	S12AD	A/D Data Register 3	ADDR3	16	16	2 or 3 PCLKB
0008 9028h	S12AD	A/D Data Register 4	ADDR4	16	16	2 or 3 PCLKB
0008 902Ch	S12AD	A/D Data Register 6	ADDR6	16	16	2 or 3 PCLKB
0008 9030h	S12AD	A/D Data Register 8	ADDR8	16	16	2 or 3 PCLKB
0008 9032h	S12AD	A/D Data Register 9	ADDR9	16	16	2 or 3 PCLKB

Table 5.8 DC Characteristics (6)Conditions: $1.8\text{ V} \leq \text{VCC} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVCC0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item			Symbol	Typ.*3	Max.	Unit	Test Conditions
Supply current*1	Software standby mode*2	T _a = 25°C	I _{CC}	0.35	0.53	μA	
		T _a = 55°C		0.54	1.17		
		T _a = 85°C		1.38	5.2		
		T _a = 105°C		2.8	11.4		
	Increment for RTC operation*4			0.31	—		RCR3.RTCDV[2:0] = 010b
				1.09	—		RCR3.RTCDV[2:0] = 100b
	Increment for IWDWT operation			0.37	—		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. The IWDWT and LVD are stopped.

Note 3. $\text{VCC} = 3.3\text{ V}$.

Note 4. Includes the oscillation circuit.

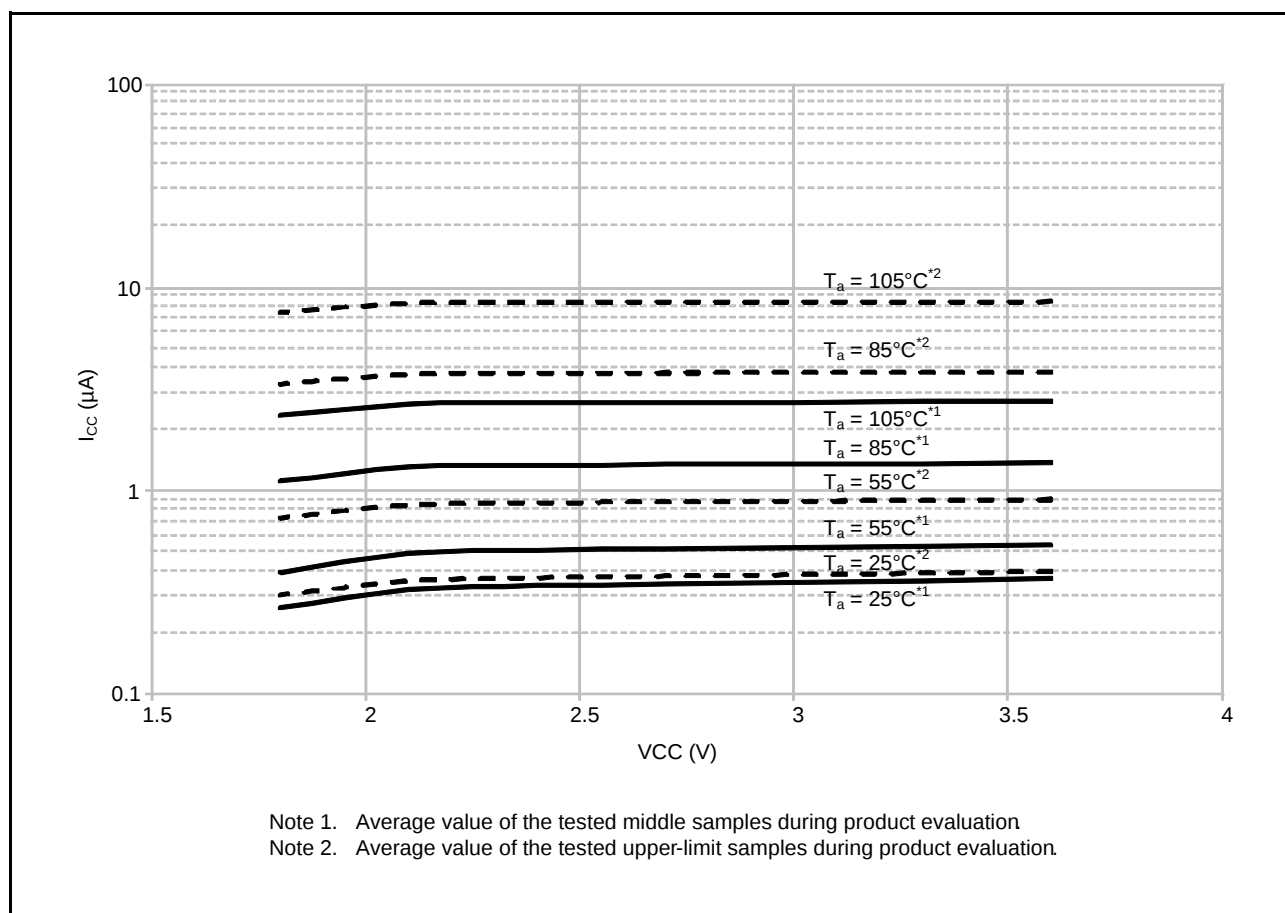
**Figure 5.4 Voltage Dependency in Software Standby Mode (Reference Data)**

Table 5.22 Clock TimingConditions: $1.8\text{ V} \leq \text{VCC} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVCC0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
XTAL external clock input cycle time	t_{Xcyc}	50	—	—	ns	Figure 5.18
XTAL external clock input high pulse width	t_{XH}	20	—	—	ns	
XTAL external clock input low pulse width	t_{XL}	20	—	—	ns	
XTAL external clock rising time	t_{Xr}	—	—	5	ns	
XTAL external clock falling time	t_{Xf}	—	—	5	ns	
XTAL external clock input wait time*1	t_{EXWT}	0.5	—	—	μs	Figure 5.20
Main clock oscillator oscillation frequency	f_{MAIN}	$2.4 \leq \text{VCC} \leq 3.6$	1	—	20	
		$1.8 \leq \text{VCC} < 2.4$	1	—	8	
Main clock oscillation stabilization time (crystal)*2	t_{MAINOSC}	—	3	—	ms	Figure 5.20
Main clock oscillation stabilization time (ceramic resonator)*2	t_{MAINOSC}	—	50	—	μs	
LOCO clock oscillation frequency	f_{LOCO}	3.44	4.0	4.56	MHz	Figure 5.21
LOCO clock oscillation stabilization time	t_{LOCO}	—	—	0.5	μs	
IWDT-dedicated clock oscillation frequency	f_{ILOCO}	12.75	15	17.25	kHz	Figure 5.19
IWDT-dedicated clock oscillation stabilization time	t_{ILOCO}	—	—	50	μs	
HOCO clock oscillation frequency	f_{HOCO}	31.52	32	32.48	MHz	$T_a = -40\text{ to }85^\circ\text{C}$
		31.68	32	32.32		$T_a = -20\text{ to }85^\circ\text{C}$
		31.36	32	32.64		$T_a = -40\text{ to }105^\circ\text{C}$
HOCO clock oscillation stabilization time	t_{HOCO2}	—	—	56	μs	Figure 5.23
Sub-clock oscillator oscillation frequency*4	f_{SUB}	—	32.768	—	kHz	Figure 5.24
Sub-clock oscillation stabilization time*3	t_{SUBOSC}	—	0.5	—	s	

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating) when the external clock is stable.

Note 2. Reference values when an 8-MHz oscillator is used.

When specifying the main clock oscillator stabilization time, set the MOSCWTCR register with a stabilization time value that is equal to or greater than the oscillator-manufacturer-recommended value.
After changing the setting of the MOSCCR.MOSTP bit so that the main clock oscillator operates, read the OSCOVFSR.MOOVF flag to confirm that it has become 1, and then start using the main clock.

Note 3. After changing the setting of the SOSCCR.SOSTP bit or RCR3.RTCEN bit so that the sub-clock oscillator operates, only start using the sub-clock after the sub-clock oscillation stabilization wait time that is equal to or greater than the oscillator-manufacturer-recommended value has elapsed.

Reference value when a 32.768-kHz resonator is used.

Note 4. Only 32.768 kHz can be used.

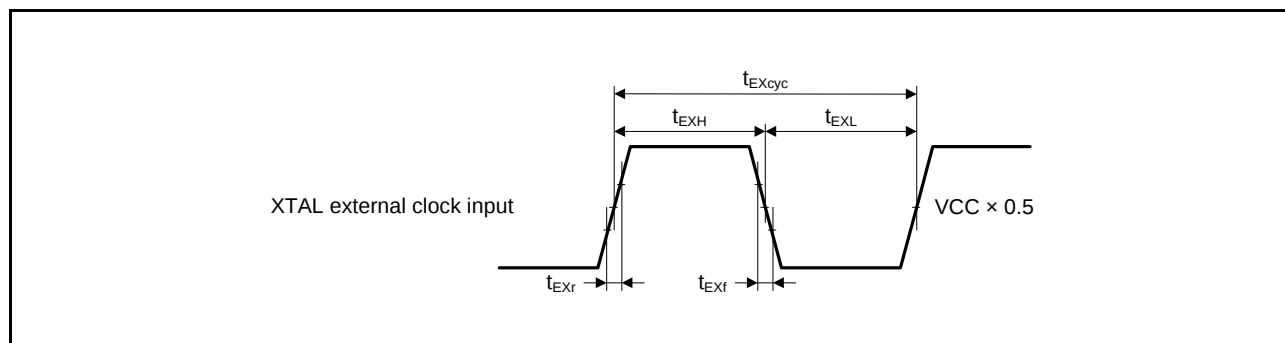
**Figure 5.18 XTAL External Clock Input Timing**

Table 5.27 Timing of Recovery from Low Power Consumption Modes (4)Conditions: $1.8\text{ V} \leq V_{CC} \leq 3.6\text{ V}$, $1.8\text{ V} \leq AV_{CC0} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS0} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from deep sleep mode*1	High-speed mode*2	$t_{DSL P}$	—	2	3.5	μs
	Middle-speed mode*3	$t_{DSL P}$	—	3	4	μs
	Low-speed mode*4	$t_{DSL P}$	—	400	500	μs

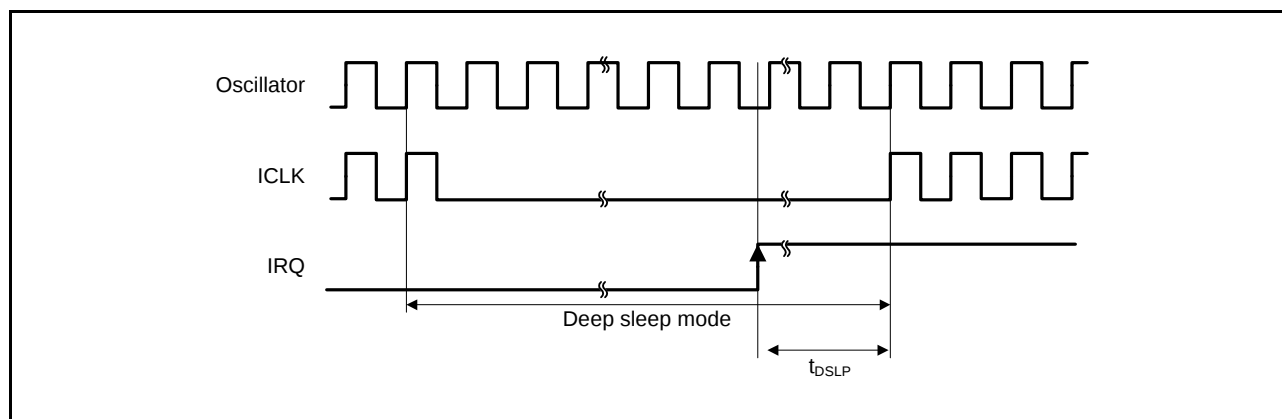
Note: When the division ratios of PCLKB, PCLKD, FCLK, and ICLK are all set to 1.

Note 1. Oscillators continue oscillating in deep sleep mode.

Note 2. When the frequency of the system clock is 32 MHz.

Note 3. When the frequency of the system clock is 12 MHz.

Note 4. When the frequency of the system clock is 32.768 kHz.

**Figure 5.29 Deep Sleep Mode Cancellation Timing****Table 5.28 Timing of Recovery from Low Power Consumption Modes (5) Operating Mode Transition Time**Conditions: $1.8\text{ V} \leq V_{CC} \leq 3.6\text{ V}$, $1.8\text{ V} \leq AV_{CC0} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS0} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Mode before Transition	Mode after Transition	ICLK Frequency	Transition Time			Unit
			Min.	Typ.	Max.	
High-speed operating mode	Middle-speed operating mode	8 MHz	—	10	—	μs
Middle-speed operating mode	High-speed operating mode	8 MHz	—	37.5	—	μs
Low-speed operating mode	Middle-speed operating mode, high-speed operating mode	32.768 kHz	—	213.62	—	μs
Middle-speed operating mode, high-speed operating mode	Low-speed operating mode	32.768 kHz	—	183.11	—	μs

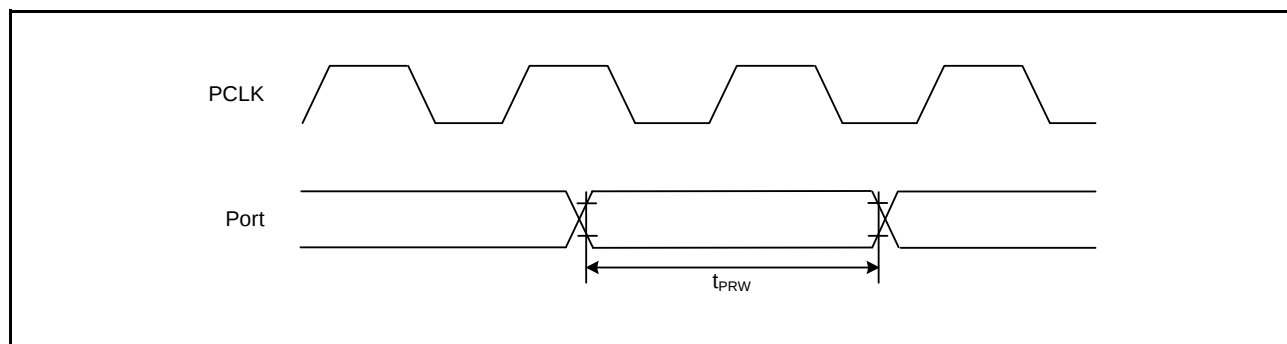
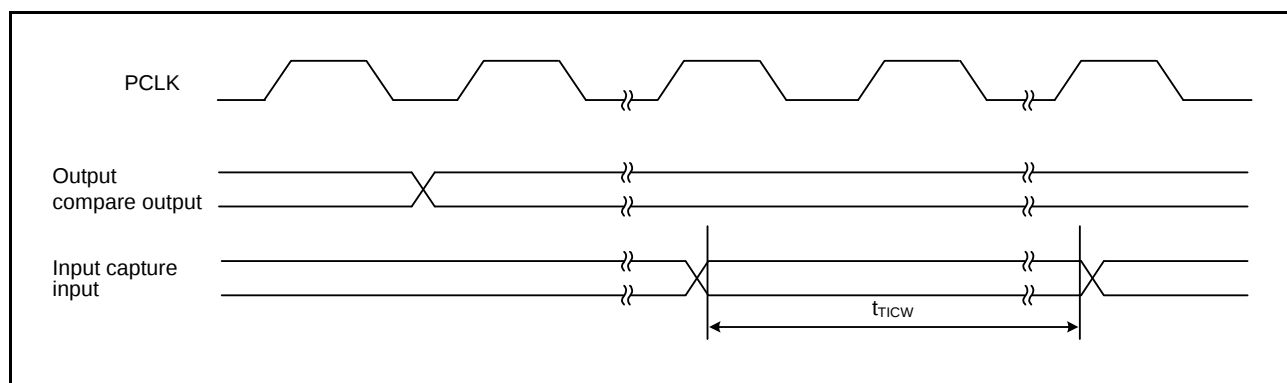
Note: When the division ratios of PCLKB, PCLKD, FCLK, and ICLK are all set to 1.

Table 5.34 Timing of On-Chip Peripheral Modules (5)Conditions: $2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$, $2.7\text{ V} \leq AV_{CC0} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS0} = 0\text{ V}$, $f_{PCLKB} \leq 32\text{ MHz}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.	Max.	Unit	Test Conditions
Simple I ² C (Standard mode)	SDA0 input rise time	t _{Sr}	—	1000	ns	Figure 5.46
	SDA0 input fall time	t _{Sf}	—	300	ns	
	SDA0 input spike pulse removal time	t _{SP}	0	4 × t _{pcyc} ^{*1}	ns	
	Data input setup time	t _{SDAS}	250	—	ns	
	Data input hold time	t _{SDAH}	0	—	ns	
	SCL0, SDA0 capacitive load	C _b	—	400	pF	
Simple I ² C (Fast mode)	SCL0, SDA0 input rise time	t _{Sr}	—	300	ns	Figure 5.46
	SCL0, SDA0 input fall time	t _{Sf}	—	300	ns	
	SCL0, SDA0 input spike pulse removal time	t _{SP}	0	4 × t _{pcyc} ^{*1}	ns	
	Data input setup time	t _{SDAS}	100	—	ns	
	Data input hold time	t _{SDAH}	0	—	ns	
	SCL0, SDA0 capacitive load	C _b	—	400	pF	

Note: t_{pcyc} : PCLK cycle

Note 1. This applies when the SMR.CKS[1:0] bits = 00b and the SNFR.NFCS[2:0] bits = 010b while the SNFR.NFE bit = 1 and the digital filter is enabled.

**Figure 5.32 I/O Port Input Timing****Figure 5.33 MTU2 Input/Output Timing**

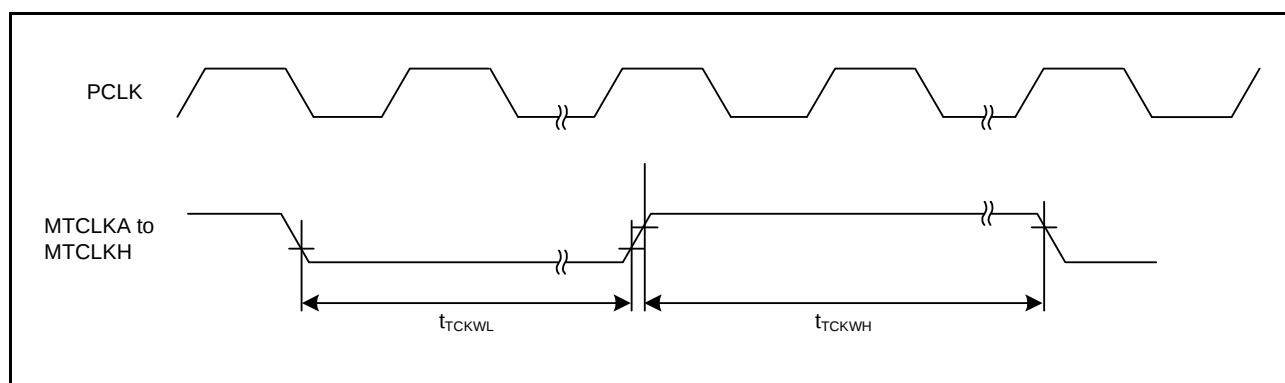


Figure 5.34 MTU2 Clock Input Timing

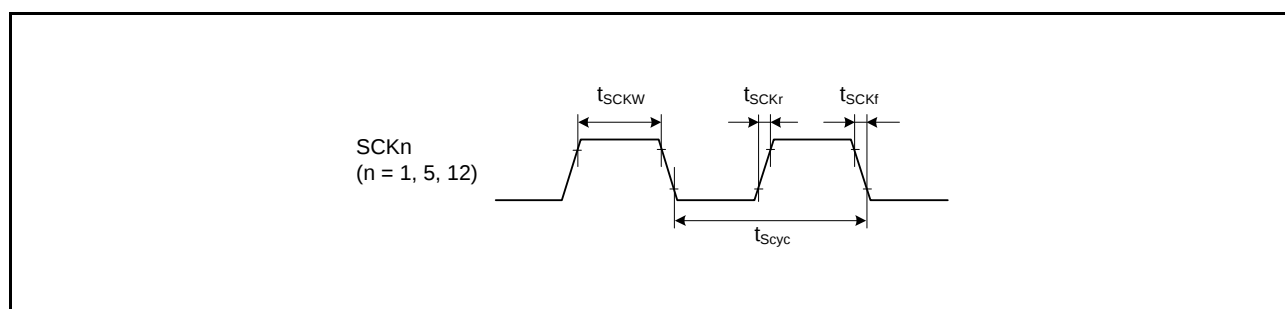


Figure 5.35 SCK Clock Input Timing

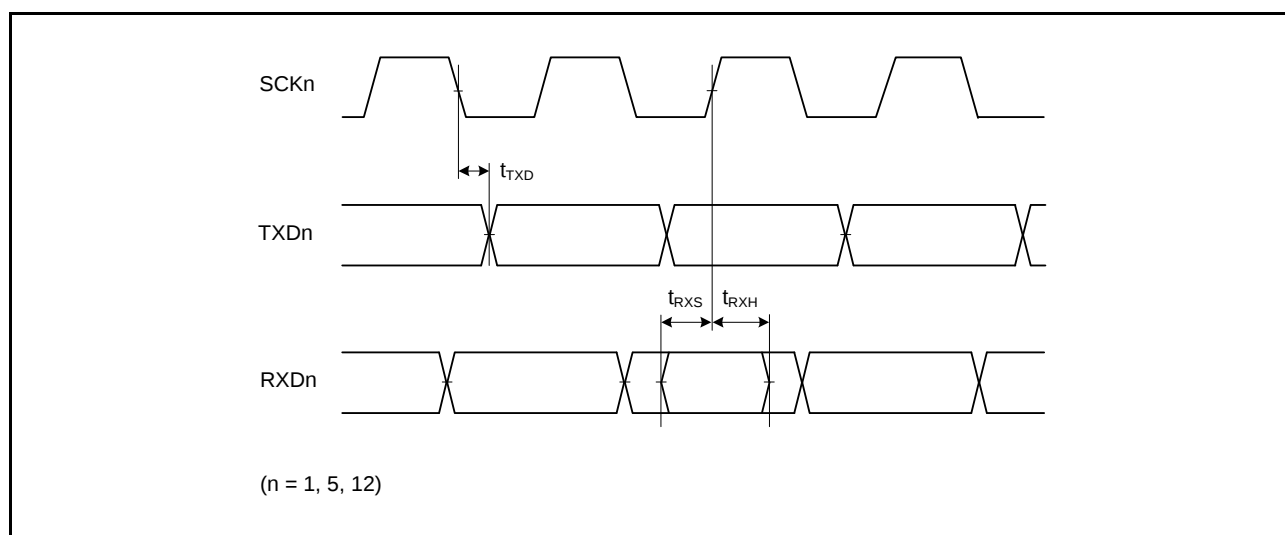


Figure 5.36 SCI Input/Output Timing: Clock Synchronous Mode

Table 5.36 A/D Conversion Characteristics (2)

Conditions: $2.4\text{ V} \leq V_{CC} \leq 3.6\text{ V}$, $2.4\text{ V} \leq AV_{CC0} \leq 3.6\text{ V}$, $2.4\text{ V} \leq V_{REFH0} \leq AV_{CC0}$, $V_{SS} = AV_{SS0} = V_{REFL0} = 0\text{ V}$,
 $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		4	—	16	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 16 MHz)	Permissible signal source impedance (Max.) = 1.0 kΩ	2.062 (0.625)*2	—	—	μs	High-precision channel ADCSR.ADHSC bit = 1 ADSSTRn.SST[7:0] bits = 09h
		2.750 (1.313)*2	—	—	μs	Normal-precision channel ADCSR.ADHSC bit = 1 ADSSTRn.SST[7:0] bits = 14h
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±0.5	±6.0	LSB	
Full-scale error		—	±1.25	±6.0	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±3.0	±8.0	LSB	
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.5	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Table 5.37 A/D Conversion Characteristics (3)

Conditions: $1.8\text{ V} \leq V_{CC} \leq 3.6\text{ V}$, $1.8\text{ V} \leq AV_{CC0} \leq 3.6\text{ V}$, $1.8\text{ V} \leq V_{REFH0} \leq AV_{CC0}$, $V_{SS} = AV_{SS0} = V_{REFL0} = 0\text{ V}$,
 $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	8	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 8 MHz)	Permissible signal source impedance (Max.) = 5.0 kΩ	4.875 (1.250)*2	—	—	μs	High-precision channel ADCSR.ADHSC bit = 0 ADSSTRn.SST[7:0] bits = 09h
		6.250 (2.625)*2	—	—		Normal-precision channel ADCSR.ADHSC bit = 0 ADSSTRn.SST[7:0] bits = 14h
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±0.5	±24.0	LSB	
Full-scale error		—	±1.25	±24.0	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±2.75	±32.0	LSB	
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.25	±12.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Table 5.38 A/D Converter Channel Classification

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN004, AN006	AVCC0 = 1.8 to 3.6 V	Pins AN000 to AN004 and AN006 cannot be used as digital outputs when the A/D converter is in use.
Normal-precision channel	AN008 to AN015		
Internal reference voltage input channel	Internal reference voltage	AVCC0 = 2.0 to 3.6 V	
Temperature sensor input channel	Temperature sensor output	AVCC0 = 2.0 to 3.6 V	

Table 5.39 A/D Internal Reference Voltage Characteristics

Conditions: $2.0\text{ V} \leq VCC \leq 3.6\text{ V}$, $2.0\text{ V} \leq AVCC0 \leq 3.6\text{ V}^{*1}$, $VSS = AVSS0 = VREFL0 = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
Internal reference voltage input channel*2	1.36	1.43	1.50	V	

Note 1. The internal reference voltage cannot be selected for input channels when $AVCC0 < 2.0\text{ V}$.

Note 2. The A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the A/D converter.

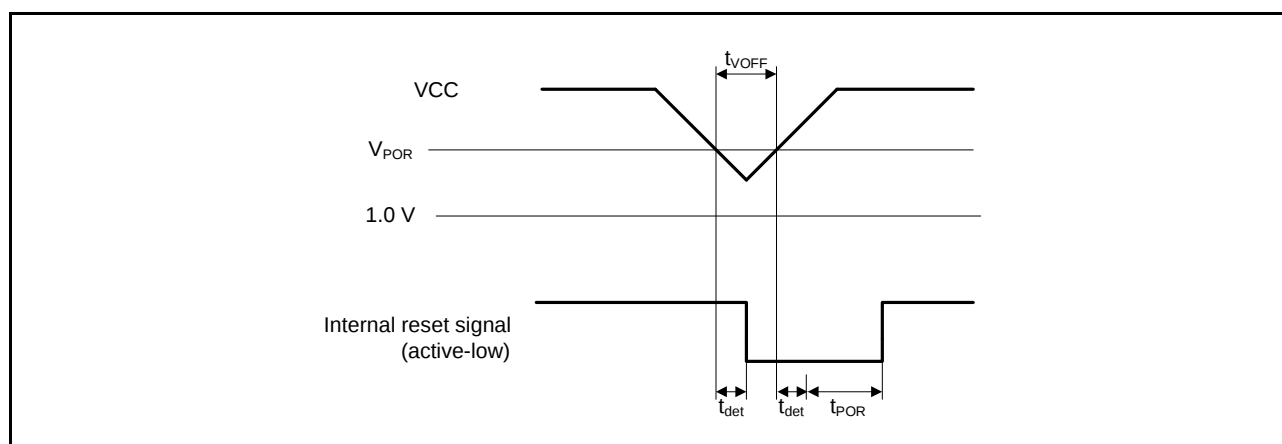


Figure 5.49 Voltage Detection Reset Timing

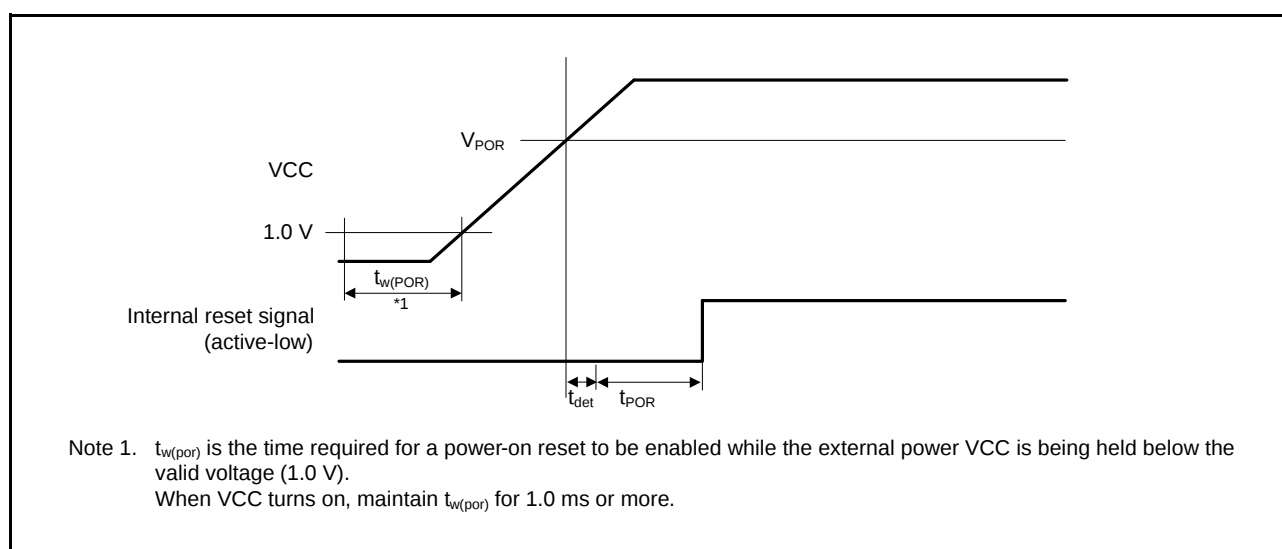


Figure 5.50 Power-On Reset Timing

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

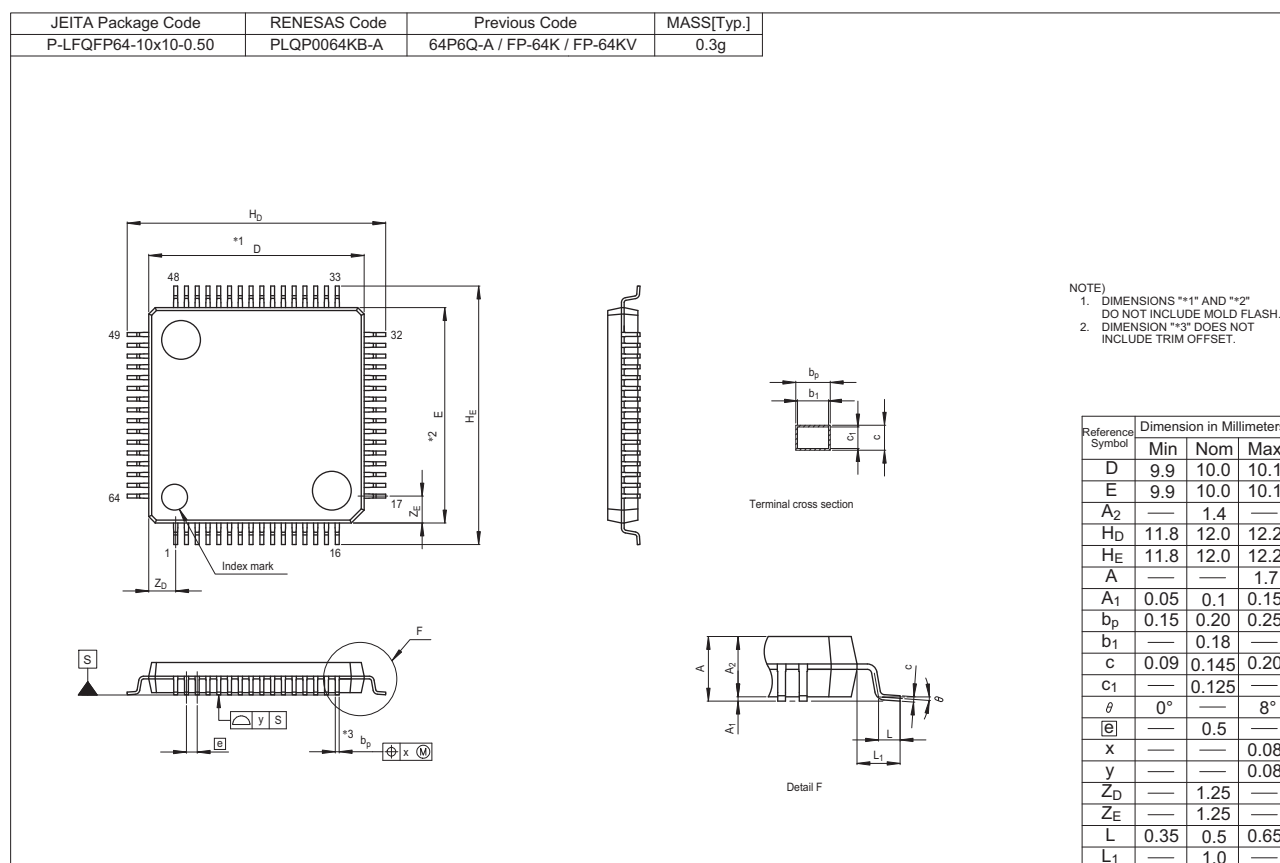


Figure A 64-Pin LFQFP (PLQP0064KB-A)