Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, PWM, WDT
Number of I/O	51
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l475rct3

3 Functional overview

3.1 ARM® Cortex®-M4 core with FPU

The ARM® Cortex®-M4 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded ARM core, the STM32L475xx family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the STM32L475xx family devices.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex®-M4 processors. It balances the inherent performance advantage of the ARM® Cortex®-M4 over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor near 100 DMIPS performance at 80MHz, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 64-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 80 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

Table 4. STM32L475 modes overview (continued)

Mode	Regulator (1)	CPU	Flash	SRAM	Clocks	DMA & Peripherals(2)	Wakeup source	Consumption(3)	Wakeup time
Standby	LPR	Powered Off	Off	SRAM2 ON	LSE LSI	BOR, RTC, IWDG *** All other peripherals are powered off. *** I/O configuration can be floating, pull-up or pull-down	Reset pin 5 I/Os (WKUPx)(10) BOR, RTC, IWDG	0.35 µA w/o RTC 0.65 µA w/ RTC	14 µs
	OFF			Powered Off				0.12 µA w/o RTC 0.42 µA w/ RTC	
Shutdown	OFF	Powered Off	Off	Powered Off	LSE	RTC *** All other peripherals are powered off. *** I/O configuration can be floating, pull-up or pull-down(11)	Reset pin 5 I/Os (WKUPx)(10) RTC	0.03 µA w/o RTC 0.33 µA w/ RTC	256 µs

1. LPR means Main regulator is OFF and Low-power regulator is ON.
2. All peripherals can be active or clock gated to save power consumption.
3. Typical current at V_{DD} = 1.8 V, 25°C. Consumptions values provided running from SRAM, Flash memory Off, 80 MHz in Range 1, 26 MHz in Range 2, 2 MHz in LPRun/LPSleep.
4. The Flash memory can be put in power-down and its clock can be gated off when executing from SRAM.
5. The SRAM1 and SRAM2 clocks can be gated on or off independently.
6. U(S)ART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
7. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
8. OTG_FS wakeup by resume from suspend and attach detection protocol event.
9. SWPMI1 wakeup by resume from suspend.
10. The I/Os with wakeup from Standby/Shutdown capability are: PA0, PC13, PE6, PA2, PC5.
11. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

Standby mode, supplied by the low-power Regulator (Standby with RAM2 retention mode).

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper) or a failure is detected on LSE (CSS on LSE).

The system clock after wakeup is MSI up to 8 MHz.

- **Shutdown** mode

  The Shutdown mode allows to achieve the lowest power consumption. The internal regulator is switched off so that the VCORE domain is powered off. The PLL, the HSI16, the MSI, the LSI and the HSE oscillators are also switched off.

  The RTC can remain active (Shutdown mode with RTC, Shutdown mode without RTC).

  The BOR is not available in Shutdown mode. No power voltage monitoring is possible in this mode, therefore the switch to Backup domain is not supported.

  SRAM1, SRAM2 and register contents are lost except for registers in the Backup domain.

  The device exits Shutdown mode when an external reset (NRST pin), a WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper).

  The system clock after wakeup is MSI at 4 MHz.

3.15 Analog to digital converter (ADC)

The device embeds 3 successive approximation analog-to-digital converters with the following features:

- 12-bit native resolution, with built-in calibration
- 5.33 Msps maximum conversion rate with full resolution
  - Down to 18.75 ns sampling time
  - Increased conversion rate for lower resolution (up to 8.88 Msps for 6-bit resolution)
- Up to 16 external channels, some of them shared between ADC1 and ADC2, or ADC1, ADC2 and ADC3.
- 5 Internal channels: internal reference voltage, temperature sensor, VBAT/3, DAC1 and DAC2 outputs.
- One external reference pin is available on some package, allowing the input voltage range to be independent from the power supply
- Single-ended and differential mode inputs
- Low-power design
  - Capable of low-current operation at low conversion rate (consumption decreases linearly with speed)
  - Dual clock domain architecture: ADC speed independent from CPU frequency
- Highly versatile digital interface
  - Single-shot or continuous/discontinuous sequencer-based scan mode: 2 groups of analog signals conversions can be programmed to differentiate background and high-priority real-time conversions
  - Handles two ADC converters for dual mode operation (simultaneous or interleaved sampling modes)
  - Each ADC support multiple trigger inputs for synchronization with on-chip timers and external signals
  - Results stored into 3 data register or in RAM with DMA controller support
  - Data pre-processing: left/right alignment and per channel offset compensation
  - Built-in oversampling unit for enhanced SNR
  - Channel-wise programmable sampling time
  - Three analog watchdog for automatic voltage monitoring, generating interrupts and trigger for selected timers
  - Hardware assistant to prepare the context of the injected channels to allow fast context switching

3.15.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{TS} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC1_IN17 and ADC3_IN17 input channels which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

3.26 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32L475xx devices have three embedded universal synchronous receiver transmitters (USART1, USART2 and USART3) and two universal asynchronous receiver transmitters (UART4, UART5).

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. They provide hardware management of the CTS and RTS signals, and RS485 Driver Enable. They are able to communicate at speeds of up to 10Mbit/s.

USART1, USART2 and USART3 also provide Smart Card mode (ISO 7816 compliant) and SPI-like communication capability.

All USART have a clock domain independent from the CPU clock, allowing the USARTx (x=1,2,3,4,5) to wake up the MCU from Stop mode using baudrates up to 200 Kbaud.The wake up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

All USART interfaces can be served by the DMA controller.

Table 12. STM32L475xx USART/UART/LPUART features

USART modes/features(1)	USART1	USART2	USART3	UART4	UART5	LPUART1
Hardware flow control for modem	X	X	X	X	X	X
Continuous communication using DMA	X	X	X	X	X	X
Multiprocessor communication	X	X	X	X	X	X
Synchronous mode	X	X	X	-	-	-
Smartcard mode	X	X	X	-	-	-
Single-wire half-duplex communication	X	X	X	X	X	X
IrDA SIR ENDEC block	X	X	X	X	X	-
LIN mode	X	X	X	X	X	-
Dual clock domain	X	X	X	X	X	X
Wakeup from Stop 0 / Stop 1 modes	X	X	X	X	X	X
Wakeup from Stop 2 mode	-	-	-	-	-	X
Receiver timeout interrupt	X	X	X	X	X	-
Modbus communication	X	X	X	X	X	-
Auto baud rate detection	X (4 modes)					-
Driver Enable	X	X	X	X	X	X
LPUART/USART data length	7, 8 and 9 bits					

1. X = supported.

- Transmission
  - Three transmit mailboxes
  - Configurable transmit priority
- Reception
  - Two receive FIFOs with three stages
  - 14 Scalable filter banks
  - Identifier list feature
  - Configurable FIFO overrun
- Time-triggered communication option
  - Disable automatic retransmission mode
  - 16-bit free running timer
  - Time Stamp sent in last two data bytes
- Management
  - Maskable interrupts
  - Software-efficient mailbox mapping at a unique address space

3.32 Secure digital input/output and MultiMediaCards Interface (SDMMC)

The card host interface (SDMMC) provides an interface between the APB peripheral bus and MultiMediaCards (MMCs), SD memory cards and SDIO cards.

The SDMMC features include the following:

- Full compliance with MultiMediaCard System Specification Version 4.2. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit
- Full compatibility with previous versions of MultiMediaCards (forward compatibility)
- Full compliance with SD Memory Card Specifications Version 2.0
- Full compliance with SD I/O Card Specification Version 2.0: card support for two different databus modes: 1-bit (default) and 4-bit
- Data transfer up to 48 MHz for the 8 bit mode
- Data write and read with DMA capability

3.33 Universal serial bus on-the-go full-speed (OTG_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG controller requires a dedicated 48 MHz clock that can be provided by the internal multispeed oscillator (MSI) automatically trimmed by 32.768 kHz external oscillator (LSE).This allows to use the USB device without external high speed crystal (HSE).

3.36 Development support

3.36.1 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.36.2 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32L475xx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. Real-time instruction and data flow activity be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

Table 15. STM32L475xx pin definitions (continued)

Pin Number		Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP100					Alternate functions	Additional functions
26	35	PB0	I/O	TT_a	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, USART3_CK, QUADSPI_BK1_IO1, COMP1_OUT, EVENTOUT	OPAMP2_ VOUT, ADC12_IN15
27	36	PB1	I/O	FT_a	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, DFSDM_DATIN0, USART3_RTS_DE, QUADSPI_BK1_IO0, LPTIM2_IN1, EVENTOUT	COMP1_INM, ADC12_IN16
28	37	PB2	I/O	FT_a	-	RTC_OUT, LPTIM1_OUT, I2C3_SMBA, DFSDM_CKIN0, EVENTOUT	COMP1_INP
-	38	PE7	I/O	FT	-	TIM1_ETR, DFSDM_DATIN2, FMC_D4, SAI1_SD_B, EVENTOUT	-
-	39	PE8	I/O	FT	-	TIM1_CH1N, DFSDM_CKIN2, FMC_D5, SAI1_SCK_B, EVENTOUT	-
-	40	PE9	I/O	FT	-	TIM1_CH1, DFSDM_CKOUT, FMC_D6, SAI1_FS_B, EVENTOUT	-
-	41	PE10	I/O	FT	-	TIM1_CH2N, DFSDM_DATIN4, TSC_G5_IO1, FMC_D7, QUADSPI_CLK, SAI1_MCLK_B, EVENTOUT	-
-	42	PE11	I/O	FT	-	TIM1_CH2, DFSDM_CKIN4, TSC_G5_IO2, QUADSPI_NCS, FMC_D8, EVENTOUT	-
-	43	PE12	I/O	FT	-	TIM1_CH3N, SPI1_NSS, DFSDM_DATIN5, TSC_G5_IO3, QUADSPI_BK1_IO0, FMC_D9, EVENTOUT	-
-	44	PE13	I/O	FT	-	TIM1_CH3, SPI1_SCK, DFSDM_CKIN5, TSC_G5_IO4, QUADSPI_BK1_IO1, FMC_D10, EVENTOUT	-

Table 15. STM32L475xx pin definitions (continued)

Pin Number		Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP100					Alternate functions	Additional functions
50	77	PA15 (JTDI)	I/O	FT	(3)	JTDI, TIM2_CH1, TIM2_ETR, SPI1_NSS, SPI3_NSS, UART4_RTS_DE, TSC_G3_IO1, SAI2_FS_B, EVENTOUT	-
51	78	PC10	I/O	FT	-	SPI3_SCK, USART3_TX, UART4_TX, TSC_G3_IO2, SDMMC1_D2, SAI2_SCK_B, EVENTOUT	-
52	79	PC11	I/O	FT	-	SPI3_MISO, USART3_RX, UART4_RX, TSC_G3_IO3, SDMMC1_D3, SAI2_MCLK_B, EVENTOUT	-
53	80	PC12	I/O	FT	-	SPI3_MOSI, USART3_CK, UART5_TX, TSC_G3_IO4, SDMMC1_CK, SAI2_SD_B, EVENTOUT	-
-	81	PD0	I/O	FT	-	SPI2_NSS, DFSDM_DATIN7, CAN1_RX, FMC_D2, EVENTOUT	-
-	82	PD1	I/O	FT	-	SPI2_SCK, DFSDM_CKIN7, CAN1_TX, FMC_D3, EVENTOUT	-
54	83	PD2	I/O	FT	-	TIM3_ETR, USART3_RTS_DE, UART5_RX, TSC_SYNC, SDMMC1_CMD, EVENTOUT	-
-	84	PD3	I/O	FT	-	SPI2_MISO, DFSDM_DATIN0, USART2_CTS, FMC_CLK, EVENTOUT	-
-	85	PD4	I/O	FT	-	SPI2_MOSI, DFSDM_CKIN0, USART2_RTS_DE, FMC_NOE, EVENTOUT	-
-	86	PD5	I/O	FT	-	USART2_TX, FMC_NWE, EVENTOUT	-
-	87	PD6	I/O	FT	-	DFSDM_DATIN1, USART2_RX, FMC_NWAIT, SAI1_SD_A, EVENTOUT	-
-	88	PD7	I/O	FT	-	DFSDM_CKIN1, USART2_CK, FMC_NE1, EVENTOUT	-

Table 16. Alternate function AF0 to AF7 (for AF8 to AF15 see *Table 17*)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2/ TIM5/TIM8/ LPTIM1	TIM1/TIM2/ TIM3/TIM4/ TIM5	TIM8	I2C1/I2C2/I2C3	SPI1/SPI2	SPI3/DFSDM	USART1/ USART2/ USART3
Port A	PA0	-	TIM2_CH1	TIM5_CH1	TIM8_ETR	-	-	-	USART2_CTS
	PA1	-	TIM2_CH2	TIM5_CH2	-	-	-	-	USART2_RTS_ DE
	PA2	-	TIM2_CH3	TIM5_CH3	-	-	-	-	USART2_TX
	PA3	-	TIM2_CH4	TIM5_CH4	-	-	-	-	USART2_RX
	PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS	USART2_CK
	PA5	-	TIM2_CH1	TIM2_ETR	TIM8_CH1N	-	SPI1_SCK	-	-
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO	-	USART3_CTS
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI	-	-
	PA8	MCO	TIM1_CH1	-	-	-	-	-	USART1_CK
	PA9	-	TIM1_CH2	-	-	-	-	-	USART1_TX
	PA10	-	TIM1_CH3	-	-	-	-	-	USART1_RX
	PA11	-	TIM1_CH4	TIM1_BKIN2	-	-	-	-	USART1_CTS
	PA12	-	TIM1_ETR	-	-	-	-	-	USART1_RTS_ DE
	PA13	JTMS-SWDIO	IR_OUT	-	-	-	-	-	-
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-
	PA15	JTDI	TIM2_CH1	TIM2_ETR	-	-	SPI1_NSS	SPI3_NSS	-

Table 18. STM32L475xx memory map and peripheral register boundary addresses (continued)[1]

Bus	Boundary address	Size (bytes)	Peripheral
APB1	0x4000 4000 - 0x4000 43FF	1 KB	Reserved
	0x4000 3C00 - 0x4000 3FFF	1 KB	SPI3
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 1800 - 0x4000 27FF	4 KB	Reserved
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 0C00- 0x4000 0FFF	1 KB	TIM5
	0x4000 0800 - 0x4000 0BFF	1 KB	TIM4
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2

1. The gray color is used for reserved boundary addresses.

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 46*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 46. HSE oscillator characteristics(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	48	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup(3)	-	-	5.5	mA
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@8 MHz	-	0.44	-	
		V_{DD} = 3 V, Rm = 45 Ω, CL = 10 pF@8 MHz	-	0.45	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 5 pF@48 MHz	-	0.68	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@48 MHz	-	0.94	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 20 pF@48 MHz	-	1.77	-	
G_m	Maximum critical crystal transconductance	Startup	-	-	1.5	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 15*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Multi-speed internal (MSI) RC oscillator

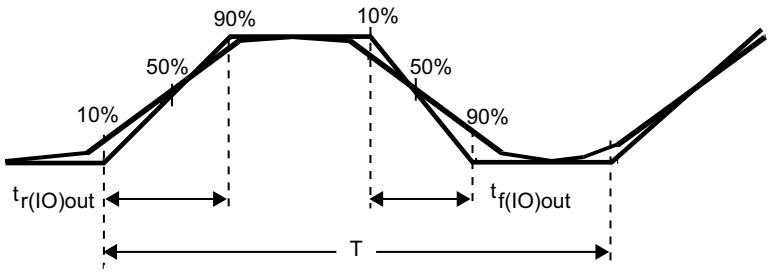
Table 49. MSI oscillator characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{MSI}	MSI frequency after factory calibration, done at V_{DD}=3 V and T_A=30 °C	MSI mode	Range 0	99	100	101	kHz
			Range 1	198	200	202	
			Range 2	396	400	404	
			Range 3	792	800	808	
			Range 4	0.99	1	1.01	MHz
			Range 5	1.98	2	2.02	
			Range 6	3.96	4	4.04	
			Range 7	7.92	8	8.08	
			Range 8	15.8	16	16.16	
			Range 9	23.8	24	24.4	
			Range 10	31.7	32	32.32	
			Range 11	47.5	48	48.48	
		PLL mode XTAL= 32.768 kHz	Range 0	-	98.304	-	kHz
			Range 1	-	196.608	-	
			Range 2	-	393.216	-	
			Range 3	-	786.432	-	
			Range 4	-	1.016	-	MHz
			Range 5	-	1.999	-	
			Range 6	-	3.998	-	
			Range 7	-	7.995	-	
			Range 8	-	15.991	-	
			Range 9	-	23.986	-	
			Range 10	-	32.014	-	
			Range 11	-	48.005	-	
Δ_{TEMP}(MSI)(2)	MSI oscillator frequency drift over temperature	MSI mode	T_A= -0 to 85 °C	-3.5	-	3	%
			T_A= -40 to 125 °C	-8	-	6	

Table 61. I/O AC characteristics(1)(2)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	5	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	1	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	0.1	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	10	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	1.5	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	0.1	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	25	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	52	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	140	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	17	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	37	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	110	
01	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	25	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	10	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	1	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	50	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	15	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	1	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	9	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	16	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	40	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	4.5	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	9	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	21	

Figure 20. I/O AC characteristics definition(1)



Maximum frequency is achieved if (t_r + t_f (≤ 2/3)T and if the duty cycle is (45-55%) when loaded by the specified capacitance.

MS32132V2

1. Refer to *Table 61: I/O AC characteristics*.

6.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 62. NRST pin characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	$0.3 \times V_{DDIOx}$	V
$V_{IH(NRST)}$	NRST input high level voltage	-	$0.7 \times V_{DDIOx}$	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	70	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	1.71 V ≤ V_{DD} ≤ 3.6 V	350	-	-	ns

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

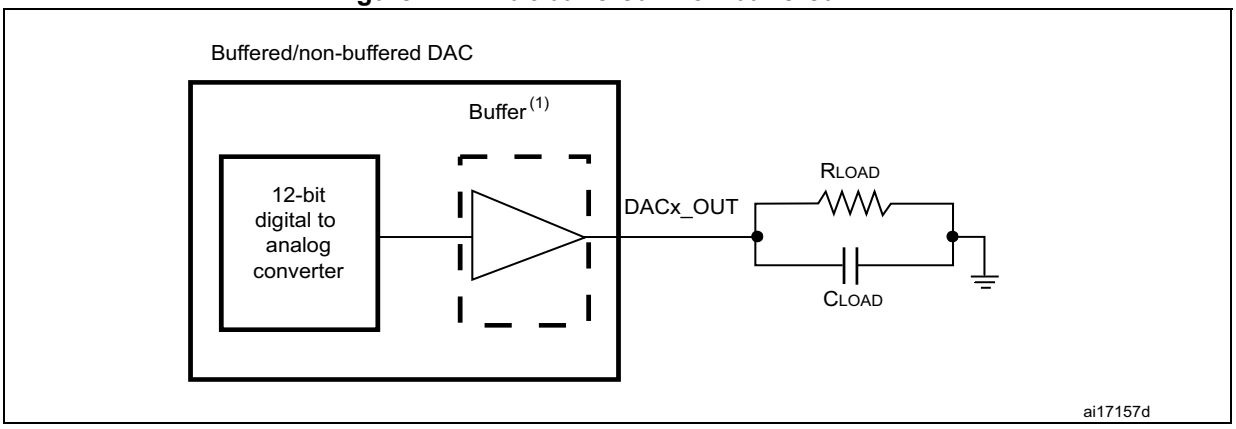
Table 65. Maximum ADC RAIN(1)(2) (continued)

Resolution	Sampling cycle @80 MHz	Sampling time [ns] @80 MHz	RAIN max (Ω)	
			Fast channels(3)	Slow channels(4)
6 bits	2.5	31.25	220	N/A
	6.5	81.25	560	330
	12.5	156.25	1200	1000
	24.5	306.25	2700	2200
	47.5	593.75	3900	3300
	92.5	1156.25	8200	6800
	247.5	3093.75	18000	15000
	640.5	8006.75	50000	50000

1. Guaranteed by design.
2. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4V). It is disable when V_{DDA} ≥ 2.4 V.
3. Fast channels are: PC0, PC1, PC2, PC3, PA0, PA1.
4. Slow channels are: all ADC inputs except the fast channels.

3. Refer to *Table 59: I/O static characteristics*.
4. Ton is the Refresh phase duration. Toff is the Hold phase duration. Refer to RM0395 reference manual for more details.

Figure 24. 12-bit buffered / non-buffered DAC

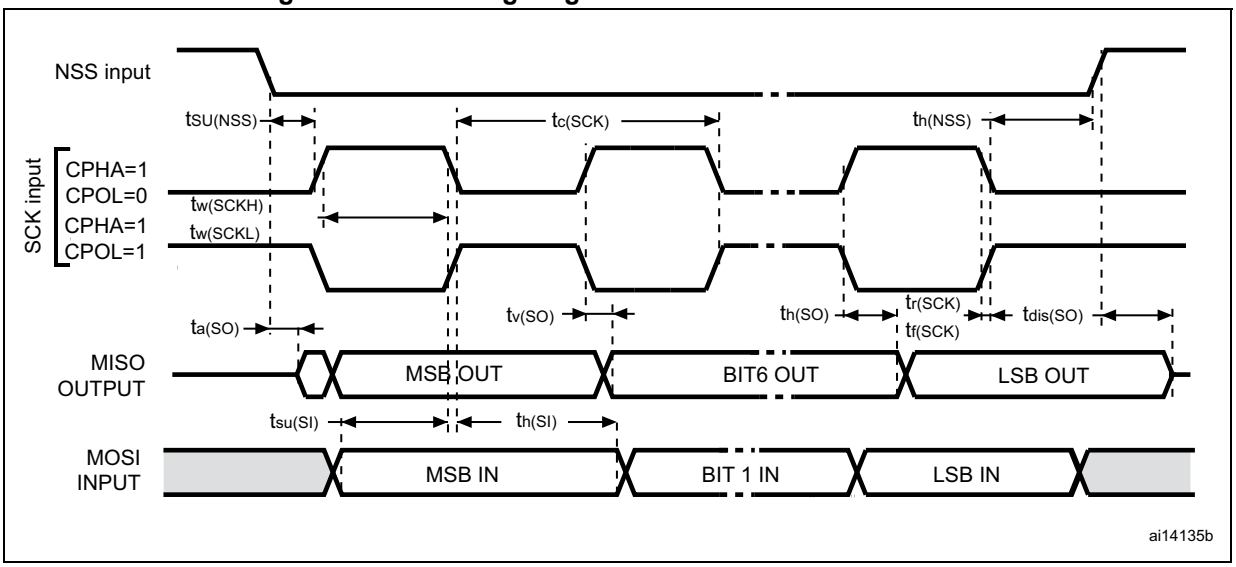


1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

Table 71. DAC accuracy(1)

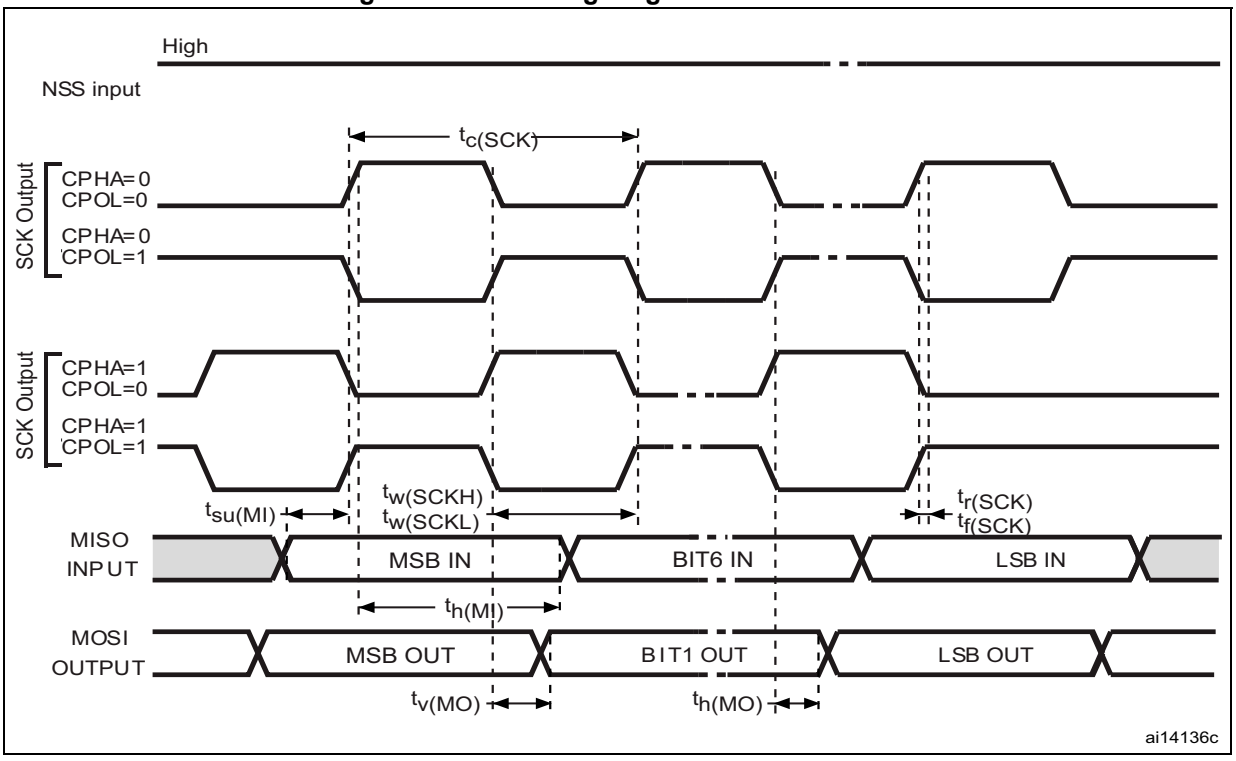
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DNL	Differential non linearity (2)	DAC output buffer ON		-	-	±2	LSB
		DAC output buffer OFF		-	-	±2	
-	monotonicity	10 bits		guaranteed			
INL	Integral non linearity(3)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±4	
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±4	
Offset	Offset error at code 0x800(3)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 3.6 V	-	-	±12	
			V_{REF+} = 1.8 V	-	-	±25	
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±8	
Offset1	Offset error at code 0x001(4)	DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±5	
OffsetCal	Offset Error at code 0x800 after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 3.6 V	-	-	±5	
			V_{REF+} = 1.8 V	-	-	±7	

Figure 26. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 27. SPI timing diagram - master mode



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 36. Synchronous multiplexed NOR/PSRAM read timings

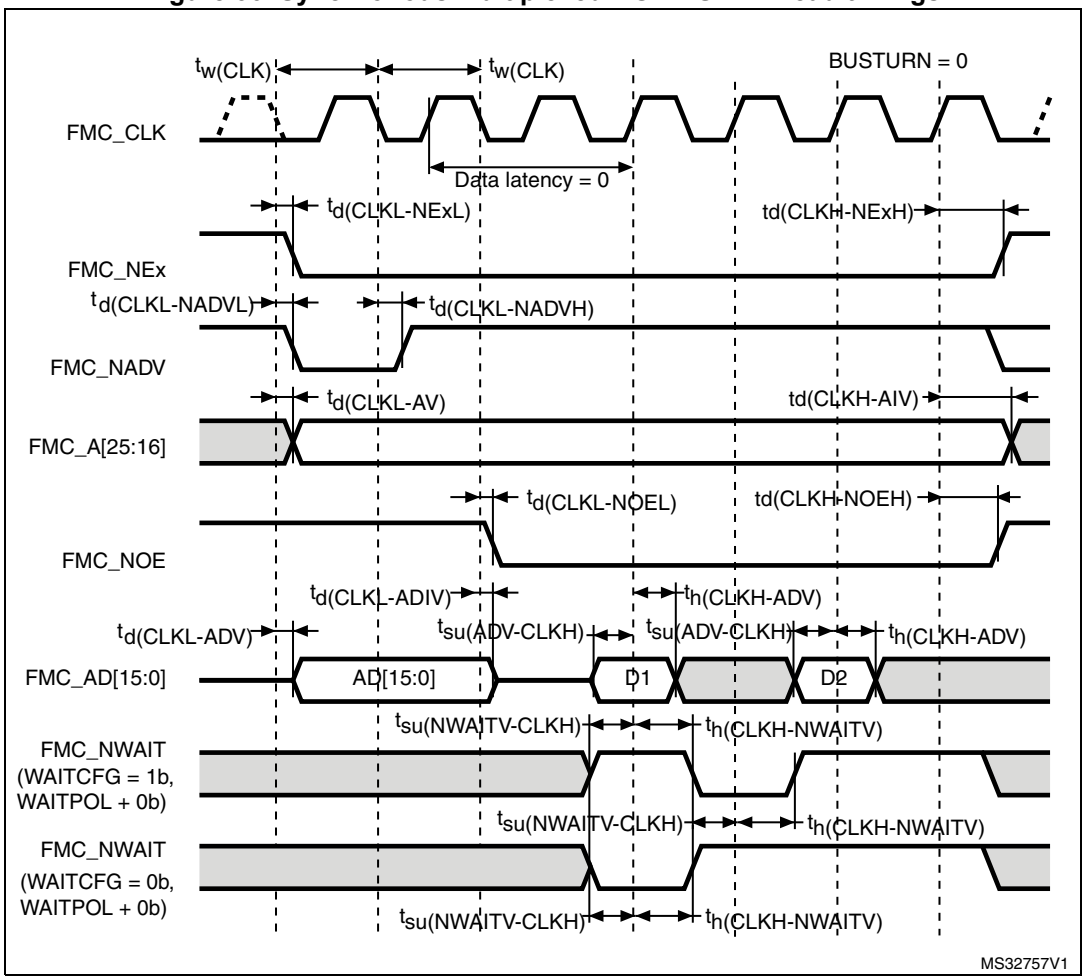


Table 96. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.