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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, PWM, WDT
Number of I/O	51
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l475rct6

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L475xx microcontrollers.

This document should be read in conjunction with the STM32L4x5 reference manual (RM0395). The reference manual is available from the STMicroelectronics website *www.st.com*.

For information on the ARM® Cortex®-M4 core, please refer to the Cortex®-M4 Technical Reference Manual, available from the www.arm.com website.

3 Functional overview

3.1 ARM® Cortex®-M4 core with FPU

The ARM® Cortex®-M4 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded ARM core, the STM32L475xx family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the STM32L475xx family devices.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex®-M4 processors. It balances the inherent performance advantage of the ARM® Cortex®-M4 over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor near 100 DMIPS performance at 80MHz, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 64-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 80 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.4 Embedded Flash memory

STM32L475xx devices feature up to 1 Mbyte of embedded Flash memory available for storing programs and data. The Flash memory is divided into two banks allowing read-while-write operations. This feature allows to perform a read operation from one bank while an erase or program operation is performed to the other bank. The dual bank boot is also supported. Each bank contains 256 pages of 2 Kbyte.

Flexible protections can be configured thanks to option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels are available:
  - Level 0: no readout protection
  - Level 1: memory readout protection: the Flash memory cannot be read from or written to if either debug features are connected, boot in RAM or bootloader is selected
  - Level 2: chip readout protection: debug features (Cortex-M4 JTAG and serial wire), boot in RAM and bootloader selection are disabled (JTAG fuse). This selection is irreversible.

Table 3. Access status versus readout protection level and execution modes

Area	Protection level	User execution			Debug, boot from RAM or boot from system memory (loader)		
		Read	Write	Erase	Read	Write	Erase
Main memory	1	Yes	Yes	Yes	No	No	No
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes	1	Yes	Yes	Yes	Yes	Yes	Yes
	2	Yes	No	No	N/A	N/A	N/A
Backup registers	1	Yes	Yes	N/A(1)	No	No	N/A(1)
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2	1	Yes	Yes	Yes(1)	No	No	No(1)
	2	Yes	Yes	Yes	N/A	N/A	N/A

1. Erased when RDP change from Level 1 to Level 0.

- Write protection (WRP): the protected area is protected against erasing and programming. Two areas per bank can be selected, with 2-Kbyte granularity.
- Proprietary code readout protection (PCROP): a part of the flash memory can be protected against read and write from third parties. The protected area is execute-only: it can only be reached by the STM32 CPU, as an instruction code, while all other accesses (DMA, debug and CPU data read, write and erase) are strictly prohibited. One area per bank can be selected, with 64-bit granularity. An additional option bit (PCROP_RDP) allows to select if the PCROP area is erased or not when the RDP protection is changed from Level 1 to Level 0.

Table 6. STM32L475xx peripherals interconnect matrix (continued)

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop 0 / Stop 1	Stop 2
GPIO	TIMx	External trigger	Y	Y	Y	Y	-	-
	LPTIMERx	External trigger	Y	Y	Y	Y	Y	Y (1)
	ADCx DACx DFSDM	Conversion external trigger	Y	Y	Y	Y	-	-

1. LPTIM1 only.

3.14 Interrupts and events

3.14.1 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 81 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.14.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 36 edge detector lines used to generate interrupt/event requests and wake-up the system from Stop mode. Each external line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently A pending register maintains the status of the interrupt requests. The internal lines are connected to peripherals with wakeup from Stop mode capability. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 114 GPIOs can be connected to the 16 external interrupt lines.

All comparators can wake up from Stop mode, generate interrupts and breaks for the timers and can be also combined into a window comparator.

3.19 Operational amplifier (OPAMP)

The STM32L475xx embeds two operational amplifiers with external or internal follower routing and PGA capability.

The operational amplifier features:

- Low input bias current
- Low offset voltage
- Low-power mode
- Rail-to-rail input

3.20 Touch sensing controller (TSC)

The touch sensing controller provides a simple solution for adding capacitive sensing functionality to any application. Capacitive sensing technology is able to detect finger presence near an electrode which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

The main features of the touch sensing controller are the following:

- Proven and robust surface charge transfer acquisition principle
- Supports up to 21 capacitive sensing channels
- Up to 3 capacitive sensing channels can be acquired in parallel offering a very good response time
- Spread spectrum feature to improve system robustness in noisy environments
- Full hardware management of the charge transfer acquisition sequence
- Programmable charge transfer frequency
- Programmable sampling capacitor I/O pin
- Programmable channel I/O pin
- Programmable max count value to avoid long acquisition when a channel is faulty
- Dedicated end of acquisition and max count error flags with interrupt capability
- One sampling capacitor for up to 3 capacitive sensing channels to reduce the system components
- Compatible with proximity, touchkey, linear and rotary touch sensor implementation
- Designed to operate with STMTouch touch sensing firmware library

Note: The number of capacitive sensing channels is dependent on the size of the packages and subject to I/O availability.

The major features are:

- Combined Rx and Tx FIFO size of 1.25 KB with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 1 bidirectional control endpoint + 5 IN endpoints + 5 OUT endpoints
- 8 host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- Software configurable to OTG 1.3 and OTG 2.0 modes of operation
- OTG 2.0 Supports ADP (Attach detection Protocol)
- USB 2.0 LPM (Link Power Management) support
- Battery Charging Specification Revision 1.2 support
- Internal FS OTG PHY support

For OTG/Host modes, a power switch is needed in case bus-powered devices are connected.

3.34 Flexible static memory controller (FSMC)

Flexible static memory controller (FSMC) is also named Flexible memory controller (FMC).

The main features of the FMC controller are the following:

- Interface with static-memory mapped devices in multiplexed mode including:
  - Static random access memory (SRAM)
  - NOR Flash memory
  - PSRAM
- 8-,16- bit data bus width
- Write FIFO
- The Maximum FMC_CLK frequency for synchronous accesses is HCLK/2.

LCD parallel interface

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

3.35 Quad SPI memory interface (QUADSPI)

The Quad SPI is a specialized communication interface targeting single, dual or quad SPI flash memories. It can operate in any of the three following modes:

- Indirect mode: all the operations are performed using the QUADSPI registers
- Status polling mode: the external flash status register is periodically read and an interrupt can be generated in case of flag setting
- Memory-mapped mode: the external flash is memory mapped and is seen by the system as if it were an internal memory

Table 15. STM32L475xx pin definitions (continued)

Pin Number		Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP100					Alternate functions	Additional functions
35	53	PB14	I/O	FT_f	-	TIM1_CH2N, TIM8_CH2N, I2C2_SDA, SPI2_MISO, DFSDM_DATIN2, USART3_RTS_DE, TSC_G1_IO3, SWPMI1_RX, SAI2_MCLK_A, TIM15_CH1, EVENTOUT	-
36	54	PB15	I/O	FT	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, SPI2_MOSI, DFSDM_CKIN2, TSC_G1_IO4, SWPMI1_SUSPEND, SAI2_SD_A, TIM15_CH2, EVENTOUT	-
-	55	PD8	I/O	FT	-	USART3_TX, FMC_D13, EVENTOUT	-
-	56	PD9	I/O	FT	-	USART3_RX, FMC_D14, SAI2_MCLK_A, EVENTOUT	-
-	57	PD10	I/O	FT	-	USART3_CK, TSC_G6_IO1, FMC_D15, SAI2_SCK_A, EVENTOUT	-
-	58	PD11	I/O	FT	-	USART3_CTS, TSC_G6_IO2, FMC_A16, SAI2_SD_A, LPTIM2_ETR, EVENTOUT	-
-	59	PD12	I/O	FT	-	TIM4_CH1, USART3_RTS_DE, TSC_G6_IO3, FMC_A17, SAI2_FS_A, LPTIM2_IN1, EVENTOUT	-
-	60	PD13	I/O	FT	-	TIM4_CH2, TSC_G6_IO4, FMC_A18, LPTIM2_OUT, EVENTOUT	-
-	61	PD14	I/O	FT	-	TIM4_CH3, FMC_D0, EVENTOUT	-
-	62	PD15	I/O	FT	-	TIM4_CH4, FMC_D1, EVENTOUT	-
37	63	PC6	I/O	FT	-	TIM3_CH1, TIM8_CH1, DFSDM_CKIN3, TSC_G4_IO1, SDMMC1_D6, SAI2_MCLK_A, EVENTOUT	-

Table 16. Alternate function AF0 to AF7 (for AF8 to AF15 see *Table 17*) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2/ TIM5/TIM8/ LPTIM1	TIM1/TIM2/ TIM3/TIM4/ TIM5	TIM8	I2C1/I2C2/I2C3	SPI1/SPI2	SPI3/DFSDM	USART1/ USART2/ USART3
Port C	PC0	-	LPTIM1_IN1	-	-	I2C3_SCL	-	DFSDM_DATIN4	-
	PC1	-	LPTIM1_OUT	-	-	I2C3_SDA	-	DFSDM_CKIN4	-
	PC2	-	LPTIM1_IN2	-	-	-	SPI2_MISO	DFSDM_CKOUT	-
	PC3	-	LPTIM1_ETR	-	-	-	SPI2_MOSI	-	-
	PC4	-	-	-	-	-	-	-	USART3_TX
	PC5	-	-	-	-	-	-	-	USART3_RX
	PC6	-	-	TIM3_CH1	TIM8_CH1	-	-	DFSDM_CKIN3	-
	PC7	-	-	TIM3_CH2	TIM8_CH2	-	-	DFSDM_DATIN3	-
	PC8	-	-	TIM3_CH3	TIM8_CH3	-	-	-	-
	PC9	-	TIM8_BKIN2	TIM3_CH4	TIM8_CH4	-	-	-	-
	PC10	-	-	-	-	-	-	SPI3_SCK	USART3_TX
	PC11	-	-	-	-	-	-	SPI3_MISO	USART3_RX
	PC12	-	-	-	-	-	-	SPI3_MOSI	USART3_CK
	PC13	-	-	-	-	-	-	-	-
	PC14	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-

Table 17. Alternate function AF8 to AF15 (for AF0 to AF7 see *Table 16*) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4, UART5, LPUART1	CAN1, TSC	OTG_FS, QUADSPI	-	SDMMC1, COMP1, COMP2, FMC, SWPMI1	SAI1, SAI2	TIM2, TIM15, TIM16, TIM17, LPTIM2	EVENTOUT
Port B	PB0	-	-	QUADSPI_BK1_IO1	-	COMP1_OUT	-	-	EVENTOUT
	PB1	-	-	QUADSPI_BK1_IO0	-	-	-	LPTIM2_IN1	EVENTOUT
	PB2	-	-	-	-	-	-	-	EVENTOUT
	PB3	-	-	-	-	-	SAI1_SCK_B	-	EVENTOUT
	PB4	UART5_RTS_DE	TSC_G2_IO1	-	-	-	SAI1_MCLK_B	TIM17_BKIN	EVENTOUT
	PB5	UART5_CTS	TSC_G2_IO2	-	-	COMP2_OUT	SAI1_SD_B	TIM16_BKIN	EVENTOUT
	PB6	-	TSC_G2_IO3	-	-	TIM8_BKIN2_COMP2	SAI1_FS_B	TIM16_CH1N	EVENTOUT
	PB7	UART4_CTS	TSC_G2_IO4	-	-	FMC_NL	TIM8_BKIN_COMP1	TIM17_CH1N	EVENTOUT
	PB8	-	CAN1_RX	-	-	SDMMC1_D4	SAI1_MCLK_A	TIM16_CH1	EVENTOUT
	PB9	-	CAN1_TX	-	-	SDMMC1_D5	SAI1_FS_A	TIM17_CH1	EVENTOUT
	PB10	LPUART1_RX	-	QUADSPI_CLK	-	COMP1_OUT	SAI1_SCK_A	-	EVENTOUT
	PB11	LPUART1_TX	-	QUADSPI_NCS	-	COMP2_OUT	-	-	EVENTOUT
	PB12	LPUART1_RTS_DE	TSC_G1_IO1	-	-	SWPMI1_IO	SAI2_FS_A	TIM15_BKIN	EVENTOUT
	PB13	LPUART1_CTS	TSC_G1_IO2	-	-	SWPMI1_TX	SAI2_SCK_A	TIM15_CH1N	EVENTOUT
	PB14	-	TSC_G1_IO3	-	-	SWPMI1_RX	SAI2_MCLK_A	TIM15_CH1	EVENTOUT
	PB15	-	TSC_G1_IO4	-	-	SWPMI1_SUSPEND	SAI2_SD_A	TIM15_CH2	EVENTOUT

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 11: Current consumption measurement scheme*.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted with the minimum wait states number, depending on the f_{HCLK} frequency (refer to the table “Number of wait states according to CPU clock (HCLK) frequency” available in the RM0395 reference manual).
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$

The parameters given in *Table 26* to *Table 39* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 30. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART disable

Symbol	Parameter	Conditions			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2 f_{HCLK} = 26 MHz	Reduced code(1)	3.1	mA	119	µA/MHz
				Coremark	2.9		111	
				Dhrystone 2.1	2.8		111	
				Fibonacci	2.7		104	
				While(1)	2.6		100	
			Range 1 f_{HCLK} = 80 MHz	Reduced code(1)	10.0	mA	125	µA/MHz
				Coremark	9.4		117	
				Dhrystone 2.1	9.1		114	
				Fibonacci	9.0		112	
				While(1)	9.3		116	
I_{DD}(LPRun)	Supply current in Low-power run	$f_{HCLK} = f_{MSI}$ = 2 MHz all peripherals disable		Reduced code(1)	358	µA	179	µA/MHz
				Coremark	392		196	
				Dhrystone 2.1	390		195	
				Fibonacci	385		192	
				While(1)	385		192	

1. Reduced code used for characterization results provided in *Table 26*, *Table 27*, *Table 28*.

Table 31. Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1

Symbol	Parameter	Conditions			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2 f_{HCLK} = 26 MHz	Reduced code(1)	2.9	mA	111	µA/MHz
				Coremark	2.9		111	
				Dhrystone 2.1	2.9		111	
				Fibonacci	2.6		100	
				While(1)	2.6		100	
			Range 1 f_{HCLK} = 80 MHz	Reduced code(1)	10.2	mA	127	µA/MHz
				Coremark	10.4		130	
				Dhrystone 2.1	10.3		129	
				Fibonacci	9.6		120	
				While(1)	9.3		116	
I_{DD}(LPRun)	Supply current in Low-power run	$f_{HCLK} = f_{MSI}$ = 2 MHz all peripherals disable		Reduced code(1)	242	µA	121	µA/MHz
				Coremark	242		121	
				Dhrystone 2.1	242		121	
				Fibonacci	225		112	
				While(1)	242		121	

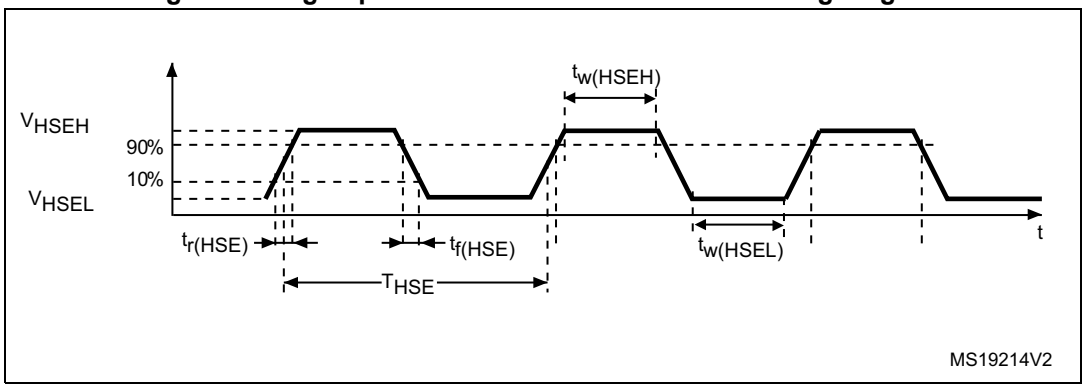
1. Reduced code used for characterization results provided in *Table 26*, *Table 27*, *Table 28*.

Table 38. Current consumption in Shutdown mode (continued)

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(Shutdown with RTC)	Supply current in Shutdown mode (backup registers retained) RTC enabled	RTC clocked by LSE bypassed at 32768 Hz	1.8 V	210	378	1299	3437	9357	-	-	-	-	-	nA
			2.4 V	303	499	1577	4056	10825	-	-	-	-	-	
			3 V	422	655	1925	4820	12569	-	-	-	-	-	
			3.6 V	584	888	2511	6158	15706	-	-	-	-	-	
		RTC clocked by LSE quartz (2) in low drive mode	1.8 V	329	499	1408	3460	-	-	-	-	-	-	
			2.4 V	431	634	1688	4064	-	-	-	-	-	-	
			3 V	554	791	2025	4795	-	-	-	-	-	-	
			3.6 V	729	1040	2619	6129	-	-	-	-	-	-	
I_{DD}(wakeup from Shutdown)	Supply current during wakeup from Shutdown mode	Wakeup clock is MSI = 4 MHz. See (3).	3 V	0.6	-	-	-	-	-	-	-	-	-	mA

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
3. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 41: Low-power mode wakeup timings*.

Figure 13. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 14*.

Table 45. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	-	250	-	-	ns

1. Guaranteed by design.

Figure 14. Low-speed external clock source AC timing diagram

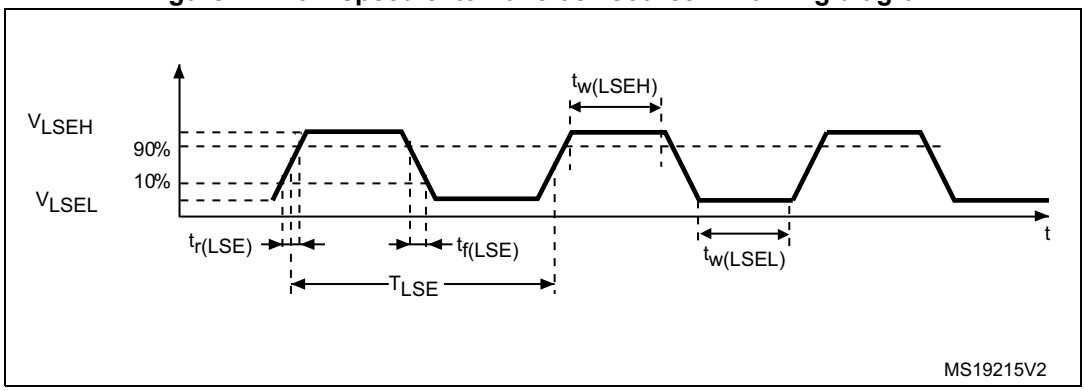
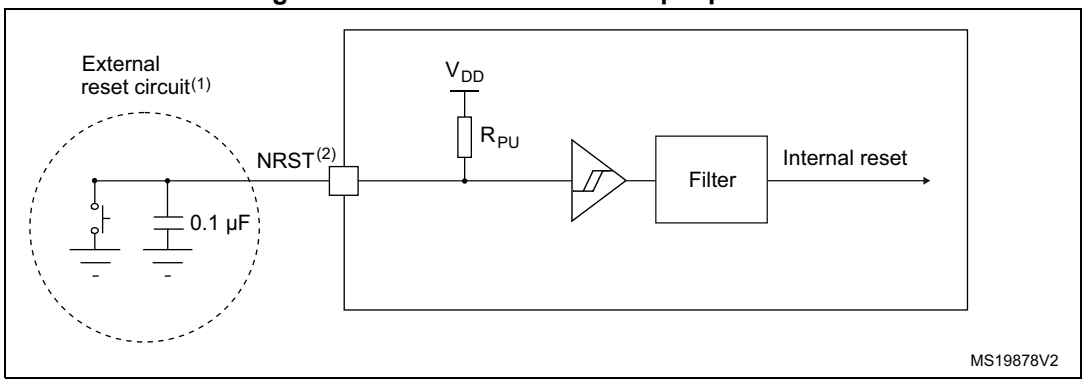


Figure 21. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 62: NRST pin characteristics*. Otherwise the reset will not be taken into account by the device.

6.3.16 Analog switches booster

Table 63. Analog switches booster characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	1.62	-	3.6	V
V_{BOOST}	Boost supply	2.7	-	4	
$t_{SU(BOOST)}$	Booster startup time	-	-	240	µs
$I_{DD(BOOST)}$	Booster consumption for 1.62 V ≤ V_{DD} ≤ 2.0 V	-	-	250	µA
	Booster consumption for 2.0 V ≤ V_{DD} ≤ 2.7 V	-	-	500	
	Booster consumption for 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	900	

1. Guaranteed by design.

Table 69. ADC accuracy - limited test conditions 4(1)(2)(3) (continued)

Symbol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 26 MHz, 1.65 V ≤ V_{DDA} = VREF+ ≤ 3.6 V, Voltage scaling Range 2	Single ended	Fast channel (max speed)	-	-71	-69	dB
				Slow channel (max speed)	-	-71	-69	
			Differential	Fast channel (max speed)	-	-73	-72	
				Slow channel (max speed)	-	-73	-72	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

6.3.20 Comparator characteristics

Table 73. COMP characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.62	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	V
V_{BG}(2)	Scaler input voltage	-		V_{REFINT}			V
V_{SC}	Scaler offset voltage	-		-	±5	±10	mV
I_{DDA}(SCALER)	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)		-	200	300	nA
		BRG_EN=1 (bridge enable)		-	0.8	1	µA
t_{START_SCALER}	Scaler startup time	-		-	100	200	µs
t_{START}	Comparator startup time to reach propagation delay specification	High-speed mode	$V_{DDA} \geq 2.7$ V	-	-	5	µs
			$V_{DDA} < 2.7$ V	-	-	7	
		Medium mode	$V_{DDA} \geq 2.7$ V	-	-	15	
			$V_{DDA} < 2.7$ V	-	-	25	
		Ultra-low-power mode		-	-	80	
t_D(3)	Propagation delay for 200 mV step with 100 mV overdrive	High-speed mode	$V_{DDA} \geq 2.7$ V	-	55	80	ns
			$V_{DDA} < 2.7$ V	-	65	100	
		Medium mode	$V_{DDA} \geq 2.7$ V	-	0.55	0.9	µs
			$V_{DDA} < 2.7$ V	-	0.65	1	
		Ultra-low-power mode		-	5	12	
V_{offset}	Comparator offset error	Full common mode range	-	-	±5	±20	mV
V_{hys}	Comparator hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		-	8	-	
		Medium hysteresis		-	15	-	
		High hysteresis		-	27	-	
I_{DDA}(COMP)	Comparator consumption from V_{DDA}	Ultra-low-power mode	Static	-	400	600	nA
			With 50 kHz ±100 mV overdrive square signal	-	1200	-	
		Medium mode	Static	-	5	7	µA
			With 50 kHz ±100 mV overdrive square signal	-	6	-	
		High-speed mode	Static	-	70	100	
			With 50 kHz ±100 mV overdrive square signal	-	75	-	

SAI characteristics

Unless otherwise specified, the parameters given in *Table 86* for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CK,SD,FS).

Table 86. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCLK}	SAI Main clock output	-	-	50	MHz
f_{CK}	SAI clock frequency(2)	Master transmitter $2.7 \le V_{DD} \le 3.6$ Voltage Range 1	-	18.5	MHz
		Master transmitter $1.71 \le V_{DD} \le 3.6$ Voltage Range 1	-	12.5	
		Master receiver Voltage Range 1	-	25	
		Slave transmitter $2.7 \le V_{DD} \le 3.6$ Voltage Range 1	-	22.5	
		Slave transmitter $1.71 \le V_{DD} \le 3.6$ Voltage Range 1	-	14.5	
		Slave receiver Voltage Range 1	-	25	
		Voltage Range 2	-	12.5	
$t_{v(FS)}$	FS valid time	Master mode $2.7 \le V_{DD} \le 3.6$	-	22	ns
		Master mode $1.71 \le V_{DD} \le 3.6$	-	40	
$t_{h(FS)}$	FS hold time	Master mode	10	-	ns
$t_{su(FS)}$	FS setup time	Slave mode	1	-	ns
$t_{h(FS)}$	FS hold time	Slave mode	2	-	ns
$t_{su(SD\_A\_MR)}$	Data input setup time	Master receiver	2.5	-	ns
$t_{su(SD\_B\_SR)}$		Slave receiver	3	-	
$t_{h(SD\_A\_MR)}$	Data input hold time	Master receiver	8	-	ns
$t_{h(SD\_B\_SR)}$		Slave receiver	4	-	

USB characteristics

The STM32L475xx USB interface is fully compliant with the USB specification version 2.0 and is USB-IF certified (for Full-speed device operation).

Table 89. USB electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDUSB}	USB transceiver operating voltage		3.0(1)	-	3.6	V
R_{PUI}	Embedded USB_DP pull-up value during idle		900	1250	1600	Ω
R_{PUR}	Embedded USB_DP pull-up value during reception		1400	2300	3200	
Z_{DRV}(2)	Output driver impedance(3)	Driving high and low	28	36	44	Ω

1. The STM32L475xx USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V voltage range.
2. Guaranteed by design.
3. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-); the matching impedance is already included in the embedded driver.

CAN (controller area network) interface

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).