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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 80MHz |
| Connectivity | CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, PWM, WDT |
| Number of I/O | 51 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 128K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | A/D 16x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l475ret6 |

# 2 Description

The STM32L475xx devices are the ultra-low-power microcontrollers based on the high-performance ARM® Cortex®-M4 32-bit RISC core operating at a frequency of up to 80 MHz. The Cortex-M4 core features a Floating point unit (FPU) single precision which supports all ARM single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32L475xx devices embed high-speed memories (Flash memory up to 1 Mbyte, up to 128 Kbyte of SRAM), a flexible external memory controller (FSMC) for static memories (for devices with 100 pins package), a Quad SPI flash memories interface (available on all packages) and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

The STM32L475xx devices embed several protection mechanisms for embedded Flash memory and SRAM: readout protection, write protection, proprietary code readout protection and Firewall.

The devices offer up to three fast 12-bit ADCs (5 Msps), two comparators, two operational amplifiers, two DAC channels, an internal voltage reference buffer, a low-power RTC, two general-purpose 32-bit timer, two 16-bit PWM timers dedicated to motor control, seven general-purpose 16-bit timers, and two 16-bit low-power timers. The devices support four digital filters for external sigma delta modulators (DFSDM).

In addition, up to 21 capacitive sensing channels are available.

They also feature standard and advanced communication interfaces.

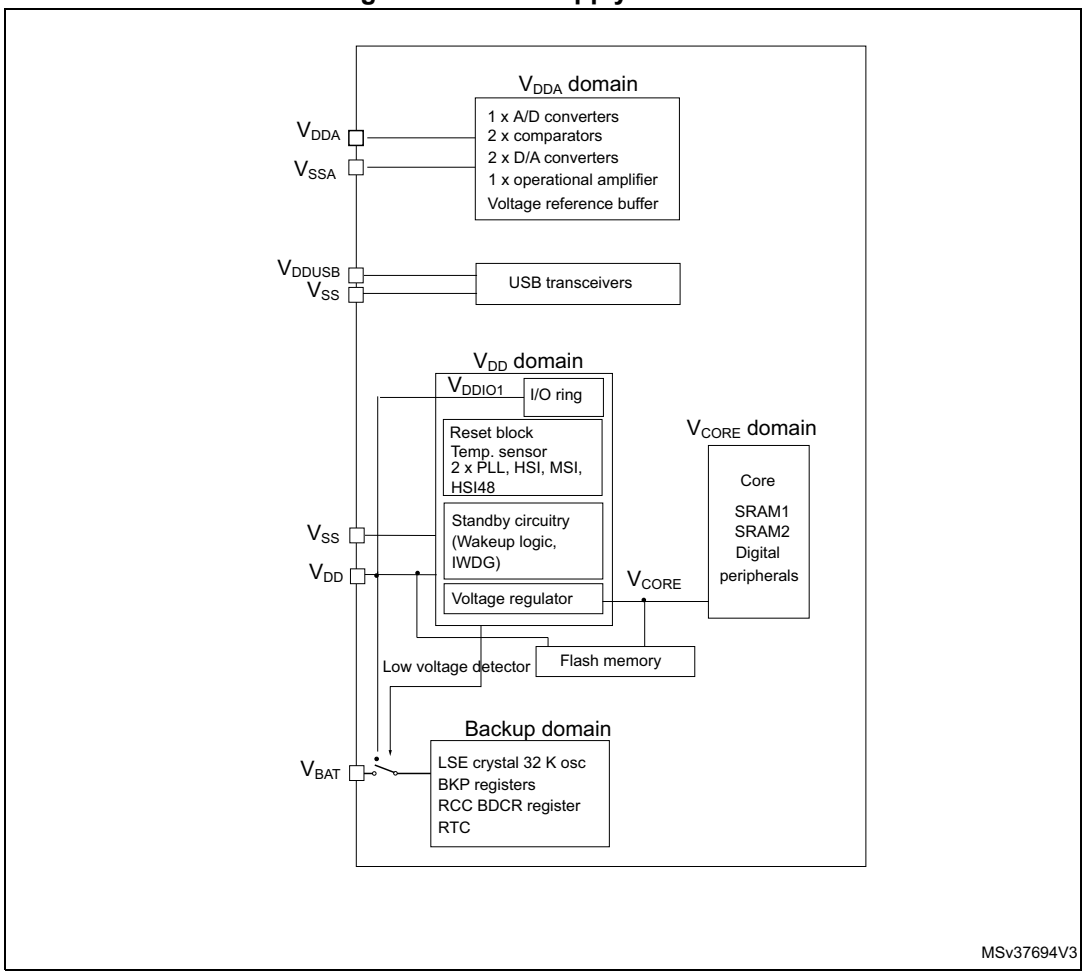
- Three I2Cs
- Three SPIs
- Three USARTs, two UARTs and one Low-Power UART.
- Two SAIs (Serial Audio Interfaces)
- One SDMMC
- One CAN
- One USB OTG full-speed
- One SWPMI (Single Wire Protocol Master Interface)

The STM32L475xx operates in the -40 to +85 °C (+105 °C junction), -40 to +105 °C (+125 °C junction) and -40 to +125 °C (+130 °C junction) temperature ranges from a 1.71 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

Some independent power supplies are supported: analog independent supply input for ADC, DAC, OPAMPs and comparators, 3.3 V dedicated supply input for USB and up to 14 I/Os can be supplied independently down to 1.08V. A VBAT input allows to backup the RTC and backup registers.

The STM32L475xx family offers two packages from 64-pin to 100-pin packages.

**Figure 2. Power supply overview**




## 3.9.2 Power supply supervisor

The device has an integrated ultra-low-power brown-out reset (BOR) active in all modes except Shutdown and ensuring proper operation after power-on and during power down. The device remains in reset mode when the monitored supply voltage $V_{DD}$ is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 1.71V at power on, and other higher thresholds can be selected through option bytes.The device features an embedded programmable voltage detector (PVD) that monitors the $V_{DD}$ power supply and compares it to the VPVD threshold. An interrupt can be generated when $V_{DD}$ drops below the VPVD threshold and/or when $V_{DD}$ is higher than the VPVD threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

In addition, the devices embeds a Peripheral Voltage Monitor which compares the independent supply voltages $V_{DDA}$, $V_{DDUSB}$ with a fixed threshold in order to ensure that the peripheral is in its functional supply range.

By default, the microcontroller is in Run mode after a system or a power Reset. It is up to the user to select one of the low-power modes described below:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Low-power run** mode

  This mode is achieved with VCORE supplied by the low-power regulator to minimize the regulator's operating current. The code can be executed from SRAM or from Flash, and the CPU frequency is limited to 2 MHz. The peripherals with independent clock can be clocked by HSI16.

- **Low-power sleep** mode

  This mode is entered from the low-power run mode. Only the CPU clock is stopped. When wakeup is triggered by an event or an interrupt, the system reverts to the low-power run mode.

- **Stop 0, Stop 1 and Stop 2** modes

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the VCORE domain are stopped, the PLL, the MSI RC, the HSI16 RC and the HSE crystal oscillators are disabled. The LSE or LSI is still running.

  The RTC can remain active (Stop mode with RTC, Stop mode without RTC).

  Some peripherals with wakeup capability can enable the HSI16 RC during Stop mode to detect their wakeup condition.

  Three Stop modes are available: Stop 0, Stop 1 and Stop 2 modes. In Stop 2 mode, most of the VCORE domain is put in a lower leakage mode.

  Stop 1 offers the largest number of active peripherals and wakeup sources, a smaller wakeup time but a higher consumption than Stop 2. In Stop 0 mode, the main regulator remains ON, allowing a very fast wakeup time but with much higher consumption.

  The system clock when exiting from Stop 0, Stop1 or Stop2 modes can be either MSI up to 48 MHz or HSI16, depending on software configuration.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption with BOR. The internal regulator is switched off so that the VCORE domain is powered off. The PLL, the MSI RC, the HSI16 RC and the HSE crystal oscillators are also switched off.

  The RTC can remain active (Standby mode with RTC, Standby mode without RTC).

  The brown-out reset (BOR) always remains active in Standby mode.

  The state of each I/O during standby mode can be selected by software: I/O with internal pull-up, internal pull-down or floating.

  After entering Standby mode, SRAM1 and register contents are lost except for registers in the Backup domain and Standby circuitry. Optionally, SRAM2 can be retained in

## 3.27 Low-power universal asynchronous receiver transmitter (LPUART)

The device embeds one Low-Power UART. The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART has a clock domain independent from the CPU clock, and can wakeup the system from Stop mode using baudrates up to 220 Kbaud. The wake up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

LPUART interface can be served by the DMA controller.

Table 15. STM32L475xx pin definitions (continued)

| Pin Number | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|
| LQFP64 | LQFP100 | | | | | Alternate functions | Additional functions |
| - | 4 | PE5 | I/O | FT | - | TRACED2, TIM3_CH3, DFSDM_CKIN3, TSC_G7_IO4, FMC_A21, SAI1_SCK_A, EVENTOUT | - |
| - | 5 | PE6 | I/O | FT | - | TRACED3, TIM3_CH4, FMC_A22, SAI1_SD_A, EVENTOUT | RTC_TAMP3/ WKUP3 |
| 1 | 6 | VBAT | S | - | - | - | - |
| 2 | 7 | PC13 | I/O | FT | (1) (2) | EVENTOUT | RTC_TAMP1/ RTC_TS/ RTC_OUT/ WKUP2 |
| 3 | 8 | PC14-OSC32_IN (PC14) | I/O | FT | (1) (2) | EVENTOUT | OSC32_IN |
| 4 | 9 | PC15-OSC32_OUT (PC15) | I/O | FT | (1) (2) | EVENTOUT | OSC32_OUT |
| - | 10 | VSS | S | - | - | - | - |
| - | 11 | VDD | S | - | - | - | - |
| 5 | 12 | PH0-OSC_IN (PH0) | I/O | FT | - | EVENTOUT | OSC_IN |
| 6 | 13 | PH1-OSC_OUT (PH1) | I/O | FT | - | EVENTOUT | OSC_OUT |
| 7 | 14 | NRST | I/O | RST | - | - | - |
| 8 | 15 | PC0 | I/O | FT_fa | - | LPTIM1_IN1, I2C3_SCL, DFSDM_DATIN4, LPUART1_RX, LPTIM2_IN1, EVENTOUT | ADC123_IN1 |
| 9 | 16 | PC1 | I/O | FT_fa | - | LPTIM1_OUT, I2C3_SDA, DFSDM_CKIN4, LPUART1_TX, EVENTOUT | ADC123_IN2 |
| 10 | 17 | PC2 | I/O | FT_a | - | LPTIM1_IN2, SPI2_MISO, DFSDM_CKOUT, EVENTOUT | ADC123_IN3 |
| 11 | 18 | PC3 | I/O | FT_a | - | LPTIM1_ETR, SPI2_MOSI, SAI1_SD_A, LPTIM2_ETR, EVENTOUT | ADC123_IN4 |
| - | 19 | VSSA | S | - | - | - | - |
| - | 20 | VREF- | S | - | - | - | - |

Table 15. STM32L475xx pin definitions (continued)

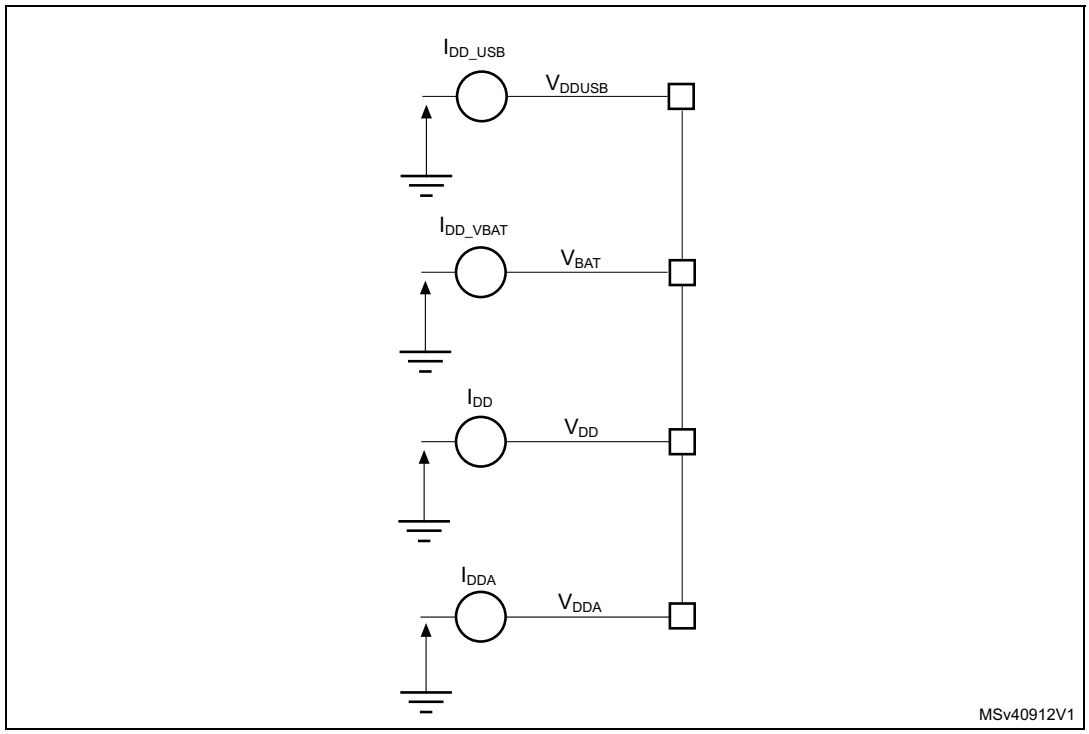
| Pin Number | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|
| LQFP64 | LQFP100 | | | | | Alternate functions | Additional functions |
| 35 | 53 | PB14 | I/O | FT_f | - | TIM1_CH2N, TIM8_CH2N, I2C2_SDA, SPI2_MISO, DFSDM_DATIN2, USART3_RTS_DE, TSC_G1_IO3, SWPMI1_RX, SAI2_MCLK_A, TIM15_CH1, EVENTOUT | - |
| 36 | 54 | PB15 | I/O | FT | - | RTC_REFIN, TIM1_CH3N, TIM8_CH3N, SPI2_MOSI, DFSDM_CKIN2, TSC_G1_IO4, SWPMI1_SUSPEND, SAI2_SD_A, TIM15_CH2, EVENTOUT | - |
| - | 55 | PD8 | I/O | FT | - | USART3_TX, FMC_D13, EVENTOUT | - |
| - | 56 | PD9 | I/O | FT | - | USART3_RX, FMC_D14, SAI2_MCLK_A, EVENTOUT | - |
| - | 57 | PD10 | I/O | FT | - | USART3_CK, TSC_G6_IO1, FMC_D15, SAI2_SCK_A, EVENTOUT | - |
| - | 58 | PD11 | I/O | FT | - | USART3_CTS, TSC_G6_IO2, FMC_A16, SAI2_SD_A, LPTIM2_ETR, EVENTOUT | - |
| - | 59 | PD12 | I/O | FT | - | TIM4_CH1, USART3_RTS_DE, TSC_G6_IO3, FMC_A17, SAI2_FS_A, LPTIM2_IN1, EVENTOUT | - |
| - | 60 | PD13 | I/O | FT | - | TIM4_CH2, TSC_G6_IO4, FMC_A18, LPTIM2_OUT, EVENTOUT | - |
| - | 61 | PD14 | I/O | FT | - | TIM4_CH3, FMC_D0, EVENTOUT | - |
| - | 62 | PD15 | I/O | FT | - | TIM4_CH4, FMC_D1, EVENTOUT | - |
| 37 | 63 | PC6 | I/O | FT | - | TIM3_CH1, TIM8_CH1, DFSDM_CKIN3, TSC_G4_IO1, SDMMC1_D6, SAI2_MCLK_A, EVENTOUT | - |

Table 15. STM32L475xx pin definitions (continued)

| Pin Number | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|
| LQFP64 | LQFP100 | | | | | Alternate functions | Additional functions |
| 38 | 64 | PC7 | I/O | FT | - | TIM3_CH2, TIM8_CH2, DFSDM_DATIN3, TSC_G4_IO2, SDMMC1_D7, SAI2_MCLK_B, EVENTOUT | - |
| 39 | 65 | PC8 | I/O | FT | - | TIM3_CH3, TIM8_CH3, TSC_G4_IO3, SDMMC1_D0, EVENTOUT | - |
| 40 | 66 | PC9 | I/O | FT | - | TIM8_BKIN2, TIM3_CH4, TIM8_CH4, TSC_G4_IO4, OTG_FS_NOE, SDMMC1_D1, SAI2_EXTCLK, TIM8_BKIN2_COMP1, EVENTOUT | - |
| 41 | 67 | PA8 | I/O | FT | - | MCO, TIM1_CH1, USART1_CK, OTG_FS_SOF, LPTIM2_OUT, EVENTOUT | - |
| 42 | 68 | PA9 | I/O | FT_u | - | TIM1_CH2, USART1_TX, TIM15_BKIN, EVENTOUT | OTG_FS_VBUS |
| 43 | 69 | PA10 | I/O | FT_u | - | TIM1_CH3, USART1_RX, OTG_FS_ID, TIM17_BKIN, EVENTOUT | - |
| 44 | 70 | PA11 | I/O | FT_u | - | TIM1_CH4, TIM1_BKIN2, USART1_CTS, CAN1_RX, OTG_FS_DM, TIM1_BKIN2_COMP1, EVENTOUT | - |
| 45 | 71 | PA12 | I/O | FT_u | - | TIM1_ETR, USART1_RTS_DE, CAN1_TX, OTG_FS_DP, EVENTOUT | - |
| 46 | 72 | PA13 (JTMS-SWDIO) | I/O | FT | (3) | JTMS-SWDIO, IR_OUT, OTG_FS_NOE, EVENTOUT | - |
| 47 | - | VSS | S | - | - | - | - |
| 48 | 73 | VDDUSB | S | - | - | - | - |
| - | 74 | VSS | S | - | - | - | - |
| - | 75 | VDD | S | - | - | - | - |
| 49 | 76 | PA14 (JTCK-SWCLK) | I/O | FT | (3) | JTCK-SWCLK, EVENTOUT | - |

### 6.1.7 Current consumption measurement

**Figure 11. Current consumption measurement scheme**




## 6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 19: Voltage characteristics*, *Table 20: Current characteristics* and *Table 21: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 19. Voltage characteristics(1)**

| Symbol | Ratings | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DDX}$ - $V_{SS}$ | External main supply voltage (including $V_{DD}$, $V_{DDA}$, $V_{DDUSB}$, $V_{BAT}$) | -0.3 | 4.0 | V |
| $V_{IN}$(2) | Input voltage on FT_xxx pins | $V_{SS}$-0.3 | min ($V_{DD}$, $V_{DDA}$, $V_{DDUSB}$) + 4.0(3)(4) | V |
| | Input voltage on TT_xx pins | $V_{SS}$-0.3 | 4.0 | |
| | Input voltage on BOOT0 pin | $V_{SS}$ | 9.0 | |
| | Input voltage on any other pins | $V_{SS}$-0.3 | 4.0 | |
| $\|\Delta V_{DDx}\|$ | Variations between different $V_{DDX}$ power pins of the same domain | - | 50 | mV |
| $\|V_{SSx}-V_{SS}\|$ | Variations between all the different ground pins(5) | - | 50 | mV |

**Figure 12. $V_{REFINT}$ versus temperature**

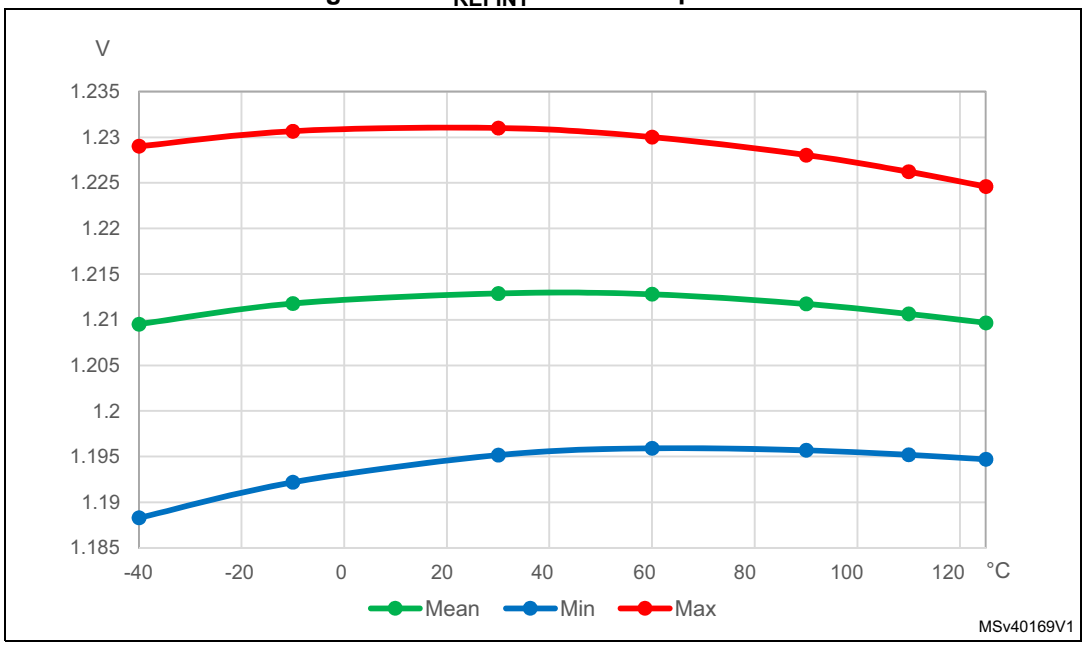


**Table 35. Current consumption in Stop 1 mode**

| Symbol | Parameter | Conditions | | TYP | | | | | MAX(1) | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | - | $V_{DD}$ | 25 °C | 55 °C | 85 °C | 105 °C | 125 °C | 25 °C | 55 °C | 85 °C | 105 °C | 125 °C | |
| $I_{DD}$ (Stop 1) | Supply current in Stop 1 mode, RTC disabled | - | 1.8 V | 6.59 | 24.7 | 92.7 | 208 | 437 | 16 | 62 | 232 | 520 | 1093 | µA |
| | | | 2.4 V | 6.65 | 24.8 | 92.9 | 209 | 439 | 17 | 62 | 232 | 523 | 1098 | |
| | | | 3 V | 6.65 | 24.9 | 93.3 | 210 | 442 | 17 | 62 | 233 | 525 | 1105 | |
| | | | 3.6 V | 6.70 | 25.1 | 93.8 | 212 | 447 | 17 | 63 | 235 | 530 | 1118 | |
| $I_{DD}$ (Stop 1 with RTC) | Supply current in stop 1 mode, RTC enabled | RTC clocked by LSI | 1.8 V | 6.88 | 25.0 | 93.1 | 209 | 439 | 17 | 63 | 233 | 523 | 1098 | µA |
| | | | 2.4 V | 7.02 | 25.2 | 93.7 | 210 | 441 | 18 | 63 | 234 | 525 | 1103 | |
| | | | 3 V | 7.12 | 25.4 | 94.2 | 212 | 444 | 18 | 64 | 236 | 530 | 1110 | |
| | | | 3.6 V | 7.25 | 25.7 | 95.2 | 214 | 449 | 18 | 64 | 238 | 535 | 1123 | |
| | | RTC clocked by LSE bypassed, at 32768 Hz | 1.8 V | 6.91 | 25.2 | 93.4 | 210 | 440 | 17 | 63 | 234 | 525 | 1100 | |
| | | | 2.4 V | 7.04 | 25.3 | 94.2 | 211 | 443 | 18 | 63 | 236 | 528 | 1108 | |
| | | | 3 V | 7.19 | 25.7 | 95.0 | 212 | 446 | 18 | 64 | 238 | 530 | 1115 | |
| | | | 3.6 V | 7.97 | 26.0 | 96.1 | 215 | 451 | 20 | 65 | 240 | 538 | 1128 | |
| | | RTC clocked by LSE quartz(2) in low drive mode | 1.8 V | 6.85 | 25.0 | 93.0 | 208.3 | - | 17 | 63 | 233 | 521 | - | |
| | | | 2.4 V | 6.94 | 25.1 | 93.2 | 209.3 | - | 17 | 63 | 233 | 523 | - | |
| | | | 3 V | 7.10 | 25.2 | 93.6 | 210.3 | - | 18 | 63 | 234 | 526 | - | |
| | | | 3.6 V | 7.34 | 25.4 | 94.1 | 212.3 | - | 18 | 64 | 235 | 531 | - | |
| $I_{DD}$ (wakeup from Stop1) | Supply current during wakeup from Stop 1 | Wakeup clock MSI = 48 MHz, voltage Range 1, See (3). | 3 V | 1.47 | - | - | - | - | - | | | | | mA |
| | | Wakeup clock MSI = 4 MHz, voltage Range 2, See (3). | 3 V | 1.7 | - | - | - | - | | | | | | |
| | | Wakeup clock HSI16 = 16 MHz, voltage Range 1, See (3). | 3 V | 1.62 | - | - | - | - | | | | | | |

1. Guaranteed based on test during characterization, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
3. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 41: Low-power mode wakeup timings*.

**Table 37. Current consumption in Standby mode**

| Symbol | Parameter | Conditions | | TYP | | | | | MAX(1) | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | - | $V_{DD}$ | 25 °C | 55 °C | 85 °C | 105 °C | 125 °C | 25 °C | 55 °C | 85 °C | 105 °C | 125 °C | |
| $I_{DD}$(Standby) | Supply current in Standby mode (backup registers retained), RTC disabled | no independent watchdog | 1.8 V | 114 | 355 | 1540 | 4146 | 10735 | 176 | 888 | 3850 | 10365 | 26838 | nA |
| | | | 2.4 V | 138 | 407 | 1795 | 4828 | 12451 | 223 | 1018 | 4488 | 12070 | 31128 | |
| | | | 3 V | 150 | 486 | 2074 | 5589 | 14291 | 263 | 1215 | 5185 | 13973 | 35728 | |
| | | | 3.6 V | 198 | 618 | 2608 | 6928 | 17499 | 383 | 1545 | 6520 | 17320 (2) | 43748 | |
| | | with independent watchdog | 1.8 V | 317 | - | - | - | - | - | - | - | - | - | |
| | | | 2.4 V | 391 | - | - | - | - | - | - | - | - | - | |
| | | | 3 V | 438 | - | - | - | - | - | - | - | - | - | |
| | | | 3.6 V | 566 | - | - | - | - | - | - | - | - | - | |
| $I_{DD}$(Standby with RTC) | Supply current in Standby mode (backup registers retained), RTC enabled | RTC clocked by LSI, no independent watchdog | 1.8 V | 377 | 621 | 1873 | 4564 | 11318 | 491 | 1207 | 4250 | 10867 | 27537 | nA |
| | | | 2.4 V | 464 | 756 | 2210 | 5348 | 13166 | 614 | 1436 | 4986 | 12694 | 31986 | |
| | | | 3 V | 572 | 913 | 2599 | 6219 | 15197 | 770 | 1727 | 5815 | 14729 | 36815 | |
| | | | 3.6 V | 722 | 1144 | 3253 | 7724 | 18696 | 1012 | 2176 | 7294 | 18275 | 45184 | |
| | | RTC clocked by LSI, with independent watchdog | 1.8 V | 456 | - | - | - | - | - | - | - | - | - | |
| | | | 2.4 V | 557 | - | - | - | - | - | - | - | - | - | |
| | | | 3 V | 663 | - | - | - | - | - | - | - | - | - | |
| | | | 3.6 V | 885 | - | - | - | - | - | - | - | - | - | |
| | | RTC clocked by LSE bypassed at 32768Hz | 1.8 V | 289 | 527 | 1747 | 4402 | 11009 | - | - | - | - | - | nA |
| | | | 2.4 V | 396 | 671 | 2108 | 5202 | 12869 | - | - | - | - | - | |
| | | | 3 V | 528 | 853 | 2531 | 6095 | 14915 | - | - | - | - | - | |
| | | | 3.6 V | 710 | 1111 | 3115 | 7470 | 18221 | - | - | - | - | - | |
| | | RTC clocked by LSE quartz (3) in low drive mode | 1.8 V | 416 | 640 | 1862 | 4479 | 11908 | - | - | - | - | - | |
| | | | 2.4 V | 514 | 796 | 2193 | 5236 | 13689 | - | - | - | - | - | |
| | | | 3 V | 652 | 961 | 2589 | 6103 | 15598 | - | - | - | - | - | |
| | | | 3.6 V | 821 | 1226 | 3235 | 7551 | 17947 | - | - | - | - | - | |

**Table 41. Low-power mode wakeup timings(1) (continued)**

| Symbol | Parameter | Conditions | | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{WUSTOP1}$ | Wake up time from Stop 1 mode to Run mode in Flash | Range 1 | Wakeup clock MSI = 48 MHz | 6.2 | 10.2 | µs |
| | | | Wakeup clock HSI16 = 16 MHz | 6.3 | 8.99 | |
| | | Range 2 | Wakeup clock MSI = 24 MHz | 6.3 | 10.46 | |
| | | | Wakeup clock HSI16 = 16 MHz | 6.3 | 8.87 | |
| | | | Wakeup clock MSI = 4 MHz | 8.0 | 13.23 | |
| | Wake up time from Stop 1 mode to Run mode in SRAM1 | Range 1 | Wakeup clock MSI = 48 MHz | 4.5 | 5.78 | |
| | | | Wakeup clock HSI16 = 16 MHz | 5.5 | 7.1 | |
| | | Range 2 | Wakeup clock MSI = 24 MHz | 5.0 | 6.5 | |
| | | | Wakeup clock HSI16 = 16 MHz | 5.5 | 7.1 | |
| | | | Wakeup clock MSI = 4 MHz | 8.2 | 13.5 | |
| | Wake up time from Stop 1 mode to Low-power run mode in Flash | Regulator in low-power mode (LPR=1 in PWR_CR1) | Wakeup clock MSI = 2 MHz | 12.7 | 20 | |
| | Wake up time from Stop 1 mode to Low-power run mode in SRAM1 | | | 10.7 | 21.5 | |
| $t_{WUSTOP2}$ | Wake up time from Stop 2 mode to Run mode in Flash | Range 1 | Wakeup clock MSI = 48 MHz | 8.0 | 9.4 | µs |
| | | | Wakeup clock HSI16 = 16 MHz | 7.3 | 9.3 | |
| | | Range 2 | Wakeup clock MSI = 24 MHz | 8.2 | 9.9 | |
| | | | Wakeup clock HSI16 = 16 MHz | 7.3 | 9.3 | |
| | | | Wakeup clock MSI = 4 MHz | 10.6 | 15.8 | |
| | Wake up time from Stop 2 mode to Run mode in SRAM1 | Range 1 | Wakeup clock MSI = 48 MHz | 5.1 | 6.7 | |
| | | | Wakeup clock HSI16 = 16 MHz | 5.7 | 8 | |
| | | Range 2 | Wakeup clock MSI = 24 MHz | 5.5 | 6.65 | |
| | | | Wakeup clock HSI16 = 16 MHz | 5.7 | 7.53 | |
| | | | Wakeup clock MSI = 4 MHz | 8.2 | 16.6 | |
| $t_{WUSTBY}$ | Wakeup time from Standby mode to Run mode | Range 1 | Wakeup clock MSI = 8 MHz | 14.3 | 20.8 | µs |
| | | | Wakeup clock MSI = 4 MHz | 20.1 | 35.5 | |
| $t_{WUSTBY\ SRAM2}$ | Wakeup time from Standby with SRAM2 to Run mode | Range 1 | Wakeup clock MSI = 8 MHz | 14.3 | 24.3 | µs |
| | | | Wakeup clock MSI = 4 MHz | 20.1 | 38.5 | |
| $t_{WUSHDN}$ | Wakeup time from Shutdown mode to Run mode | Range 1 | Wakeup clock MSI = 4 MHz | 256 | 330.6 | µs |

1. Guaranteed by characterization results.

### High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 46*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 46. HSE oscillator characteristics(1)**

| Symbol | Parameter | Conditions(2) | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{OSC\_IN}$ | Oscillator frequency | - | 4 | 8 | 48 | MHz |
| $R_F$ | Feedback resistor | - | - | 200 | - | kΩ |
| $I_{DD(HSE)}$ | HSE current consumption | During startup(3) | - | - | 5.5 | mA |
| | | $V_{DD}$ = 3 V, Rm = 30 Ω, CL = 10 pF@8 MHz | - | 0.44 | - | |
| | | $V_{DD}$ = 3 V, Rm = 45 Ω, CL = 10 pF@8 MHz | - | 0.45 | - | |
| | | $V_{DD}$ = 3 V, Rm = 30 Ω, CL = 5 pF@48 MHz | - | 0.68 | - | |
| | | $V_{DD}$ = 3 V, Rm = 30 Ω, CL = 10 pF@48 MHz | - | 0.94 | - | |
| | | $V_{DD}$ = 3 V, Rm = 30 Ω, CL = 20 pF@48 MHz | - | 1.77 | - | |
| $G_m$ | Maximum critical crystal transconductance | Startup | - | - | 1.5 | mA/V |
| $t_{SU(HSE)}$(4) | Startup time | $V_{DD}$ is stabilized | - | 2 | - | ms |

1. Guaranteed by design.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For $C_{L1}$ and $C_{L2}$, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 15*). $C_{L1}$ and $C_{L2}$ are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of $C_{L1}$ and $C_{L2}$. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing $C_{L1}$ and $C_{L2}$.

**Figure 17. HSI16 frequency versus temperature**

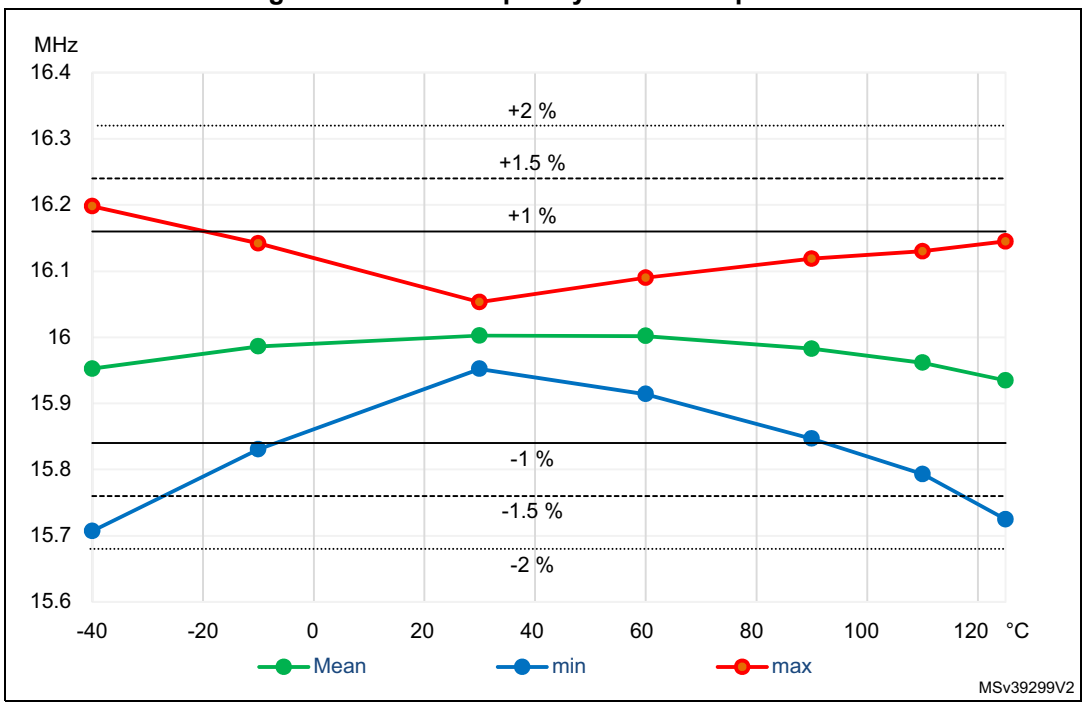


**Table 59. I/O static characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{lkg}$ | FT_xx input leakage current(3) | $V_{IN} \le Max(V_{DDXXX})$(4) | - | - | ±100 | nA |
| | | $Max(V_{DDXXX}) \le V_{IN} \le Max(V_{DDXXX})+1$ V(4)(5) | - | - | 650(3)(6) | |
| | | $Max(V_{DDXXX})+1$ V < VIN ≤ 5.5 V(3)(5) | - | - | 200(6) | |
| | FT_lu, FT_u and PC3 IO | $V_{IN} \le Max(V_{DDXXX})$ (4) | - | - | ±150 | |
| | | $Max(V_{DDXXX}) \le V_{IN} \le Max(V_{DDXXX})+1$ V(4) | - | - | 2500(3)(7) | |
| | | $Max(V_{DDXXX})+1$ V < VIN ≤ 5.5 V(4)(5)(7) | - | - | 250(7) | |
| | TT_xx input leakage current | $V_{IN} \le Max(V_{DDXXX})$(6) | - | - | ±150 | |
| | | $Max(V_{DDXXX}) \le V_{IN}$ < 3.6 V(6) | - | - | 2000(3) | |
| $R_{PU}$ | Weak pull-up equivalent resistor (8) | $V_{IN} = V_{SS}$ | 25 | 40 | 55 | kΩ |
| $R_{PD}$ | Weak pull-down equivalent resistor(8) | $V_{IN} = V_{DDIOx}$ | 25 | 40 | 55 | kΩ |
| $C_{IO}$ | I/O pin capacitance | - | - | 5 | - | pF |

1. Refer to *Figure 19: I/O input characteristics*.
2. Tested in production.
3. Guaranteed by design.
4. $Max(V_{DDXXX})$ is the maximum value of all the I/O supplies. Refer to *Table: Legend/Abbreviations used in the pinout table.*
5. All TX_xx IO except FT_lu, FT_u and PC3.
6. This value represents the pad leakage of the IO itself. The total product pad leakage is provided by this formula: $I_{Total\_Ileak\_max}$ = 10 µA + [number of IOs where $V_{IN}$ is applied on the pad] x $I_{lkg}$(Max).
7. To sustain a voltage higher than MIN($V_{DD}$, $V_{DDA}$, $V_{DDUSB}$) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
8. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

**Table 70. DAC characteristics(1) (continued)**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{SAMP}$ | Sampling time in sample and hold mode (code transition between the lowest input code and the highest input code when DACOUT reaches final value ±1LSB) | DAC_OUT pin connected | DAC output buffer ON, $C_{SH}$ = 100 nF | - | 0.7 | 3.5 | ms |
| | | | DAC output buffer OFF, $C_{SH}$ = 100 nF | - | 10.5 | 18 | |
| | | DAC_OUT pin not connected (internal connection only) | DAC output buffer OFF | - | 2 | 3.5 | µs |
| $I_{leak}$ | Output leakage current | Sample and hold mode, DAC_OUT pin connected | | - | - | -(3) | nA |
| $CI_{int}$ | Internal sample and hold capacitor | - | | 5.2 | 7 | 8.8 | pF |
| $t_{TRIM}$ | Middle code offset trim time | DAC output buffer ON | | 50 | - | - | µs |
| $V_{offset}$ | Middle code offset for 1 trim code step | $V_{REF+}$ = 3.6 V | | - | 1500 | - | µV |
| | | $V_{REF+}$ = 1.8 V | | - | 750 | - | |
| $I_{DDA}$(DAC) | DAC consumption from $V_{DDA}$ | DAC output buffer ON | No load, middle code (0x800) | - | 315 | 500 | µA |
| | | | No load, worst code (0xF1C) | - | 450 | 670 | |
| | | DAC output buffer OFF | No load, middle code (0x800) | - | - | 0.2 | |
| | | Sample and hold mode, $C_{SH}$ = 100 nF | | - | 315 x Ton/(Ton +Toff) (4) | 670 x Ton/(Ton +Toff) (4) | |
| $I_{DDV}$(DAC) | DAC consumption from $V_{REF+}$ | DAC output buffer ON | No load, middle code (0x800) | - | 185 | 240 | µA |
| | | | No load, worst code (0xF1C) | - | 340 | 400 | |
| | | DAC output buffer OFF | No load, middle code (0x800) | - | 155 | 205 | |
| | | Sample and hold mode, buffer ON, $C_{SH}$ = 100 nF, worst case | | - | 185 x Ton/(Ton +Toff) (4) | 400 x Ton/(Ton +Toff) (4) | |
| | | Sample and hold mode, buffer OFF, $C_{SH}$ = 100 nF, worst case | | - | 155 x Ton/(Ton +Toff) (4) | 205 x Ton/(Ton +Toff) (4) | |

1. Guaranteed by design.
2. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).

**Table 74. OPAMP characteristics(1) (continued)**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{network}$ | R2/R1 internal resistance values in PGA mode(5) | PGA Gain = 2 | | - | 80/80 | - | kΩ/kΩ |
| | | PGA Gain = 4 | | - | 120/ 40 | - | |
| | | PGA Gain = 8 | | - | 140/ 20 | - | |
| | | PGA Gain = 16 | | - | 150/ 10 | - | |
| Delta R | Resistance variation (R1 or R2) | - | | -15 | - | 15 | % |
| PGA gain error | PGA gain error | - | | -1 | - | 1 | % |
| PGA BW | PGA bandwidth for different non inverting gain | Gain = 2 | - | - | GBW/ 2 | - | MHz |
| | | Gain = 4 | - | - | GBW/ 4 | - | |
| | | Gain = 8 | - | - | GBW/ 8 | - | |
| | | Gain = 16 | - | - | GBW/ 16 | - | |
| en | Voltage noise density | Normal mode | at 1 kHz, Output loaded with 4 kΩ | - | 500 | - | nV/√Hz |
| | | Low-power mode | at 1 kHz, Output loaded with 20 kΩ | - | 600 | - | |
| | | Normal mode | at 10 kHz, Output loaded with 4 kΩ | - | 180 | - | |
| | | Low-power mode | at 10 kHz, Output loaded with 20 kΩ | - | 290 | - | |
| $I_{DDA}(OPAMP)$(3) | OPAMP consumption from $V_{DDA}$ | Normal mode | no Load, quiescent mode | - | 120 | 260 | µA |
| | | Low-power mode | | - | 45 | 100 | |

1. Guaranteed by design, unless otherwise specified.
2. The temperature range is limited to 0 °C-125 °C when $V_{DDA}$ is below 2 V
3. Guaranteed by characterization results.
4. Mostly I/O leakage, when used in analog mode. Refer to $I_{lkg}$ parameter in *Table 59: I/O static characteristics*.
5. R2 is the internal resistance between OPAMP output and OPAMP inverting input. R1 is the internal resistance between OPAMP inverting input and ground. The PGA gain =1+R2/R1

### SAI characteristics

Unless otherwise specified, the parameters given in *Table 86* for SAI are derived from tests performed under the ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x $V_{DD}$

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CK,SD,FS).

**Table 86. SAI characteristics(1)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{MCLK}$ | SAI Main clock output | - | - | 50 | MHz |
| $f_{CK}$ | SAI clock frequency(2) | Master transmitter<br>$2.7 \le V_{DD} \le 3.6$<br>Voltage Range 1 | - | 18.5 | MHz |
| | | Master transmitter<br>$1.71 \le V_{DD} \le 3.6$<br>Voltage Range 1 | - | 12.5 | |
| | | Master receiver<br>Voltage Range 1 | - | 25 | |
| | | Slave transmitter<br>$2.7 \le V_{DD} \le 3.6$<br>Voltage Range 1 | - | 22.5 | |
| | | Slave transmitter<br>$1.71 \le V_{DD} \le 3.6$<br>Voltage Range 1 | - | 14.5 | |
| | | Slave receiver<br>Voltage Range 1 | - | 25 | |
| | | Voltage Range 2 | - | 12.5 | |
| $t_{v(FS)}$ | FS valid time | Master mode<br>$2.7 \le V_{DD} \le 3.6$ | - | 22 | ns |
| | | Master mode<br>$1.71 \le V_{DD} \le 3.6$ | - | 40 | |
| $t_{h(FS)}$ | FS hold time | Master mode | 10 | - | ns |
| $t_{su(FS)}$ | FS setup time | Slave mode | 1 | - | ns |
| $t_{h(FS)}$ | FS hold time | Slave mode | 2 | - | ns |
| $t_{su(SD\_A\_MR)}$ | Data input setup time | Master receiver | 2.5 | - | ns |
| $t_{su(SD\_B\_SR)}$ | | Slave receiver | 3 | - | |
| $t_{h(SD\_A\_MR)}$ | Data input hold time | Master receiver | 8 | - | ns |
| $t_{h(SD\_B\_SR)}$ | | Slave receiver | 4 | - | |

## 6.3.27 FSMC characteristics

Unless otherwise specified, the parameters given in *Table 90* to *Table 95* for the FMC interface are derived from tests performed under the ambient temperature, $f_{HCLK}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 22*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output characteristics.

### Asynchronous waveforms and timings

*Figure 34* and *Figure 35* represent asynchronous waveforms and *Table 90* through *Table 93* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0

In all timing tables, the THCLK is the HCLK clock period.