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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 80MHz |
| Connectivity | CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, PWM, WDT |
| Number of I/O | 82 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 128K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | A/D 16x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l475vet6 |

**Table 4. STM32L475 modes overview (continued)**

| Mode | Regulator (1) | CPU | Flash | SRAM | Clocks | DMA & Peripherals(2) | Wakeup source | Consumption(3) | Wakeup time |
|---|---|---|---|---|---|---|---|---|---|
| Standby | LPR | Powered Off | Off | SRAM2 ON | LSE LSI | BOR, RTC, IWDG<br>***<br>All other peripherals are powered off.<br>***<br>I/O configuration can be floating, pull-up or pull-down | Reset pin<br>5 I/Os (WKUPx)(10)<br>BOR, RTC, IWDG | 0.35 µA w/o RTC<br>0.65 µA w/ RTC | 14 µs |
| | OFF | | | Powered Off | | | | 0.12 µA w/o RTC<br>0.42 µA w/ RTC | |
| Shutdown | OFF | Powered Off | Off | Powered Off | LSE | RTC<br>***<br>All other peripherals are powered off.<br>***<br>I/O configuration can be floating, pull-up or pull-down(11) | Reset pin<br>5 I/Os (WKUPx)(10)<br>RTC | 0.03 µA w/o RTC<br>0.33 µA w/ RTC | 256 µs |

1. LPR means Main regulator is OFF and Low-power regulator is ON.
2. All peripherals can be active or clock gated to save power consumption.
3. Typical current at $V_{DD}$ = 1.8 V, 25°C. Consumptions values provided running from SRAM, Flash memory Off, 80 MHz in Range 1, 26 MHz in Range 2, 2 MHz in LPRun/LPSleep.
4. The Flash memory can be put in power-down and its clock can be gated off when executing from SRAM.
5. The SRAM1 and SRAM2 clocks can be gated on or off independently.
6. U(S)ART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
7. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
8. OTG_FS wakeup by resume from suspend and attach detection protocol event.
9. SWPMI1 wakeup by resume from suspend.
10. The I/Os with wakeup from Standby/Shutdown capability are: PA0, PC13, PE6, PA2, PC5.
11. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

Standby mode, supplied by the low-power Regulator (Standby with RAM2 retention mode).

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper) or a failure is detected on LSE (CSS on LSE).

The system clock after wakeup is MSI up to 8 MHz.

- **Shutdown** mode

  The Shutdown mode allows to achieve the lowest power consumption. The internal regulator is switched off so that the VCORE domain is powered off. The PLL, the HSI16, the MSI, the LSI and the HSE oscillators are also switched off.

  The RTC can remain active (Shutdown mode with RTC, Shutdown mode without RTC).

  The BOR is not available in Shutdown mode. No power voltage monitoring is possible in this mode, therefore the switch to Backup domain is not supported.

  SRAM1, SRAM2 and register contents are lost except for registers in the Backup domain.

  The device exits Shutdown mode when an external reset (NRST pin), a WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper).

  The system clock after wakeup is MSI at 4 MHz.

## 3.11 Clocks and startup

The clock controller (see *Figure 3*) distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source:** four different clock sources can be used to drive the master clock SYSCLK:
  - 4-48 MHz high-speed external crystal or ceramic resonator (HSE), that can supply a PLL. The HSE can also be configured in bypass mode for an external clock.
  - 16 MHz high-speed internal RC oscillator (HSI16), trimmable by software, that can supply a PLL
  - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 12 frequencies from 100 kHz to 48 MHz. When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be automatically trimmed by hardware to reach better than ±0.25% accuracy. In this mode the MSI can feed the USB device, saving the need of an external high-speed crystal (HSE). The MSI can supply a PLL.
  - System PLL which can be fed by HSE, HSI16 or MSI, with a maximum frequency at 80 MHz.
- **Auxiliary clock source:** two ultralow-power clock sources that can be used to drive the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for an external clock.
  - 32 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock accuracy is ±5% accuracy.
- **Peripheral clock sources:** Several peripherals (USB, SDMMC, RNG, SAI, USARTs, I2Cs, LPTimers, ADC, SWPMI) have their own independent clock whatever the system clock. Three PLLs, each having three independent outputs allowing the highest flexibility, can generate independent clocks for the ADC, the USB/SDMMC/RNG and the two SAIs.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 4 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI16 and a software

### 3.23.3 Basic timers (TIM6 and TIM7)

The basic timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit timebases.

### 3.23.4 Low-power timer (LPTIM1 and LPTIM2)

The devices embed two low-power timers. These timers have an independent clock and are running in Stop mode if they are clocked by LSE, LSI or an external clock. They are able to wakeup the system from Stop mode.

LPTIM1 is active in Stop 0, Stop 1 and Stop 2 modes.

LPTIM2 is active in Stop 0 and Stop 1 mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous/ one shot mode
- Selectable software/hardware input trigger
- Selectable clock source
  - Internal clock sources: LSE, LSI, HSI16 or APB clock
  - External clock source over LPTIM input (working even with no internal clock source running, used by pulse counter application).
- Programmable digital glitch filter
- Encoder mode (LPTIM1 only)

### 3.23.5 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC (LSI) and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

### 3.23.6 System window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

## 3.28 Serial peripheral interface (SPI)

Three SPI interfaces allow communication up to 40 Mbits/s in master and up to 24 Mbits/s slave modes, in half-duplex, full-duplex and simplex modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits. The SPI interfaces support NSS pulse mode, TI mode and Hardware CRC calculation.

All SPI interfaces can be served by the DMA controller.

## 3.29 Serial audio interfaces (SAI)

The device embeds 2 SAI. Refer to *Table 13: SAI implementation* for the features implementation. The SAI bus interface handles communications between the microcontroller and the serial audio protocol.

The SAI peripheral supports:

- Two independent audio sub-blocks which can be transmitters or receivers with their respective FIFO.
- 8-word integrated FIFOs for each audio sub-block.
- Synchronous or asynchronous mode between the audio sub-blocks.
- Master or slave configuration independent for both audio sub-blocks.
- Clock generator for each audio block to target independent audio frequency sampling when both audio sub-blocks are configured in master mode.
- Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit.
- Peripheral with large configurability and flexibility allowing to target as example the following audio protocol: I2S, LSB or MSB-justified, PCM/DSP, TDM, AC’97 and SPDIF out.
- Up to 16 slots available with configurable size and with the possibility to select which ones are active in the audio frame.
- Number of bits by frame may be configurable.
- Frame synchronization active level configurable (offset, bit length, level).
- First active bit position in the slot is configurable.
- LSB first or MSB first for data transfer.
- Mute mode.
- Stereo/Mono audio frame capability.
- Communication clock strobing edge configurable (SCK).
- Error flags with associated interrupts if enabled respectively.
  - Overrun and underrun detection.
  - Anticipated frame synchronization signal detection in slave mode.
  - Late frame synchronization signal detection in slave mode.
  - Codec not ready for the AC’97 mode in reception.
- Interruption sources when enabled:
  - Errors.
  - FIFO requests.
- DMA interface with 2 dedicated channels to handle access to the dedicated integrated FIFO of each SAI audio sub-block.

- Transmission
  - Three transmit mailboxes
  - Configurable transmit priority
- Reception
  - Two receive FIFOs with three stages
  - 14 Scalable filter banks
  - Identifier list feature
  - Configurable FIFO overrun
- Time-triggered communication option
  - Disable automatic retransmission mode
  - 16-bit free running timer
  - Time Stamp sent in last two data bytes
- Management
  - Maskable interrupts
  - Software-efficient mailbox mapping at a unique address space

## 3.32 Secure digital input/output and MultiMediaCards Interface (SDMMC)

The card host interface (SDMMC) provides an interface between the APB peripheral bus and MultiMediaCards (MMCs), SD memory cards and SDIO cards.

The SDMMC features include the following:

- Full compliance with MultiMediaCard System Specification Version 4.2. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit
- Full compatibility with previous versions of MultiMediaCards (forward compatibility)
- Full compliance with SD Memory Card Specifications Version 2.0
- Full compliance with SD I/O Card Specification Version 2.0: card support for two different databus modes: 1-bit (default) and 4-bit
- Data transfer up to 48 MHz for the 8 bit mode
- Data write and read with DMA capability

## 3.33 Universal serial bus on-the-go full-speed (OTG_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG controller requires a dedicated 48 MHz clock that can be provided by the internal multispeed oscillator (MSI) automatically trimmed by 32.768 kHz external oscillator (LSE).This allows to use the USB device without external high speed crystal (HSE).

**Table 14. Legend/abbreviations used in the pinout table**

| Name | | Abbreviation | Definition |
|---|---|---|---|
| Pin name | | Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name | |
| Pin type | | S | Supply pin |
| | | I | Input only pin |
| | | I/O | Input / output pin |
| I/O structure | | FT | 5 V tolerant I/O |
| | | TT | 3.6 V tolerant I/O |
| | | B | Dedicated BOOT0 pin |
| | | RST | Bidirectional reset pin with embedded weak pull-up resistor |
| | | **Option for TT or FT I/Os** | |
| | | _f (1) | I/O, Fm+ capable |
| | | _u (2) | I/O, with USB function supplied by $V_{DDUSB}$ |
| | | _a (3) | I/O, with Analog switch function supplied by $V_{DDA}$ |
| Notes | | Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset. | |
| Pin functions | Alternate functions | Functions selected through GPIOx_AFR registers | |
| | Additional functions | Functions directly selected/enabled through peripheral registers | |

1. The related I/O structures in *Table 15* are: FT_f, FT_fa, FT_f, FT_fa.
2. The related I/O structures in *Table 15* are: FT_u.
3. The related I/O structures in *Table 15* are: FT_a, FT_fa, TT_a.

**Table 15. STM32L475xx pin definitions**

| Pin Number | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|
| LQFP64 | LQFP100 | | | | | Alternate functions | Additional functions |
| - | 1 | PE2 | I/O | FT | - | TRACECK, TIM3_ETR, TSC_G7_IO1, FMC_A23, SAI1_MCLK_A, EVENTOUT | - |
| - | 2 | PE3 | I/O | FT | - | TRACED0, TIM3_CH1, TSC_G7_IO2, FMC_A19, SAI1_SD_B, EVENTOUT | - |
| - | 3 | PE4 | I/O | FT | - | TRACED1, TIM3_CH2, DFSDM_DATIN3, TSC_G7_IO3, FMC_A20, SAI1_FS_A, EVENTOUT | - |

Table 15. STM32L475xx pin definitions (continued)

| Pin Number | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|
| LQFP64 | LQFP100 | | | | | Alternate functions | Additional functions |
| 55 | 89 | PB3 (JTDO-TRACESWO) | I/O | FT_a | (3) | JTDO-TRACESWO, TIM2_CH2, SPI1_SCK, SPI3_SCK, USART1_RTS_DE, SAI1_SCK_B, EVENTOUT | COMP2_INM |
| 56 | 90 | PB4 (NJTRST) | I/O | FT_a | (3) | NJTRST, TIM3_CH1, SPI1_MISO, SPI3_MISO, USART1_CTS, UART5_RTS_DE, TSC_G2_IO1, SAI1_MCLK_B, TIM17_BKIN, EVENTOUT | COMP2_INP |
| 57 | 91 | PB5 | I/O | FT_a | - | LPTIM1_IN1, TIM3_CH2, I2C1_SMBA, SPI1_MOSI, SPI3_MOSI, USART1_CK, UART5_CTS, TSC_G2_IO2, COMP2_OUT, SAI1_SD_B, TIM16_BKIN, EVENTOUT | - |
| 58 | 92 | PB6 | I/O | FT_fa | - | LPTIM1_ETR, TIM4_CH1, TIM8_BKIN2, I2C1_SCL, DFSDM_DATIN5, USART1_TX, TSC_G2_IO3, TIM8_BKIN2_COMP2, SAI1_FS_B, TIM16_CH1N, EVENTOUT | COMP2_INP |
| 59 | 93 | PB7 | I/O | FT_fa | - | LPTIM1_IN2, TIM4_CH2, TIM8_BKIN, I2C1_SDA, DFSDM_CKIN5, USART1_RX, UART4_CTS, TSC_G2_IO4, FMC_NL, TIM8_BKIN_COMP1, TIM17_CH1N, EVENTOUT | COMP2_INM, PVD_IN |
| 60 | 94 | BOOT0 | I | - | - | - | - |
| 61 | 95 | PB8 | I/O | FT_f | - | TIM4_CH3, I2C1_SCL, DFSDM_DATIN6, CAN1_RX, SDMMC1_D4, SAI1_MCLK_A, TIM16_CH1, EVENTOUT | - |
| 62 | 96 | PB9 | I/O | FT_f | - | IR_OUT, TIM4_CH4, I2C1_SDA, SPI2_NSS, DFSDM_CKIN6, CAN1_TX, SDMMC1_D5, SAI1_FS_A, TIM17_CH1, EVENTOUT | - |
| - | 97 | PE0 | I/O | FT | - | TIM4_ETR, FMC_NBL0, TIM16_CH1, EVENTOUT | - |

**Figure 12. $V_{REFINT}$ versus temperature**

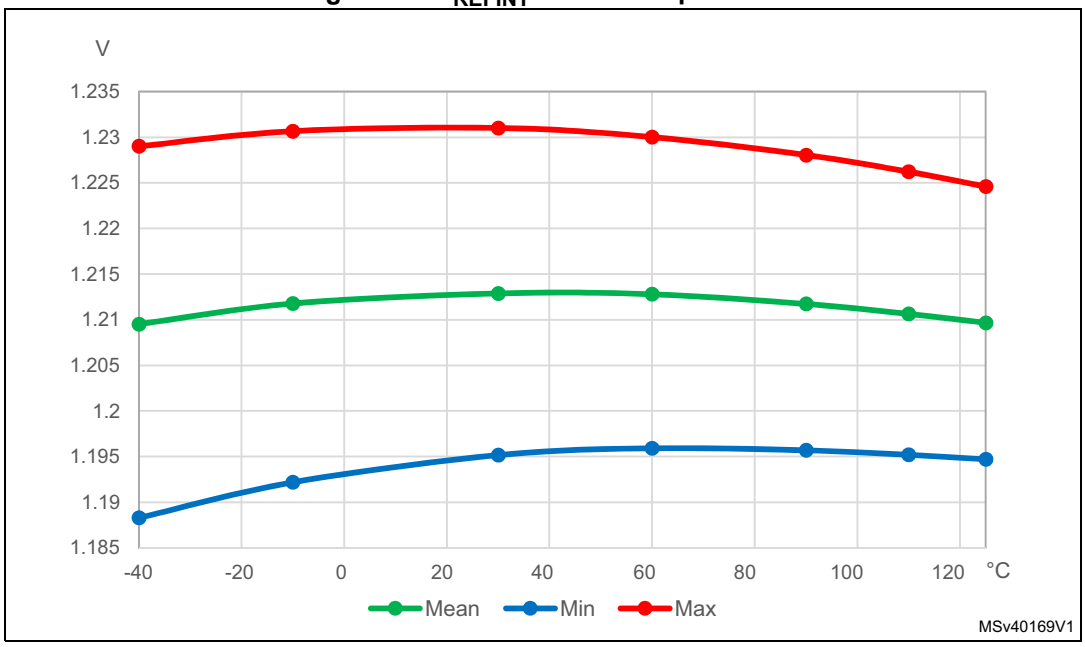


**Table 26. Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART enable (Cache ON Prefetch OFF)**

| Symbol | Parameter | Conditions | | | TYP | | | | | MAX(1) | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | - | Voltage scaling | $f_{HCLK}$ | 25 °C | 55 °C | 85 °C | 105 °C | 125 °C | 25 °C | 55 °C | 85 °C | 105 °C | 125 °C | |
| $I_{DD}$(Run) | Supply current in Run mode | $f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable | Range 2 | 26 MHz | 2.88 | 2.93 | 3.05 | 3.23 | 3.58 | 3.20 | 3.37 | 3.51 | 3.93 | 4.76 | mA |
| | | | | 16 MHz | 1.83 | 1.87 | 1.98 | 2.16 | 2.49 | 2.01 | 2.16 | 2.30 | 2.72 | 3.34 | |
| | | | | 8 MHz | 0.98 | 1.02 | 1.12 | 1.29 | 1.62 | 1.10 | 1.17 | 1.31 | 1.73 | 2.56 | |
| | | | | 4 MHz | 0.55 | 0.59 | 0.69 | 0.85 | 1.18 | 0.61 | 0.70 | 0.89 | 1.24 | 1.95 | |
| | | | | 2 MHz | 0.34 | 0.37 | 0.47 | 0.64 | 0.96 | 0.37 | 0.46 | 0.64 | 0.98 | 1.71 | |
| | | | | 1 MHz | 0.23 | 0.26 | 0.36 | 0.53 | 0.85 | 0.27 | 0.33 | 0.50 | 0.86 | 1.57 | |
| | | | | 100 kHz | 0.14 | 0.17 | 0.27 | 0.43 | 0.75 | 0.17 | 0.21 | 0.38 | 0.74 | 1.44 | |
| | | | Range 1 | 80 MHz | 10.2 | 10.3 | 10.5 | 10.7 | 11.1 | 11.22 | 11.8 | 12.1 | 12.5 | 13.3 | |
| | | | | 72 MHz | 9.24 | 9.31 | 9.47 | 9.69 | 10.1 | 10.16 | 10.7 | 11.0 | 11.4 | 12.2 | |
| | | | | 64 MHz | 8.25 | 8.32 | 8.46 | 8.68 | 9.09 | 9.08 | 9.6 | 9.9 | 10.3 | 11.1 | |
| | | | | 48 MHz | 6.28 | 6.35 | 6.5 | 6.72 | 7.11 | 6.91 | 7.3 | 7.6 | 8.0 | 8.8 | |
| | | | | 32 MHz | 4.24 | 4.30 | 4.44 | 4.65 | 5.04 | 4.66 | 4.97 | 5.26 | 5.67 | 6.51 | |
| | | | | 24 MHz | 3.21 | 3.27 | 3.4 | 3.61 | 3.98 | 3.53 | 3.76 | 4.05 | 4.46 | 5.30 | |
| | | | | 16 MHz | 2.19 | 2.24 | 2.36 | 2.56 | 2.94 | 2.41 | 2.66 | 2.95 | 3.16 | 3.99 | |
| $I_{DD}$(LPRun) | Supply current in Low-power run mode | $f_{HCLK} = f_{MSI}$ all peripherals disable | | 2 MHz | 272 | 303 | 413 | 592 | 958 | 330 | 393 | 579 | 954 | 1704 | µA |
| | | | | 1 MHz | 154 | 184 | 293 | 473 | 835 | 195 | 265 | 457 | 822 | 1572 | |
| | | | | 400 kHz | 78 | 108 | 217 | 396 | 758 | 110 | 180 | 380 | 755 | 1505 | |
| | | | | 100 kHz | 42 | 73 | 182 | 360 | 723 | 75 | 138 | 331 | 706 | 1456 | |

1. Guaranteed by characterization results, unless otherwise specified.

**Table 40. Peripheral current consumption (continued)**

| Peripheral | | Range 1 | Range 2 | Low-power run and sleep | Unit |
|---|---|---|---|---|---|
| AHB | SRAM2 | 1.6 | 1.4 | 1.6 | µA/MHz |
| | TSC | 1.8 | 1.4 | 1.6 | |
| | All AHB Peripherals | 118.5 | 77.3 | 87.6 | |
| APB1 | AHB to APB1 bridge(3) | 0.9 | 0.7 | 0.9 | µA/MHz |
| | CAN1 | 4.6 | 4.0 | 4.4 | |
| | DAC1 | 2.4 | 1.9 | 2.2 | |
| | I2C1 independent clock domain | 3.7 | 3.1 | 3.2 | |
| | I2C1 APB clock domain | 1.3 | 1.1 | 1.5 | |
| | I2C2 independent clock domain | 3.7 | 3.0 | 3.2 | |
| | I2C2 APB clock domain | 1.4 | 1.1 | 1.5 | |
| | I2C3 independent clock domain | 2.9 | 2.3 | 2.5 | |
| | I2C3 APB clock domain | 0.9 | 0.9 | 1.1 | |
| | LPUART1 independent clock domain | 2.1 | 1.6 | 2.0 | |
| | LPUART1 APB clock domain | 0.6 | 0.6 | 0.6 | |
| | LPTIM1 independent clock domain | 3.3 | 2.6 | 2.9 | |
| | LPTIM1 APB clock domain | 0.9 | 0.8 | 1.0 | |
| | LPTIM2 independent clock domain | 3.1 | 2.7 | 2.9 | |
| | LPTIM2 APB clock domain | 0.8 | 0.6 | 0.7 | |
| | OPAMP | 0.4 | 0.4 | 0.3 | |
| | PWR | 0.5 | 0.5 | 0.4 | |
| | SPI2 | 1.8 | 1.6 | 1.6 | |
| | SPI3 | 2.1 | 1.7 | 1.8 | |
| | SWPMI1 independent clock domain | 2.3 | 1.8 | 2.2 | |
| | SWPMI1 APB clock domain | 1.1 | 1.1 | 1.0 | |
| | TIM2 | 6.8 | 5.7 | 6.3 | |
| | TIM3 | 5.4 | 4.6 | 5.0 | |
| | TIM4 | 5.2 | 4.4 | 4.9 | |
| | TIM5 | 6.5 | 5.5 | 6.1 | |
| | TIM6 | 1.1 | 1.0 | 1.0 | |
| | TIM7 | 1.1 | 0.9 | 1.0 | |

### Multi-speed internal (MSI) RC oscillator

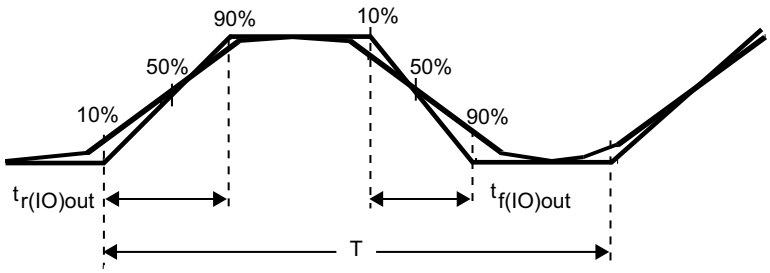
**Table 49. MSI oscillator characteristics(1)**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{MSI}$ | MSI frequency after factory calibration, done at $V_{DD}$=3 V and $T_A$=30 °C | MSI mode | Range 0 | 99 | 100 | 101 | kHz |
| | | | Range 1 | 198 | 200 | 202 | |
| | | | Range 2 | 396 | 400 | 404 | |
| | | | Range 3 | 792 | 800 | 808 | |
| | | | Range 4 | 0.99 | 1 | 1.01 | MHz |
| | | | Range 5 | 1.98 | 2 | 2.02 | |
| | | | Range 6 | 3.96 | 4 | 4.04 | |
| | | | Range 7 | 7.92 | 8 | 8.08 | |
| | | | Range 8 | 15.8 | 16 | 16.16 | |
| | | | Range 9 | 23.8 | 24 | 24.4 | |
| | | | Range 10 | 31.7 | 32 | 32.32 | |
| | | | Range 11 | 47.5 | 48 | 48.48 | |
| | | PLL mode XTAL= 32.768 kHz | Range 0 | - | 98.304 | - | kHz |
| | | | Range 1 | - | 196.608 | - | |
| | | | Range 2 | - | 393.216 | - | |
| | | | Range 3 | - | 786.432 | - | |
| | | | Range 4 | - | 1.016 | - | MHz |
| | | | Range 5 | - | 1.999 | - | |
| | | | Range 6 | - | 3.998 | - | |
| | | | Range 7 | - | 7.995 | - | |
| | | | Range 8 | - | 15.991 | - | |
| | | | Range 9 | - | 23.986 | - | |
| | | | Range 10 | - | 32.014 | - | |
| | | | Range 11 | - | 48.005 | - | |
| $\Delta_{TEMP}$(MSI)(2) | MSI oscillator frequency drift over temperature | MSI mode | $T_A$= -0 to 85 °C | -3.5 | - | 3 | % |
| | | | $T_A$= -40 to 125 °C | -8 | - | 6 | |

**Table 61. I/O AC characteristics(1)(2)**

| Speed | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| 00 | Fmax | Maximum frequency | C=50 pF, 2.7 V≤$V_{DDIOx}$≤3.6 V | - | 5 | MHz |
| | | | C=50 pF, 1.62 V≤$V_{DDIOx}$≤2.7 V | - | 1 | |
| | | | C=50 pF, 1.08 V≤$V_{DDIOx}$≤1.62 V | - | 0.1 | |
| | | | C=10 pF, 2.7 V≤$V_{DDIOx}$≤3.6 V | - | 10 | |
| | | | C=10 pF, 1.62 V≤$V_{DDIOx}$≤2.7 V | - | 1.5 | |
| | | | C=10 pF, 1.08 V≤$V_{DDIOx}$≤1.62 V | - | 0.1 | |
| | Tr/Tf | Output rise and fall time | C=50 pF, 2.7 V≤$V_{DDIOx}$≤3.6 V | - | 25 | ns |
| | | | C=50 pF, 1.62 V≤$V_{DDIOx}$≤2.7 V | - | 52 | |
| | | | C=50 pF, 1.08 V≤$V_{DDIOx}$≤1.62 V | - | 140 | |
| | | | C=10 pF, 2.7 V≤$V_{DDIOx}$≤3.6 V | - | 17 | |
| | | | C=10 pF, 1.62 V≤$V_{DDIOx}$≤2.7 V | - | 37 | |
| | | | C=10 pF, 1.08 V≤$V_{DDIOx}$≤1.62 V | - | 110 | |
| 01 | Fmax | Maximum frequency | C=50 pF, 2.7 V≤$V_{DDIOx}$≤3.6 V | - | 25 | MHz |
| | | | C=50 pF, 1.62 V≤$V_{DDIOx}$≤2.7 V | - | 10 | |
| | | | C=50 pF, 1.08 V≤$V_{DDIOx}$≤1.62 V | - | 1 | |
| | | | C=10 pF, 2.7 V≤$V_{DDIOx}$≤3.6 V | - | 50 | |
| | | | C=10 pF, 1.62 V≤$V_{DDIOx}$≤2.7 V | - | 15 | |
| | | | C=10 pF, 1.08 V≤$V_{DDIOx}$≤1.62 V | - | 1 | |
| | Tr/Tf | Output rise and fall time | C=50 pF, 2.7 V≤$V_{DDIOx}$≤3.6 V | - | 9 | ns |
| | | | C=50 pF, 1.62 V≤$V_{DDIOx}$≤2.7 V | - | 16 | |
| | | | C=50 pF, 1.08 V≤$V_{DDIOx}$≤1.62 V | - | 40 | |
| | | | C=10 pF, 2.7 V≤$V_{DDIOx}$≤3.6 V | - | 4.5 | |
| | | | C=10 pF, 1.62 V≤$V_{DDIOx}$≤2.7 V | - | 9 | |
| | | | C=10 pF, 1.08 V≤$V_{DDIOx}$≤1.62 V | - | 21 | |

**Figure 20. I/O AC characteristics definition(1)**




Maximum frequency is achieved if ($t_r$ + $t_f$ (≤ 2/3)T and if the duty cycle is (45-55%) when loaded by the specified capacitance.

MS32132V2

1. Refer to *Table 61: I/O AC characteristics*.

## 6.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, $R_{PU}$.

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*.

**Table 62. NRST pin characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$ | NRST input low level voltage | - | - | - | $0.3 \times V_{DDIOx}$ | V |
| $V_{IH(NRST)}$ | NRST input high level voltage | - | $0.7 \times V_{DDIOx}$ | - | - | |
| $V_{hys(NRST)}$ | NRST Schmitt trigger voltage hysteresis | - | - | 200 | - | mV |
| $R_{PU}$ | Weak pull-up equivalent resistor(2) | $V_{IN} = V_{SS}$ | 25 | 40 | 55 | kΩ |
| $V_{F(NRST)}$ | NRST input filtered pulse | - | - | - | 70 | ns |
| $V_{NF(NRST)}$ | NRST input not filtered pulse | 1.71 V ≤ $V_{DD}$ ≤ 3.6 V | 350 | - | - | ns |

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

**Table 64. ADC characteristics(1) (2) (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{LATRINJ}$ | Trigger conversion latency Injected channels aborting a regular conversion | CKMODE = 00 | 2.5 | 3 | 3.5 | $1/f_{ADC}$ |
| | | CKMODE = 01 | - | - | 3.0 | |
| | | CKMODE = 10 | - | - | 3.25 | |
| | | CKMODE = 11 | - | - | 3.125 | |
| $t_s$ | Sampling time | $f_{ADC}$ = 80 MHz | 0.03125 | - | 8.00625 | µs |
| | | - | 2.5 | - | 640.5 | $1/f_{ADC}$ |
| $t_{ADCVREG\_STUP}$ | ADC voltage regulator start-up time | - | - | - | 20 | µs |
| $t_{CONV}$ | Total conversion time (including sampling time) | $f_{ADC}$ = 80 MHz Resolution = 12 bits | 0.1875 | - | 8.1625 | µs |
| | | Resolution = 12 bits | ts + 12.5 cycles for successive approximation = 15 to 653 | | | $1/f_{ADC}$ |
| $I_{DDA}$(ADC) | ADC consumption from the $V_{DDA}$ supply | fs = 5 Msps | - | 730 | 830 | µA |
| | | fs = 1 Msps | - | 160 | 220 | |
| | | fs = 10 ksps | - | 16 | 50 | |
| $I_{DDV\_S}$(ADC) | ADC consumption from the $V_{REF+}$ single ended mode | fs = 5 Msps | - | 130 | 160 | µA |
| | | fs = 1 Msps | - | 30 | 40 | |
| | | fs = 10 ksps | - | 0.6 | 2 | |
| $I_{DDV\_D}$(ADC) | ADC consumption from the $V_{REF+}$ differential mode | fs = 5 Msps | - | 260 | 310 | µA |
| | | fs = 1 Msps | - | 60 | 70 | |
| | | fs = 10 ksps | - | 1.3 | 3 | |

1. Guaranteed by design
2. The I/O analog switch voltage booster is enable when $V_{DDA}$ < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA}$ < 2.4V). It is disable when $V_{DDA}$ ≥ 2.4 V.
3. $V_{REF+}$ can be internally connected to $V_{DDA}$ and $V_{REF-}$ can be internally connected to $V_{SSA}$, depending on the package. Refer to *Section 4: Pinouts and pin description* for further details.

**Table 66. ADC accuracy - limited test conditions 1(1)(2)(3) (continued)**

| Symbol | Parameter | Conditions(4) | | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| THD | Total harmonic distortion | ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, $V_{DDA} = V_{REF+} = 3$ V, TA = 25 °C | Single ended | Fast channel (max speed) | - | -74 | -73 | dB |
| | | | | Slow channel (max speed) | - | -74 | -73 | |
| | | | Differential | Fast channel (max speed) | - | -79 | -76 | |
| | | | | Slow channel (max speed) | - | -79 | -76 | |

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when $V_{DDA} < 2.4$ V (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA} < 2.4$ V). It is disable when $V_{DDA} \geq 2.4$ V. No oversampling.

### USB characteristics

The STM32L475xx USB interface is fully compliant with the USB specification version 2.0 and is USB-IF certified (for Full-speed device operation).

**Table 89. USB electrical characteristics**

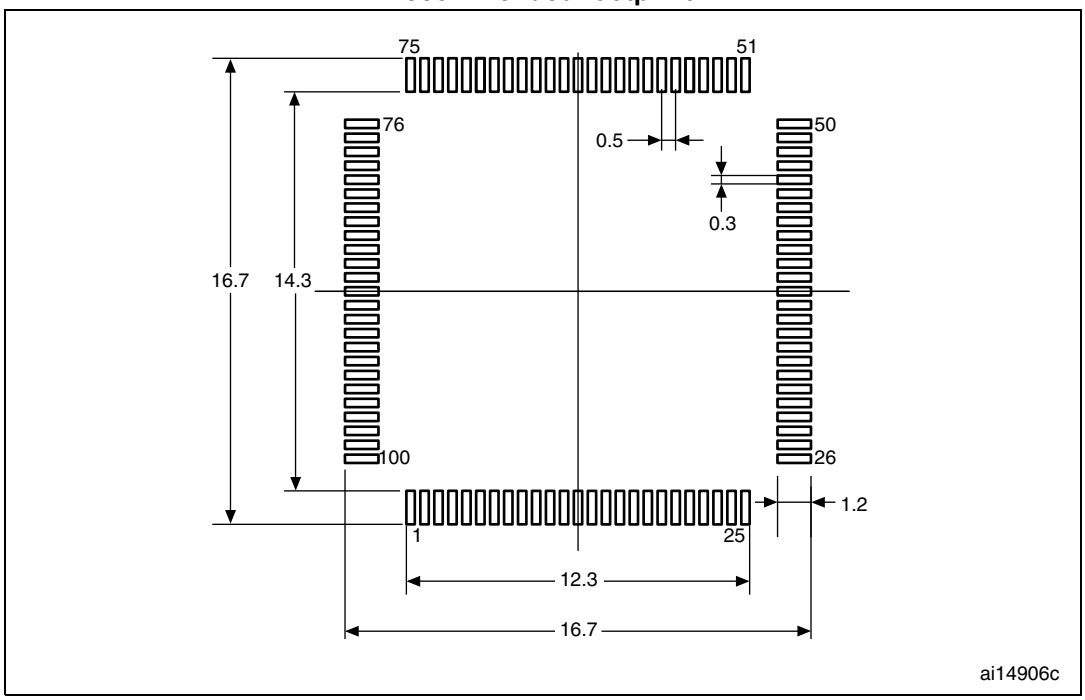
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDUSB}$ | USB transceiver operating voltage | | 3.0(1) | - | 3.6 | V |
| $R_{PUI}$ | Embedded USB_DP pull-up value during idle | | 900 | 1250 | 1600 | Ω |
| $R_{PUR}$ | Embedded USB_DP pull-up value during reception | | 1400 | 2300 | 3200 | |
| $Z_{DRV}$(2) | Output driver impedance(3) | Driving high and low | 28 | 36 | 44 | Ω |

1. The STM32L475xx USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V voltage range.
2. Guaranteed by design.
3. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-); the matching impedance is already included in the embedded driver.

### CAN (controller area network) interface

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

**Figure 39. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint**

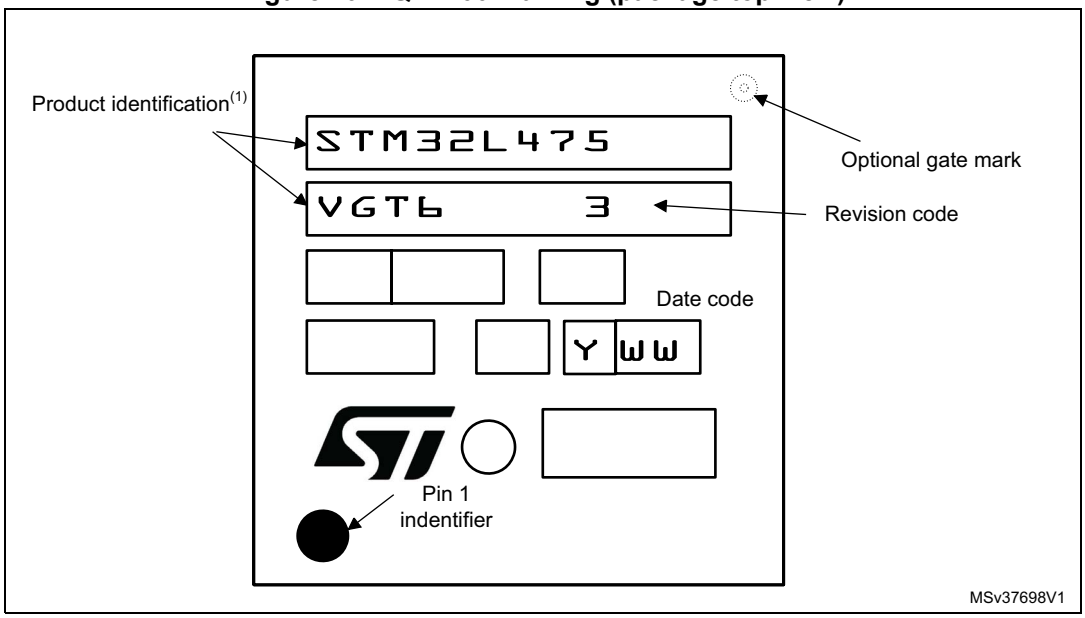



1. Dimensions are expressed in millimeters.

## Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

**Figure 40. LQFP100 marking (package top view)**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering