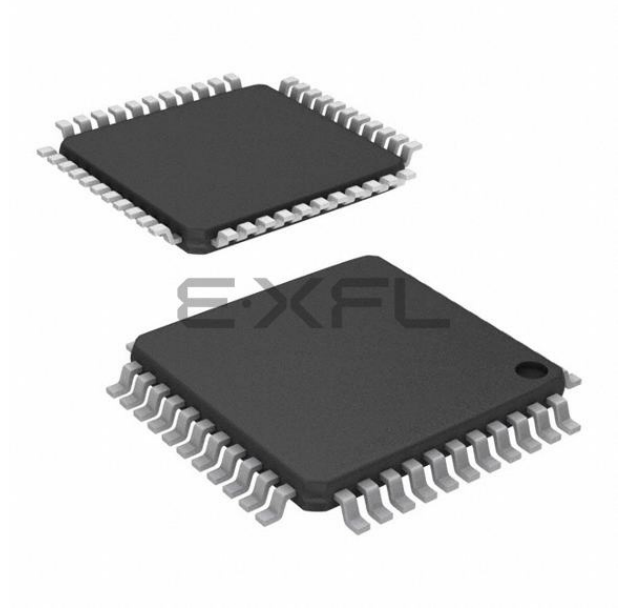

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SCI, SPI, USB OTG
Peripherals	LVD, PWM, WDT
Number of I/O	33
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf51jm128vld

2 Up to 16 pins on Ports A, H, and J are shared with the ColdFire Rapid GPIO module.

1.2 Block Diagram

Figure 1 shows the connections between the MCF51JM128 series pins and modules.

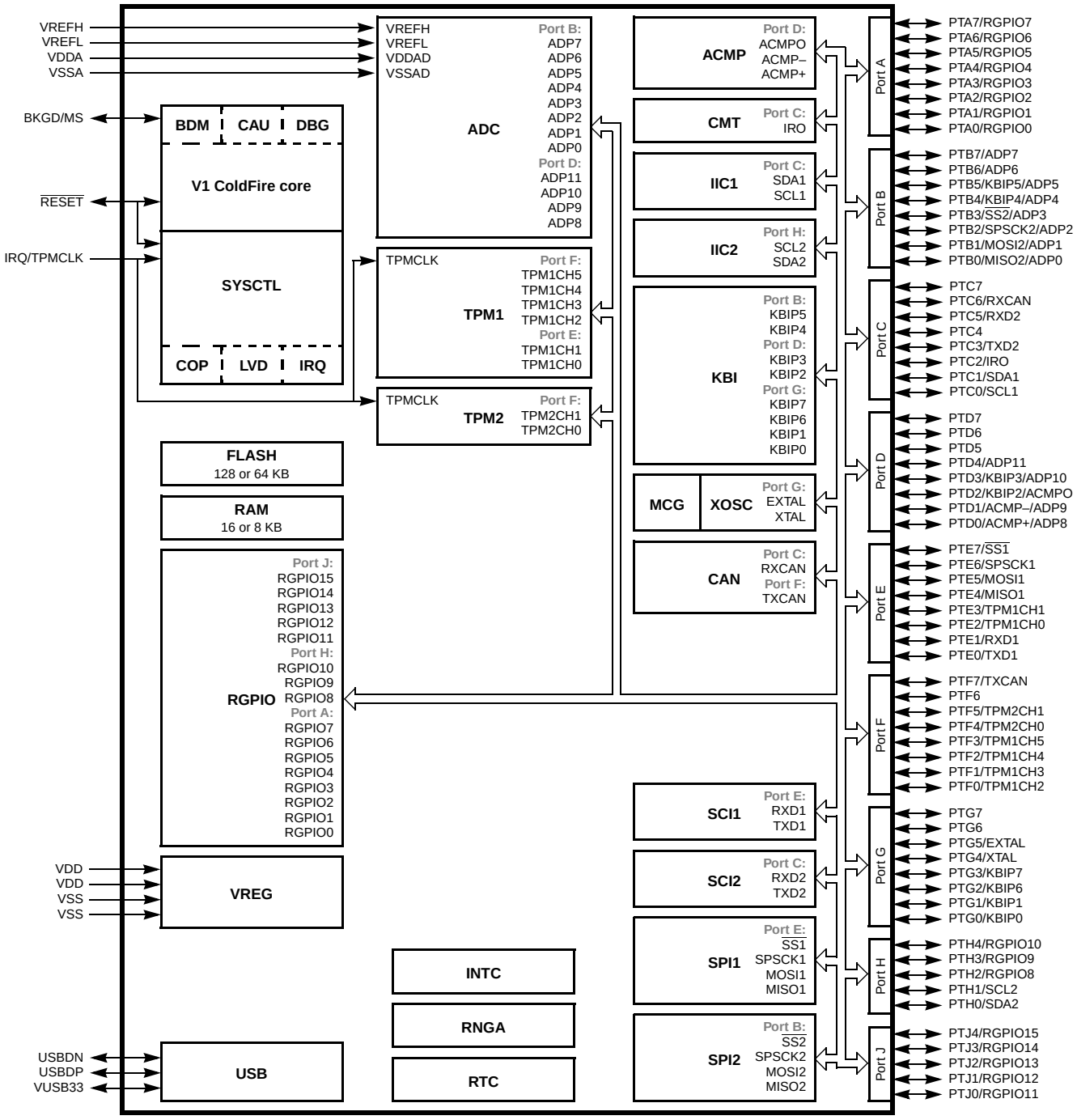


Figure 1. MCF51JM128 Block Diagram

Table 3. Orderable Part Number Summary (continued)

MCF51JM64EVLD	MCF51JM64 ColdFire Microcontroller with CAU and RNGA Enabled	64 / 16	44 LQFP	–40 to +105 °C
MCF51JM64VLD	MCF51JM64 ColdFire Microcontroller	64 / 16	44 LQFP	–40 to +105 °C
MCF51JM32EVLK	MCF51JM32 ColdFire Microcontroller with CAU and RNGA Enabled	32 / 16	80 LQFP	–40 to +105 °C
MCF51JM32VLK	MCF51JM32 ColdFire Microcontroller	32 / 16	80 LQFP	–40 to +105 °C
MCF51JM32EVLH	MCF51JM32 ColdFire Microcontroller with CAU and RNGA Enabled	32 / 16	64 LQFP	–40 to +105 °C
MCF51JM32VLH	MCF51JM32 ColdFire Microcontroller	32 / 16	64 LQFP	–40 to +105 °C
MCF51JM32EVQH	MCF51JM32 ColdFire Microcontroller with CAU and RNGA Enabled	32 / 16	64 QFP	–40 to +105 °C
MCF51JM32VQH	MCF51JM32 ColdFire Microcontroller	32 / 16	64 QFP	–40 to +105 °C
MCF51JM32EVLD	MCF51JM32 ColdFire Microcontroller with CAU and RNGA Enabled	32 / 16	44 LQFP	–40 to +105 °C
MCF51JM32VLD	MCF51JM32 ColdFire Microcontroller	32 / 16	44 LQFP	–40 to +105 °C

Figure 3 shows the pinout of the 64-pin LQFP and QFP.

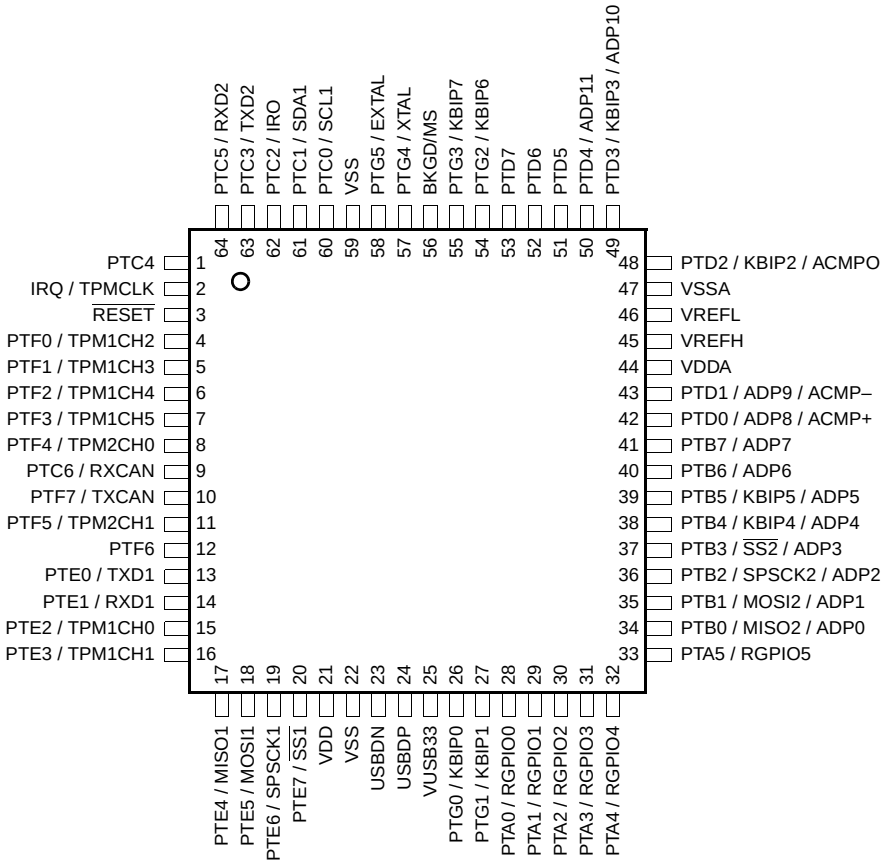


Figure 3. 64-pin QFP and LQFP

Table 4. Pin Assignments by Package and Pin Sharing Priority (continued)

Pin Number			<-- Lowest **Priority** --> Highest		
80	**64**	**44**	**Port Pin**	**Alt 1**	**Alt 2**
49	41	—	PTB7	ADP7	—
50	42	29	PTD0	ADP8	ACMP+
51	43	30	PTD1	ADP9	ACMP–
52	44	31	—	—	VDDA
53	45		—	—	VREFH
54	46	32	—	—	VREFL
55	47		—	—	VSSA
56	48	33	PTD2	KBIP2	ACMPO
57	—	—	PTJ0	RGPIO11	—
58	—	—	PTJ1	RGPIO12	—
59	—	—	PTJ2	RGPIO13	—
60	—	—	PTJ3	RGPIO14	—
61	—	—	PTJ4	RGPIO15	—
62	49	—	PTD3	KBIP3	ADP10
63	50	—	PTD4	ADP11	—
64	51	—	PTD5	—	—
65	52	—	PTD6	—	—
66	53	—	PTD7	—	—
67	54	34	PTG2	KBIP6	—
68	55	35	PTG3	KBIP7	—
69	56	36	—	BKGD	MS
70	57	37	PTG4	XTAL	
71	58	38	PTG5	EXTAL	
72	59	39	—	—	VSS
73	—	—	—	—	VDD
74	—	—	PTG6	—	—
75	—	—	PTG7	—	—
76	60	40	PTC0	SCL1	—
77	61	41	PTC1	SDA1	—
78	62	42	PTC2	IRO	—
79	63	43	PTC3	TXD2	—
80	64	44	PTC5	RXD2	—

[3] 1s - Single Layer Board, one signal layer
[4] 2s2p - Four Layer Board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °Cθ_{JA} = Package thermal resistance, junction-to-ambient, °C/W$P_D = P_{int} + P_{I/O}$$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations 1 and 2 iteratively for any value of T_A.

2.4 Electrostatic Discharge (ESD) Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (http://www.aecouncil.com/) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 8. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulse per pin	–	3	
Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table 10. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typ[1]	Max	Unit
7	P	Input low voltage; all digital inputs V_{DD} = 5V V_{DD} = 3V	V_{IL}	—	—	 1.75 1.05	V
8	P	Input hysteresis; all digital inputs	V_{hys}	0.06 x V_{DD}			mV
9	P	Input leakage current; input only pins[3]	$\|I_{In}\|$	—	0.1	1	µA
10	P	High Impedance (off-state) leakage current[3]	$\|I_{OZ}\|$	—	0.1	1	µA
11	P	Internal pullup resistors[4]	R_{PU}	20	45	65	kΩ
12	P	Internal pulldown resistors[5]	R_{PD}	20	45	65	kΩ
13		Internal pullup resistor to USBDP (to V_{USB33}) Idle Transmit	R_{PUPD}	 900 1425	 1300 2400	 1575 3090	kΩ
14	C	Input Capacitance; all non-supply pins	C_{In}	—	—	8	pF
15	D	RAM retention voltage[6]	V_{RAM}	—	0.6	1.0	V
16	P	POR rearm voltage	V_{POR}	0.9	1.4	2.0	V
17	D	POR rearm time	t_{POR}	10	—	—	µs
18	P	Low-voltage detection threshold — high range V_{DD} falling V_{DD} rising	V_{LVD1}	 3.9 4.0	 4.0 4.1	 4.1 4.2	V
19	P	Low-voltage detection threshold — low range V_{DD} falling V_{DD} rising	V_{LVD0}	 2.48 2.54	 2.56 2.62	 2.64 2.70	V
20	C	Low-voltage warning threshold — high range 1 V_{DD} falling V_{DD} rising	V_{LVW3}	 4.5 4.6	 4.6 4.7	 4.7 4.8	V
21	P	Low-voltage warning threshold — high range 0 V_{DD} falling V_{DD} rising	V_{LVW2}	 4.2 4.3	 4.3 4.4	 4.4 4.5	V
22	P	Low-voltage warning threshold low range 1 V_{DD} falling V_{DD} rising	V_{LVW1}	 2.84 2.90	 2.92 2.98	 3.00 3.06	V
23	C	Low-voltage warning threshold — low range 0 V_{DD} falling V_{DD} rising	V_{LVW0}	 2.66 2.72	 2.74 2.80	 2.82 2.88	V
24	T	Low-voltage inhibit reset/recover hysteresis 5 V 3 V	V_{hys}	 — —	 100 60	 — —	mV

1 Typical values are based on characterization data at 25°C unless otherwise stated.
2 Operating voltage with USB enabled can be found in Section 2.14, “USB Electricals.”
3 Measured with $V_{In} = V_{DD}$ or V_{SS}.
4 Measured with $V_{In} = V_{SS}$.
5 Measured with $V_{In} = V_{DD}$.
6 This is the voltage below which the contents of RAM are not guaranteed to be maintained.

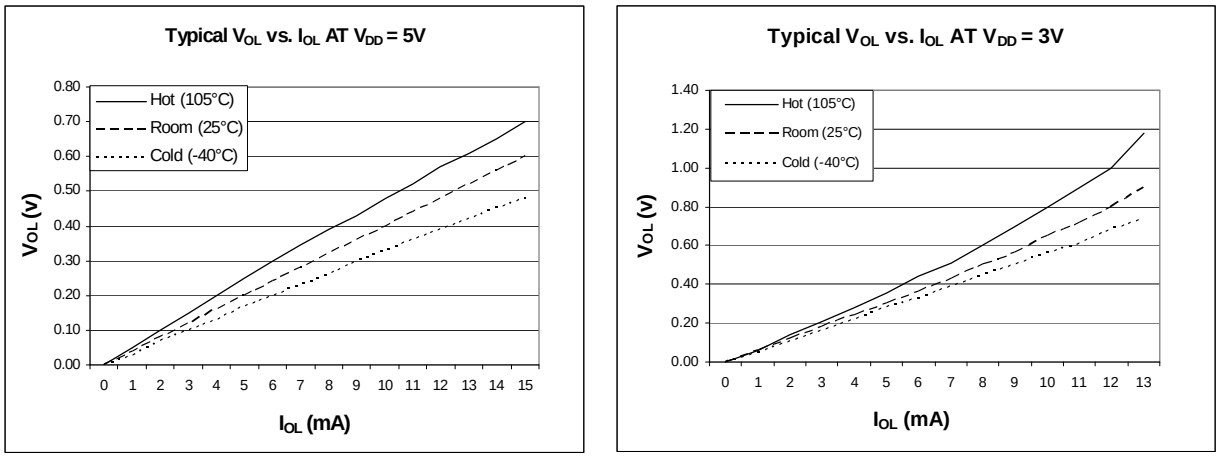


Figure 5. Typical Low-side Drive (sink) characteristics – High Drive (PTxDSn = 1)

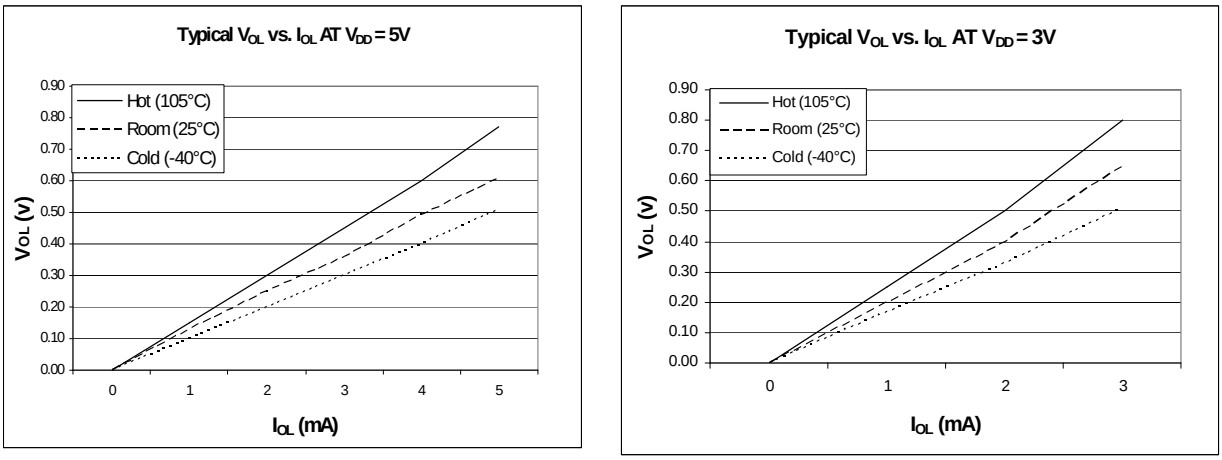


Figure 6. Typical Low-side Drive (sink) characteristics – Low Drive (PTxDSn = 0)

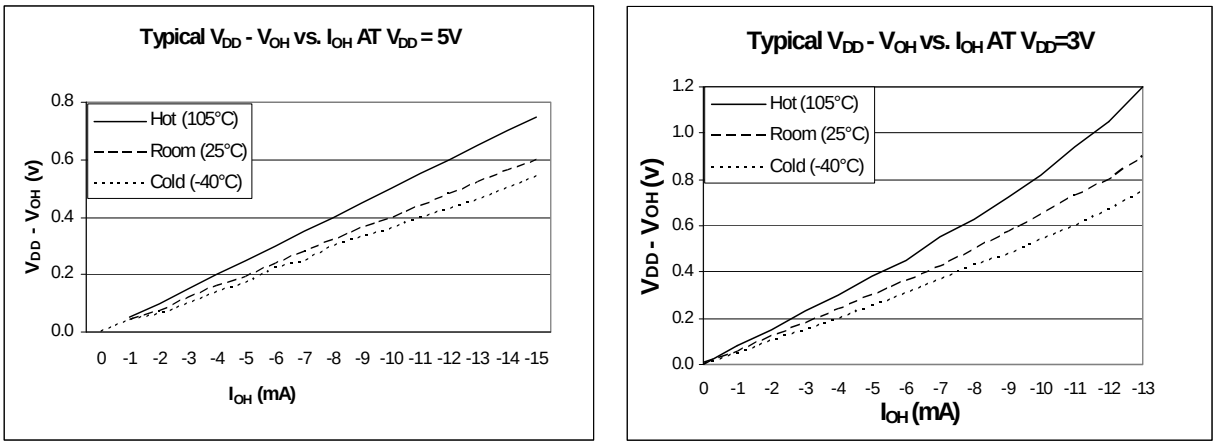


Figure 7. Typical High-side Drive (source) characteristics – High Drive (PTxDSn = 1)

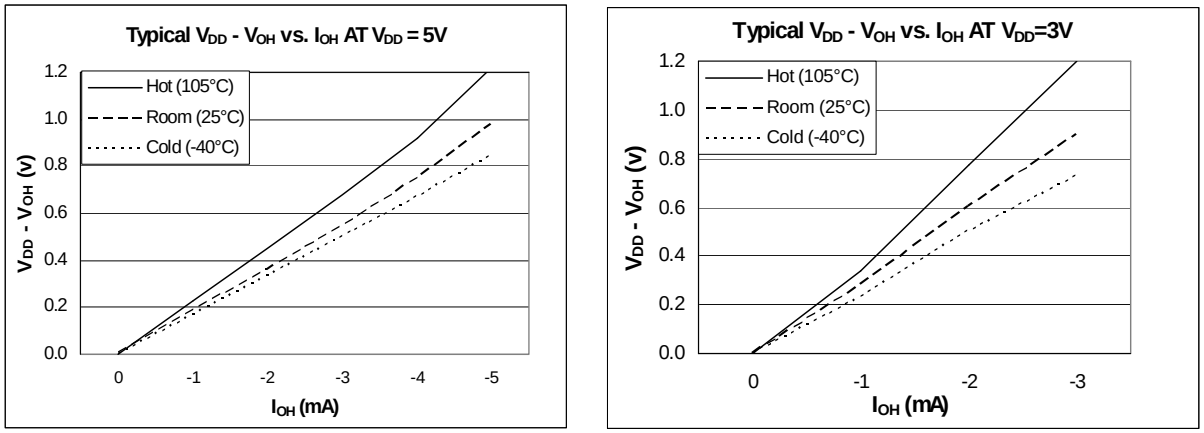


Figure 8. Typical High-side Drive (source) characteristics – Low Drive (PTxDSn = 0)

2.6 Supply Current Characteristics

Table 11. Supply Current Characteristics

Num	C	Parameter	Symbol	V_{DD} (V)	Typical[1]	Max[2]	Unit
1	C	Run supply current[3] measured at (CPU clock = 2 MHz, f_{Bus} = 1 MHz)	RI_{DD}	5	4.0	7	mA
				3	4.0	7	
2	P	Run supply current[3] measured at (CPU clock = 16 MHz, f_{Bus} = 8 MHz)		5	19	30	mA
				3	18.7	30	
3	C	Run supply current[3] measured at (CPU clock = 48 MHz, f_{Bus} = 24 MHz)		5	45	70	mA
				3	44	70	

2.7 Analog Comparator (ACMP) Electricals

Table 12. Analog Comparator Electrical Specifications

Num	C	Rating	Symbol	Min	Typical	Max	Unit
1		Supply voltage	V_{DD}	2.7	—	5.5	V
2		Supply current (active)	I_{DDAC}	—	20	35	µA
3		Analog input voltage	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
4		Analog input offset voltage	V_{AIO}		20	40	mV
5		Analog Comparator hysteresis	V_H	3.0	6.0	20.0	mV
6		Analog input leakage current	I_{ALKG}	--	--	1.0	µA
7		Analog Comparator initialization delay	t_{AINIT}	—	—	1.0	µs
8		Bandgap Voltage Reference Factory trimmed at V_{DD} = 3.0 V, Temp = 25°C	V_{BG}	1.19	1.20	1.21	V

2.8 ADC Characteristics

Table 13. 5 Volt 12-bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	
	Delta to V_{DD} (V_{DD}-V_{DDA})[2]	ΔV_{DDA}	–100	0	+100	mV	
Ground voltage	Delta to V_{SS} (V_{SS}-V_{SSA})[2]	ΔV_{SSA}	–100	0	+100	mV	
Ref Voltage High		V_{REFH}	2.7	V_{DDA}	V_{DDA}	V	
Ref Voltage Low		V_{REFL}	V_{SSA}	V_{SSA}	V_{SSA}	V	
Input Voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
Input Capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input Resistance		R_{ADIN}	—	3	5	kΩ	
Analog Source Resistance	12 bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz	R_{AS}	 — —	 — —	 2 5	kΩ	External to MCU
	10 bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz		 — —	 — —	 5 10		
	8 bit mode (all valid f_{ADCK})		—	—	10		
ADC Conversion Clock Freq.	High Speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	
	Low Power (ADLPC=1)		0.4	—	4.0		

1 Typical values assume V_{DDA} = 5.0V, Temp = 25°C, f_{ADCK}=1.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

Table 14. 5 Volt 12-bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Comment
Conversion Time (Including sample time)	Short Sample (ADLSMP=0)	T	t_{ADC}	—	20	—	ADCK cycles	See Table 9 for conversion time variances
	Long Sample (ADLSMP=1)			—	40	—		
Sample Time	Short Sample (ADLSMP=0)	T	t_{ADS}	—	3.5	—	ADCK cycles	
	Long Sample (ADLSMP=1)			—	23.5	—		
Total Unadjusted Error	12 bit mode	T	E_{TUE}	—	±3.0	—	LSB[2]	Includes quantization
	10 bit mode	P		—	±1	±2.5		
	8 bit mode	T		—	±0.5	±1.0		
Differential Non-Linearity	12 bit mode	T	DNL	—	±1.75	—	LSB[2]	
	10 bit mode[3]	P		—	±0.5	±1.0		
	8 bit mode[3]	T		—	±0.3	±0.5		
Integral Non-Linearity	12 bit mode	T	INL	—	±1.5	—	LSB[2]	
	10 bit mode	T		—	±0.5	±1.0		
	8 bit mode	T		—	±0.3	±0.5		
Zero-Scale Error	12 bit mode	T	E_{ZS}	—	±1.5	—	LSB[2]	V_{ADIN} = V_{SSAD}
	10 bit mode	P		—	±0.5	±1.5		
	8 bit mode	T		—	±0.5	±0.5		
Full-Scale Error	12 bit mode	T	E_{FS}	—	±1	—	LSB[2]	V_{ADIN} = V_{DDAD}
	10 bit mode	T		—	±0.5	±1		
	8 bit mode	T		—	±0.5	±0.5		
Quantization Error	12 bit mode	D	E_Q	—	-1 to 0	—	LSB[2]	
	10 bit mode			—	—	±0.5		
	8 bit mode			—	—	±0.5		
Input Leakage Error	12 bit mode	D	E_{IL}	—	±1	—	LSB[2]	Pad leakage[4] * R_{AS}
	10 bit mode			—	±0.2	±2.5		
	8 bit mode			—	±0.1	±1		
Temp Sensor Voltage	25°C	D	V_{TEMP25}	—	1.396	—	V	
Temp Sensor Slope	-40°C - 25°C	D	m	—	3.266	—	mV/°C	
	25°C - 125°C			—	3.638	—		

1 Typical values assume V_{DDA} = 5.0V, Temp = 25°C, f_{ADCK}=1.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Monotonicity and No-Missing-Codes guaranteed in 10 bit and 8 bit modes

4 Based on input pad leakage current. Refer to pad electricals.

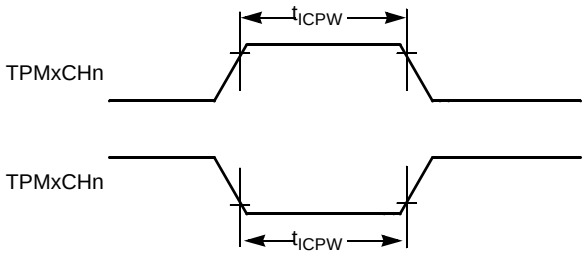


Figure 13. Timer Input Capture Pulse

2.11.3 MSCAN

Table 19. MSCAN Wake-up Pulse Characteristics

Num	C	Parameter	Symbol	Min	Typ[1]	Max	Unit
1	D	MSCAN Wake-up dominant pulse filtered	t_{WUP}			2	µs
2	D	MSCAN Wake-up dominant pulse pass	t_{WUP}	5		5	µs

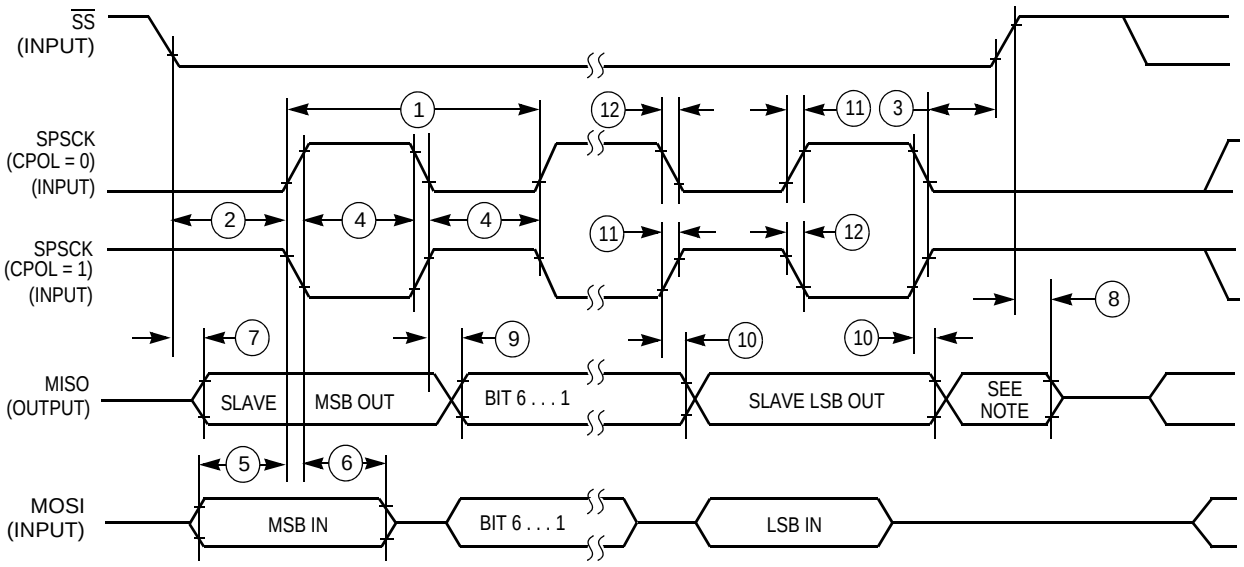
1 Typical values are based on characterization data at V_{DD} = 5.0V, 25°C unless otherwise stated.

2.12 SPI Characteristics

Table 20 and Figure 14 through Figure 17 describe the timing requirements for the SPI system.

Table 20. SPI Timing

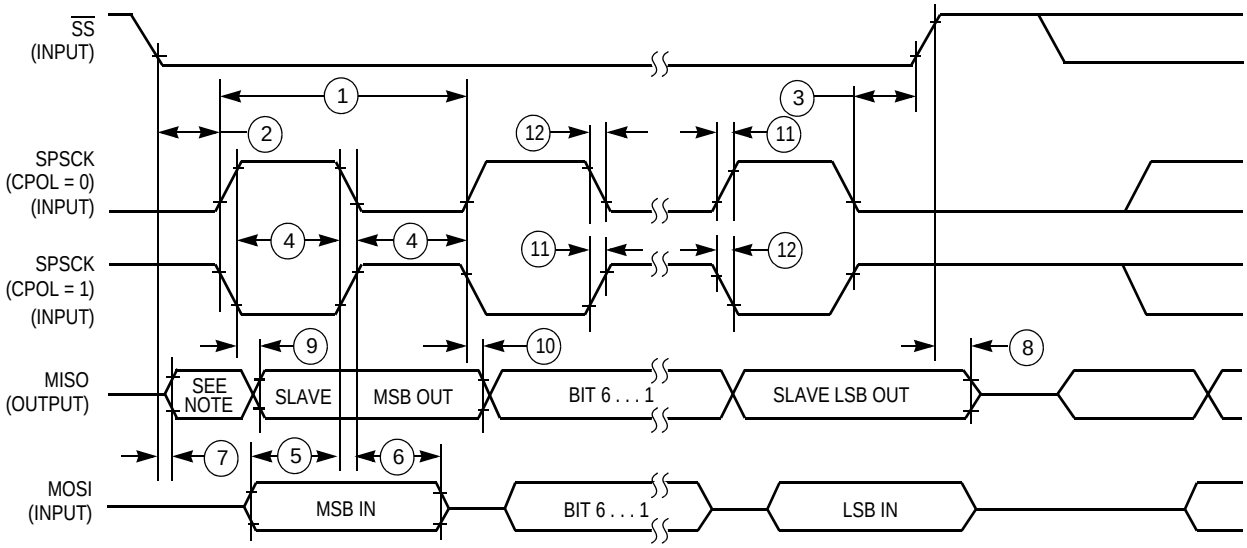
No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	$f_{Bus}/2048$ 0	$f_{Bus}/2$ $f_{Bus}/4$	Hz
1	D	SPSCK period Master Slave	t_{SPSCK}	2 4	2048 —	t_{cyc} t_{cyc}
2	D	Enable lead time Master Slave	t_{Lead}	1/2 1	— —	t_{SPSCK} t_{cyc}
3	D	Enable lag time Master Slave	t_{Lag}	1/2 1	— —	t_{SPSCK} t_{cyc}
4	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	$t_{cyc} - 30$ $t_{cyc} - 30$	1024 t_{cyc} —	ns ns
5	D	Data setup time (inputs) Master Slave	t_{SU}	15 15	— —	ns ns
6	D	Data hold time (inputs) Master Slave	t_{HI}	0 25	— —	ns ns
7	D	Slave access time	t_a	—	1	t_{cyc}
8	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
9	D	Data valid (after SPSCK edge) Master Slave	t_v	— —	25 25	ns ns
10	D	Data hold time (outputs) Master Slave	t_{HO}	0 0	— —	ns ns
11	D	Rise time Input Output	t_{RI} t_{RO}	— —	$t_{cyc} - 25$ 25	ns ns
12	D	Fall time Input Output	t_{FI} t_{FO}	— —	$t_{cyc} - 25$ 25	ns ns



NOTE:

1. Not defined but normally MSB of character just received

Figure 16. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined but normally LSB of character just received

Figure 17. SPI Slave Timing (CPHA = 1)

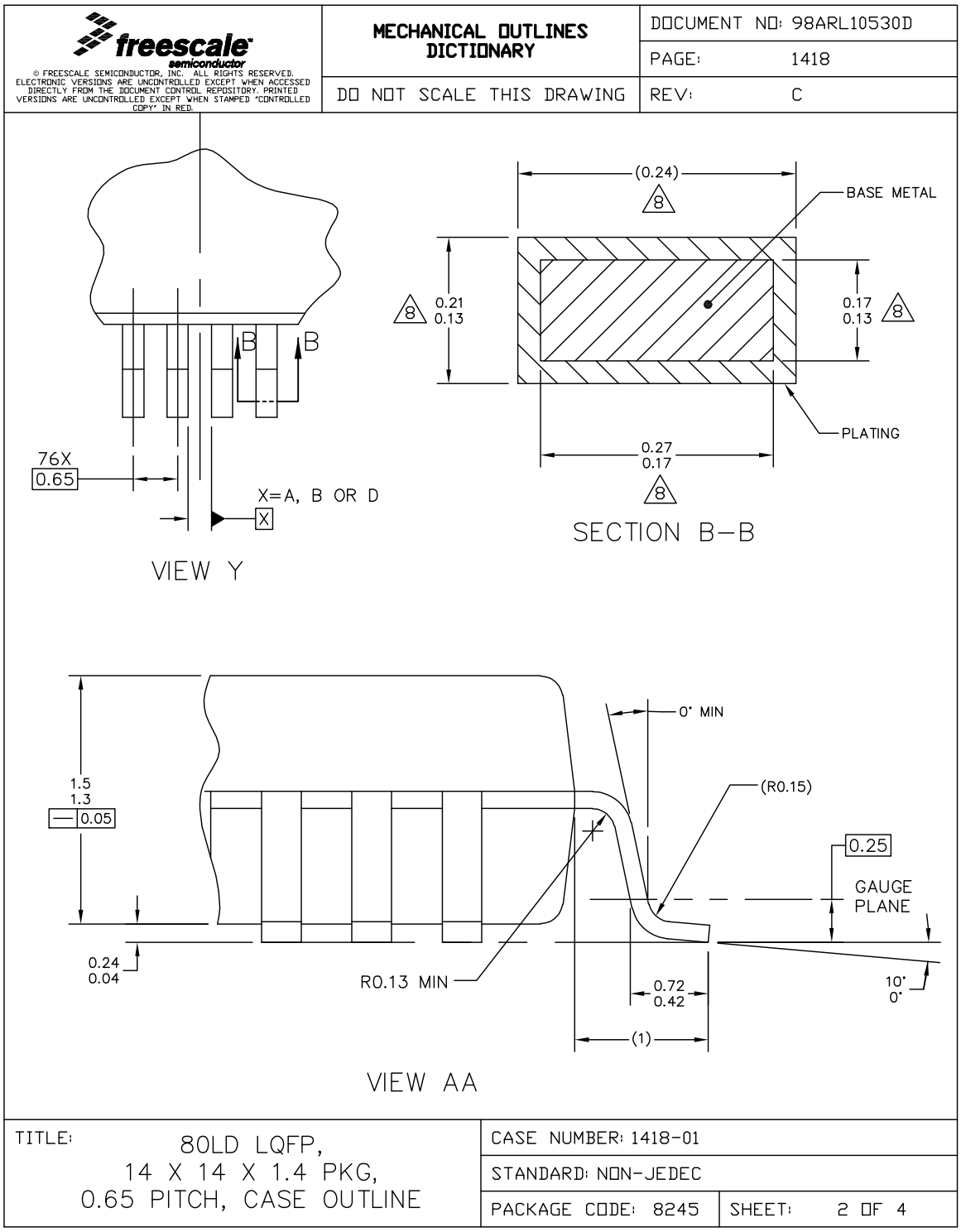


Figure 19. 80-pin LQFP Diagram - II

3.2 64-pin LQFP

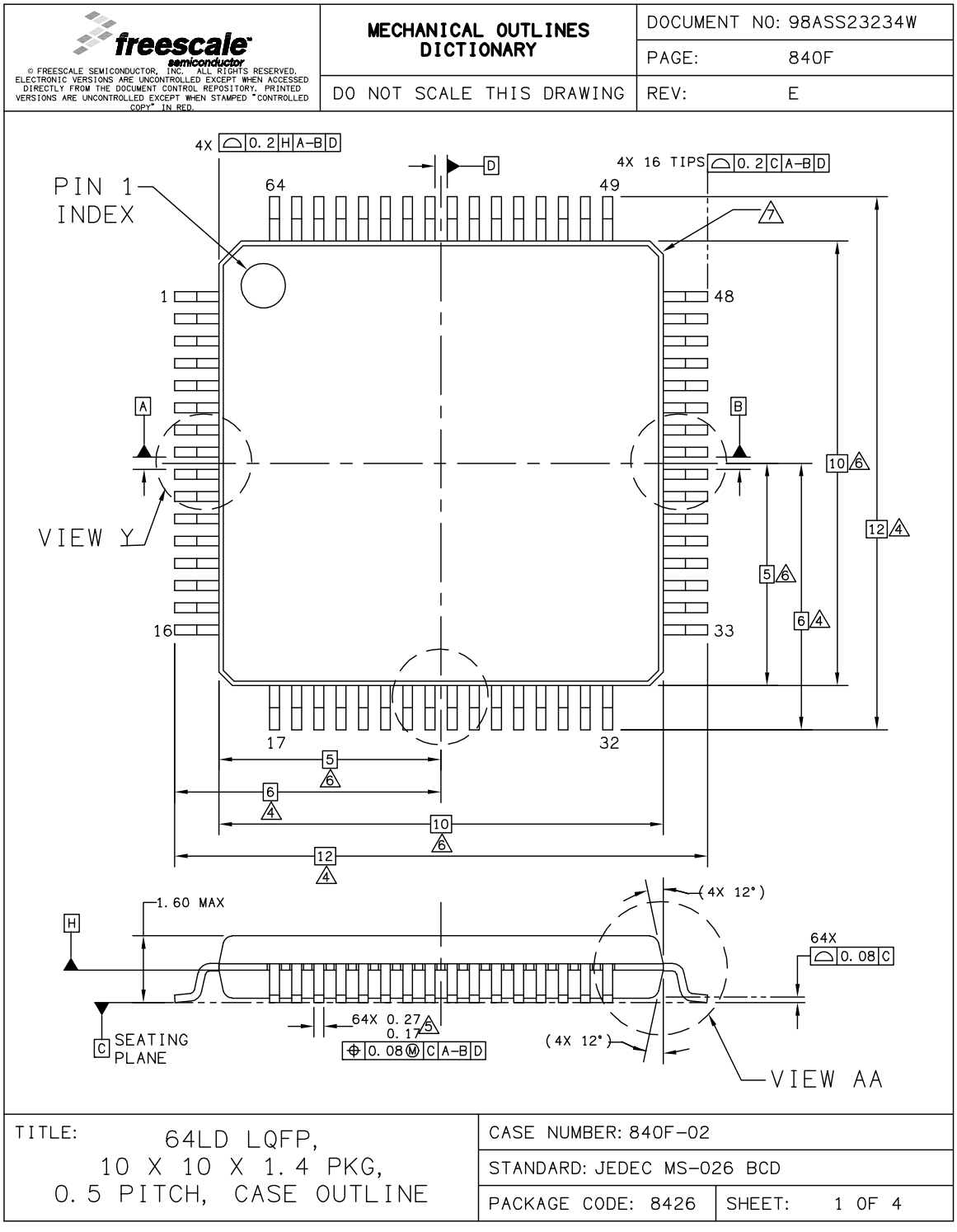


Figure 21. 64-pin LQFP Diagram - I

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NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	CASE NUMBER: 840F–02	
	STANDARD: JEDEC MS–026 BCD	
	PACKAGE CODE: 8426	SHEET: 3

Figure 23. 64-pin LQFP Diagram - III

3.3 64-pin QFP

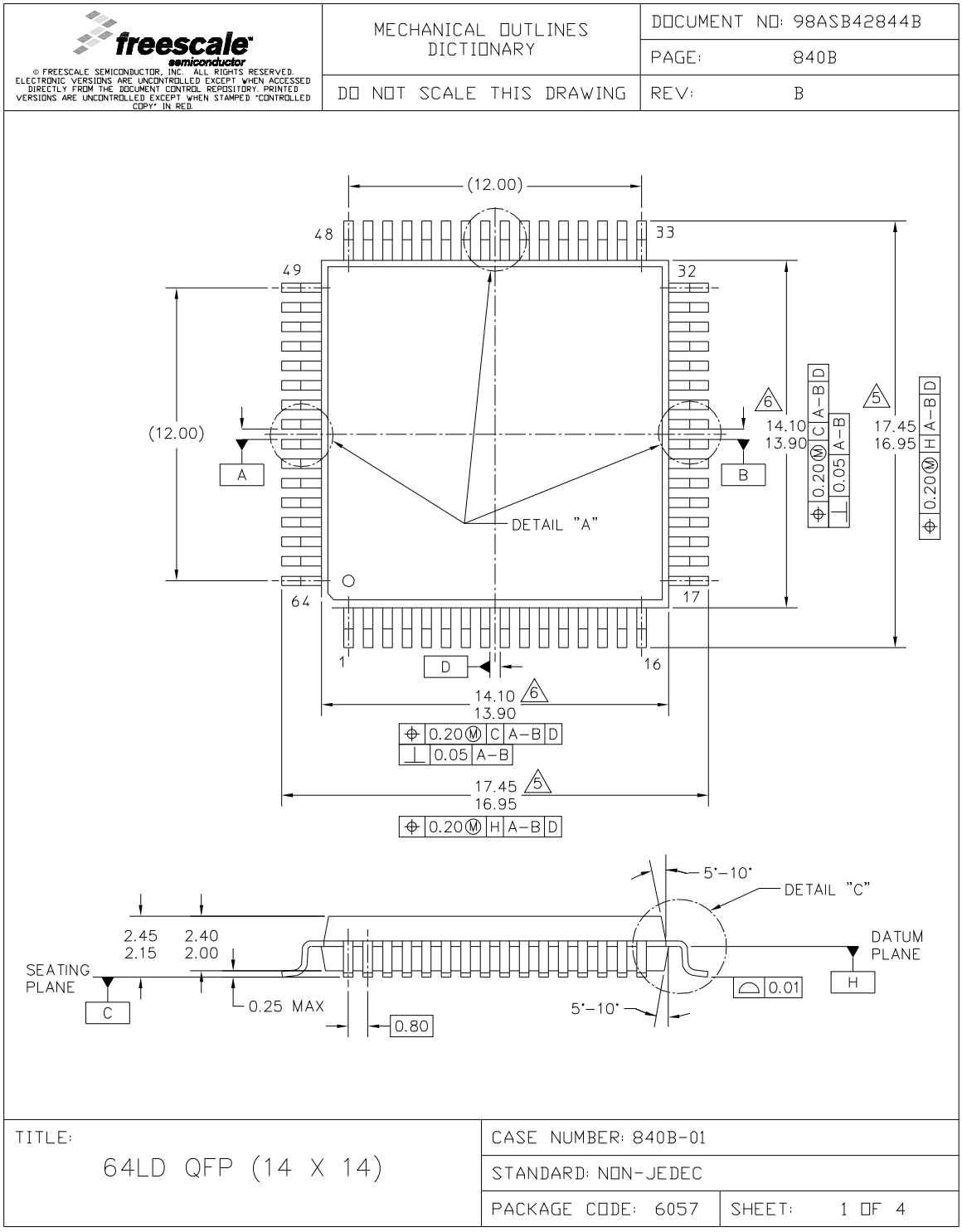

Figure 24. 64-pin QFP Diagram - I

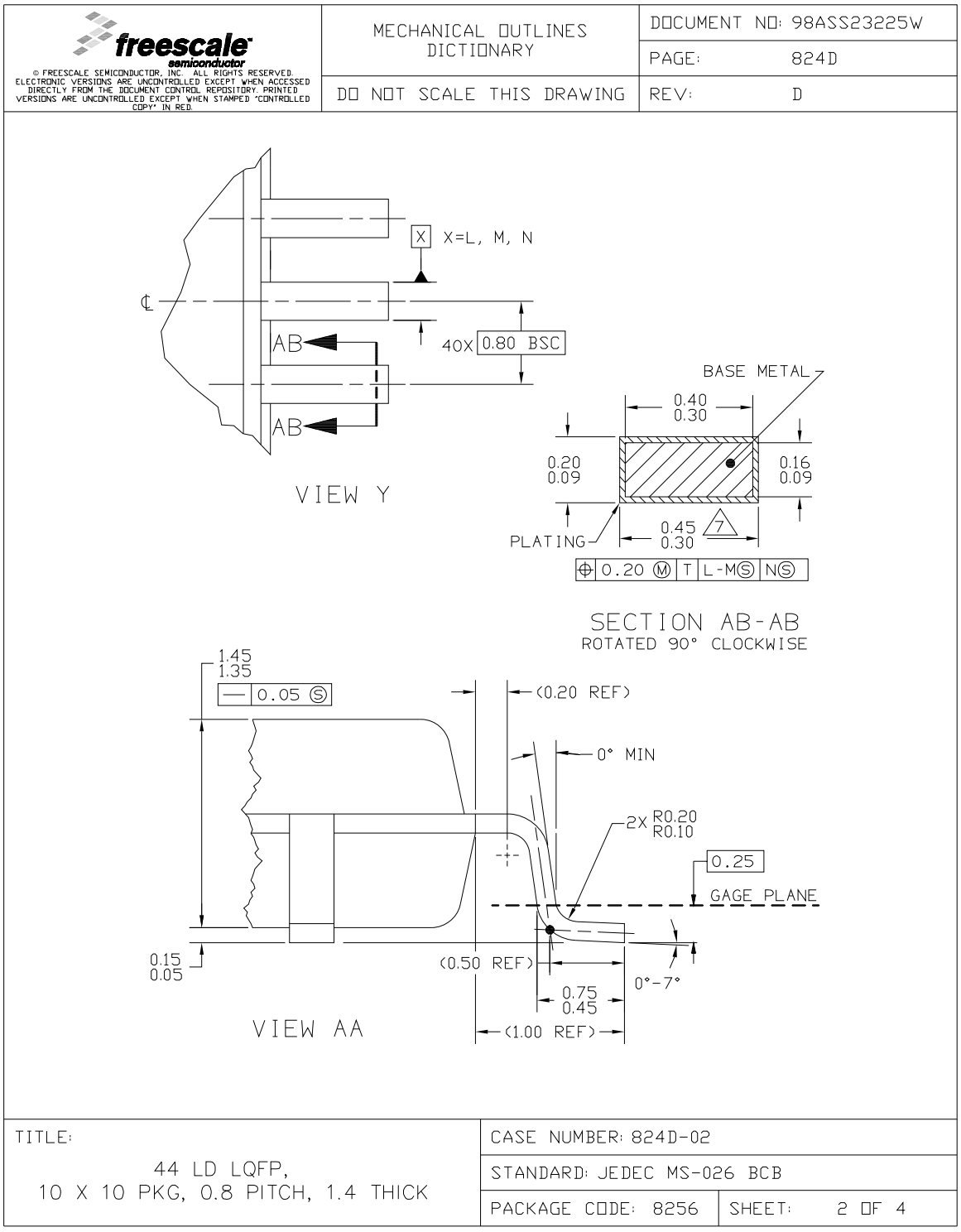

Figure 28. 44-pin LQFP Diagram - II

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23225W
		PAGE: 824D
	DO NOT SCALE THIS DRAWING	REV: D

NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DATUM PLANE H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS L, M AND N TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE T.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE DIMENSION TO EXCEED 0.53. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

TITLE: 44 LD LQFP, 10 X 10 PKG, 0.8 PITCH, 1.4 THICK	CASE NUMBER: 824D-02	
	STANDARD: JEDEC MS-026 BCB	
	PACKAGE CODE: 8256	SHEET: 3 OF 4

Figure 29. 44-pin LQFP Diagram - III

4 Revision History

This section lists major changes between versions of the MCF51JM128 Data Sheet document.

Table 23. Changes Between Revisions

Revision	Description
1	Updated features list Updated the figures Typical Low-side Drive (sink) characteristics – High Drive (PTxDSn = 1), Typical Low-side Drive (sink) characteristics – Low Drive (PTxDSn = 0), and Typical High-side Drive (source) characteristics – High Drive (PTxDSn = 1) Added the figure Typical High-side Drive (source) characteristics – Low Drive (PTxDSn = 0) Updated the table Supply Current Characteristics Updated the table Oscillator Electrical Specifications (Temperature Range = –40 to 105×C Ambient) Updated the table SPI Electrical Characteristic, DC Characteristics
2	Updated the table Orderable Part Number Summary, DC Characteristics, and Supply Current Characteristics
3	Updated the table Orderable Part Number Summary, MCG Characteristics, SPI Characteristics, and Supply Current Characteristics Changed V_{DDAD} to V_{DDA}, V_{SSAD} to V_{SSA} Updated the table Device comparison
4	Added “RAM retention voltage” parameter in “DC Characteristics” table, alongwith a table note. Added “Temp sensor voltage” parameter in “5 Volt 12-bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})” table. Added “ “Temp sensor slope” parameter in 5 Volt 12-bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) table. Also, corrected unit of “Temp sensor voltage” parameter in 5 Volt 12-bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) table.