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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, I²C, SCI, SPI, USB OTG
Peripherals	LVD, PWM, WDT
Number of I/O	66
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf51jm128vlk

1.3.1 Feature List

- 32-bit Version 1 ColdFire Central Processor Unit (CPU)
  - Up to 50.33 MHz at 2.7 V – 5.5 V
  - Performance (Dhrystone 2.1):
    - 0.94 Dhrystone 2.1 MIPS per MHz when running from internal RAM
    - 0.76 Dhrystone 2.1 MIPS per MHz when running from flash
  - Implements Instruction Set Revision C (ISA_C)
  - Supports up to 30 peripheral interrupt requests and seven software interrupts
- On-chip memory
  - Up to 128 KB Flash memory with read/program/erase over full operating voltage and temperature range
  - Up to 16 KB static random access memory (RAM)
  - Security circuitry to prevent unauthorized access to RAM and flash contents
- Power-saving modes
  - Two low-power stop plus wait modes
  - Peripheral clock enable register can disable clocks to unused modules, thereby reducing currents; this behavior allows clocks to remain enabled to specific perhipherals in Stop3 mode
  - Very lower power real-time counter for use in run, wait, and stop modes with internal and external clock sources
- Four Clock Source Options
  - Oscillator (XOSC) — Loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - FLL/PLL controlled by internal or external reference
  - Trimmable internal reference allows 0.2% resolution and 2% deviation
- System protection features
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock
  - Low-voltage detection with reset or interrupt; selectable trip points
  - Illegal opcode and illegal address detection with programmable reset or exception response
  - Flash block protection
- Debug support
  - Single-wire Background debug interface
  - 4 Program Counters plus two address (optional data) breakpoint registers with programmable 1- or 2-level trigger response
  - 64-entry processor status and debug data trace buffer with programmable start/stop conditions
- Universal Serial Bus (USB) On-The-Go dual-role controller
  - Full-speed USB device controller
    - Fully compliant with USB specification 1.1 and 2.0
    - 16 bidirectional endpoints, with double buffering to provide the maximum throughput
    - Supports control, bulk, interrupt, and isochronous endpoints
    - Supports bus-powered capability with low-power consumption
  - Full-speed / low-speed host controller
    - Host mode allows control, bulk, interrupt, and isochronous transfers
  - OTG protocol logic
  - On-chip USB transceiver
  - On-chip 3.3 V USB regulator and pull-up resistors save system cost

- RTC
  - 8-bit modulus counter with binary- or decimal-based prescaler
  - External clock source for precise time base, time-of-day, calendar or task scheduling functions
  - Free running on-chip low power oscillator (1 kHz) for cyclic wake-up without external components
- Carrier modulator timer (CMT)
  - carrier generator, modulator, and transmitter drive the infrared out (IRO) pin
  - operation in independent high/low time control, baseband, FSK, and direct IRO control modes
- Input/Output
  - 66 GPIOs
  - Eight keyboard interrupt pins with selectable polarity
  - Hysteresis and configurable pull-up device on all input pins; configurable slew rate and drive strength on all output pins
  - 16 bits of Rapid GPIO connected to the processor's local 32-bit platform bus with set, clear, and faster toggle functionality

1.4 Part Numbers

Table 3. Orderable Part Number Summary

Freescale Part Number	Description	Flash / SRAM (KB)	Package	Temperature
MCF51JM128EVLK	MCF51JM128 ColdFire Microcontroller with CAU and RNGA Enabled	128 / 16	80 LQFP	–40 to +105 °C
MCF51JM128VLK	MCF51JM128 ColdFire Microcontroller	128 / 16	80 LQFP	–40 to +105 °C
MCF51JM128EVLH	MCF51JM128 ColdFire Microcontroller with CAU and RNGA Enabled	128 / 16	64 LQFP	–40 to +105 °C
MCF51JM128VLH	MCF51JM128 ColdFire Microcontroller	128 / 16	64 LQFP	–40 to +105 °C
MCF51JM128EVQH	MCF51JM128 ColdFire Microcontroller with CAU and RNGA Enabled	128 / 16	64 QFP	–40 to +105 °C
MCF51JM128VQH	MCF51JM128 ColdFire Microcontroller	128 / 16	64 QFP	–40 to +105 °C
MCF51JM128EVLD	MCF51JM128 ColdFire Microcontroller with CAU and RNGA Enabled	128 / 16	44 LQFP	–40 to +105 °C
MCF51JM128VLD	MCF51JM128 ColdFire Microcontroller	128 / 16	44 LQFP	–40 to +105 °C
MCF51JM64EVLK	MCF51JM64 ColdFire Microcontroller with CAU and RNGA Enabled	64 / 16	80 LQFP	–40 to +105 °C
MCF51JM64VLK	MCF51JM64 ColdFire Microcontroller	64 / 16	80 LQFP	–40 to +105 °C
MCF51JM64EVLH	MCF51JM64 ColdFire Microcontroller with CAU and RNGA Enabled	64 / 16	64 LQFP	–40 to +105 °C
MCF51JM64VLH	MCF51JM64 ColdFire Microcontroller	64 / 16	64 LQFP	–40 to +105 °C
MCF51JM64EVQH	MCF51JM64 ColdFire Microcontroller with CAU and RNGA Enabled	64 / 16	64 QFP	–40 to +105 °C
MCF51JM64VQH	MCF51JM64 ColdFire Microcontroller	64 / 16	64 QFP	–40 to +105 °C

Table 3. Orderable Part Number Summary (continued)

MCF51JM64EVLD	MCF51JM64 ColdFire Microcontroller with CAU and RNGA Enabled	64 / 16	44 LQFP	–40 to +105 °C
MCF51JM64VLD	MCF51JM64 ColdFire Microcontroller	64 / 16	44 LQFP	–40 to +105 °C
MCF51JM32EVLK	MCF51JM32 ColdFire Microcontroller with CAU and RNGA Enabled	32 / 16	80 LQFP	–40 to +105 °C
MCF51JM32VLK	MCF51JM32 ColdFire Microcontroller	32 / 16	80 LQFP	–40 to +105 °C
MCF51JM32EVLH	MCF51JM32 ColdFire Microcontroller with CAU and RNGA Enabled	32 / 16	64 LQFP	–40 to +105 °C
MCF51JM32VLH	MCF51JM32 ColdFire Microcontroller	32 / 16	64 LQFP	–40 to +105 °C
MCF51JM32EVQH	MCF51JM32 ColdFire Microcontroller with CAU and RNGA Enabled	32 / 16	64 QFP	–40 to +105 °C
MCF51JM32VQH	MCF51JM32 ColdFire Microcontroller	32 / 16	64 QFP	–40 to +105 °C
MCF51JM32EVLD	MCF51JM32 ColdFire Microcontroller with CAU and RNGA Enabled	32 / 16	44 LQFP	–40 to +105 °C
MCF51JM32VLD	MCF51JM32 ColdFire Microcontroller	32 / 16	44 LQFP	–40 to +105 °C

Table 4. Pin Assignments by Package and Pin Sharing Priority (continued)

Pin Number			<-- Lowest **Priority** --> Highest		
80	**64**	**44**	**Port Pin**	**Alt 1**	**Alt 2**
49	41	—	PTB7	ADP7	—
50	42	29	PTD0	ADP8	ACMP+
51	43	30	PTD1	ADP9	ACMP–
52	44	31	—	—	VDDA
53	45		—	—	VREFH
54	46	32	—	—	VREFL
55	47		—	—	VSSA
56	48	33	PTD2	KBIP2	ACMPO
57	—	—	PTJ0	RGPIO11	—
58	—	—	PTJ1	RGPIO12	—
59	—	—	PTJ2	RGPIO13	—
60	—	—	PTJ3	RGPIO14	—
61	—	—	PTJ4	RGPIO15	—
62	49	—	PTD3	KBIP3	ADP10
63	50	—	PTD4	ADP11	—
64	51	—	PTD5	—	—
65	52	—	PTD6	—	—
66	53	—	PTD7	—	—
67	54	34	PTG2	KBIP6	—
68	55	35	PTG3	KBIP7	—
69	56	36	—	BKGD	MS
70	57	37	PTG4	XTAL	
71	58	38	PTG5	EXTAL	
72	59	39	—	—	VSS
73	—	—	—	—	VDD
74	—	—	PTG6	—	—
75	—	—	PTG7	—	—
76	60	40	PTC0	SCL1	—
77	61	41	PTC1	SDA1	—
78	62	42	PTC2	IRO	—
79	63	43	PTC3	TXD2	—
80	64	44	PTC5	RXD2	—

Table 6. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to + 5.8	V
Input voltage	V_{In}	– 0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	± 25	mA
Maximum current into V_{DD}	I_{DD}	120	mA
Storage temperature	T_{stg}	–55 to +150	°C
Maximum junction temperature	T_J	150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load shunt current is greater than maximum injection current. This is the greatest risk when the MCU is not consuming power. Examples: if no system clock is present or if the clock rate is low, which would reduce overall power consumption.

2.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} is small.

Table 7. Thermal Characteristics

Rating		Symbol	Value	Unit
Operating temperature range (packaged)		T_A	–40 to +105	°C
Thermal resistance [1,2,3,4]				
80-pin LQFP				
	1s		52	
	2s2p		40	
64-pin LQFP				
	1s		65	
	2s2p	θ_{JA}	47	°C/W
64-pin QFP				
	1s		54	
	2s2p		40	
44-pin LQFP				
	1s		69	
	2s2p		48	

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Junction to Ambient Natural Convection

[3] 1s - Single Layer Board, one signal layer
[4] 2s2p - Four Layer Board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °Cθ_{JA} = Package thermal resistance, junction-to-ambient, °C/W$P_D = P_{int} + P_{I/O}$$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations 1 and 2 iteratively for any value of T_A.

2.4 Electrostatic Discharge (ESD) Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (http://www.aecouncil.com/) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 8. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulse per pin	–	3	
Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table 9. ESD and Latch-Up Protection Characteristics

Num	Rating	Symbol	Min	Max	Unit
1	Human Body Model (HBM)	V_{HBM}	+/– 2000	—	V
2	Charge Device Model (CDM)	V_{CDM}	+/– 500	—	V
3	Latch-up Current at T_A = 105°C	I_{LAT}	+/– 100	—	mA

2.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 10. DC Characteristics

Num	C	Parameter	Symbol	Min	Typ[1]	Max	Unit
1		Operating voltage[2]		2.7	—	5.5	V
2	P	Output high voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = –4 mA 3 V, I_{Load} = –2 mA 5 V, I_{Load} = –2 mA 3 V, I_{Load} = –1 mA	V_{OH}	 V_{DD} – 1.5 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.8	 — — — —	 — — — —	V
		Output high voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = –15 mA 3 V, I_{Load} = –8 mA 5 V, I_{Load} = –8 mA 3 V, I_{Load} = –4 mA		 V_{DD} – 1.5 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.8	 — — — —	 — — — —	
3	P	Output low voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = 4mA 3 V, I_{Load} = 2 mA 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 1 mA	V_{OL}		 — — — —	 1.5 1.5 0.8 0.8	V
		Output low voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = 15 mA 3 V, I_{Load} = 8 mA 5 V, I_{Load} = 8 mA 3 V, I_{Load} = 4 mA			 — — — —	 1.5 1.5 0.8 0.8	
4	P	Output high current — Max total I_{OH} for all ports 5V 3V	I_{OHT}	 — —	 — —	 100 60	mA
5	P	Output low current — Max total I_{OL} for all ports 5V 3V	I_{OLT}	 — —	 — —	 100 60	mA
6	P	Input high voltage; all digital inputs	V_{IH}				V
		V_{DD} = 5V V_{DD} = 3V		3.25 2.10	— —	— —	

Table 10. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typ[1]	Max	Unit
7	P	Input low voltage; all digital inputs V_{DD} = 5V V_{DD} = 3V	V_{IL}	—	—	 1.75 1.05	V
8	P	Input hysteresis; all digital inputs	V_{hys}	0.06 x V_{DD}			mV
9	P	Input leakage current; input only pins[3]	$\|I_{In}\|$	—	0.1	1	µA
10	P	High Impedance (off-state) leakage current[3]	$\|I_{OZ}\|$	—	0.1	1	µA
11	P	Internal pullup resistors[4]	R_{PU}	20	45	65	kΩ
12	P	Internal pulldown resistors[5]	R_{PD}	20	45	65	kΩ
13		Internal pullup resistor to USBDP (to V_{USB33}) Idle Transmit	R_{PUPD}	 900 1425	 1300 2400	 1575 3090	kΩ
14	C	Input Capacitance; all non-supply pins	C_{In}	—	—	8	pF
15	D	RAM retention voltage[6]	V_{RAM}	—	0.6	1.0	V
16	P	POR rearm voltage	V_{POR}	0.9	1.4	2.0	V
17	D	POR rearm time	t_{POR}	10	—	—	µs
18	P	Low-voltage detection threshold — high range V_{DD} falling V_{DD} rising	V_{LVD1}	 3.9 4.0	 4.0 4.1	 4.1 4.2	V
19	P	Low-voltage detection threshold — low range V_{DD} falling V_{DD} rising	V_{LVD0}	 2.48 2.54	 2.56 2.62	 2.64 2.70	V
20	C	Low-voltage warning threshold — high range 1 V_{DD} falling V_{DD} rising	V_{LVW3}	 4.5 4.6	 4.6 4.7	 4.7 4.8	V
21	P	Low-voltage warning threshold — high range 0 V_{DD} falling V_{DD} rising	V_{LVW2}	 4.2 4.3	 4.3 4.4	 4.4 4.5	V
22	P	Low-voltage warning threshold low range 1 V_{DD} falling V_{DD} rising	V_{LVW1}	 2.84 2.90	 2.92 2.98	 3.00 3.06	V
23	C	Low-voltage warning threshold — low range 0 V_{DD} falling V_{DD} rising	V_{LVW0}	 2.66 2.72	 2.74 2.80	 2.82 2.88	V
24	T	Low-voltage inhibit reset/recover hysteresis 5 V 3 V	V_{hys}	 — —	 100 60	 — —	mV

1 Typical values are based on characterization data at 25°C unless otherwise stated.
2 Operating voltage with USB enabled can be found in Section 2.14, “USB Electricals.”
3 Measured with $V_{In} = V_{DD}$ or V_{SS}.
4 Measured with $V_{In} = V_{SS}$.
5 Measured with $V_{In} = V_{DD}$.
6 This is the voltage below which the contents of RAM are not guaranteed to be maintained.

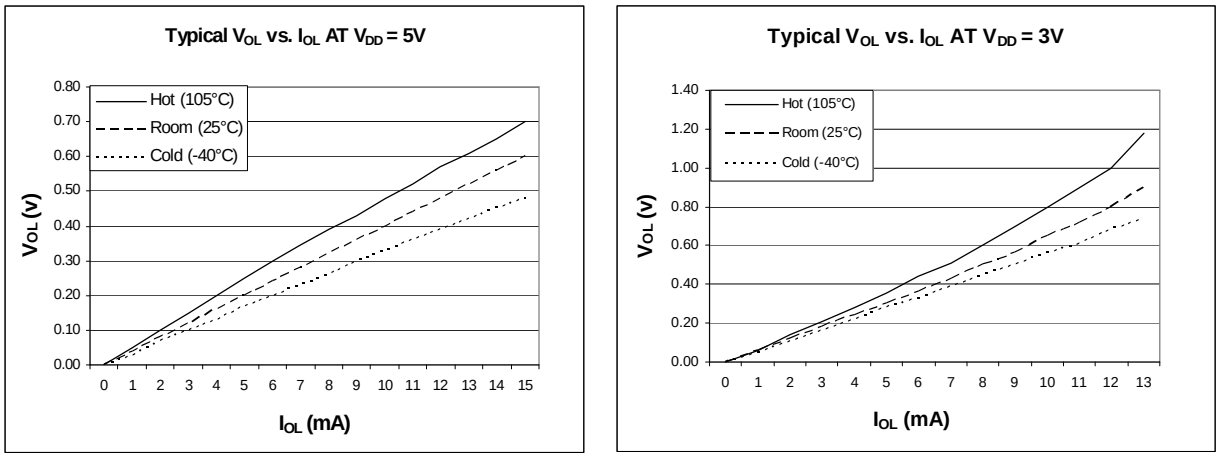


Figure 5. Typical Low-side Drive (sink) characteristics – High Drive (PTxDSn = 1)

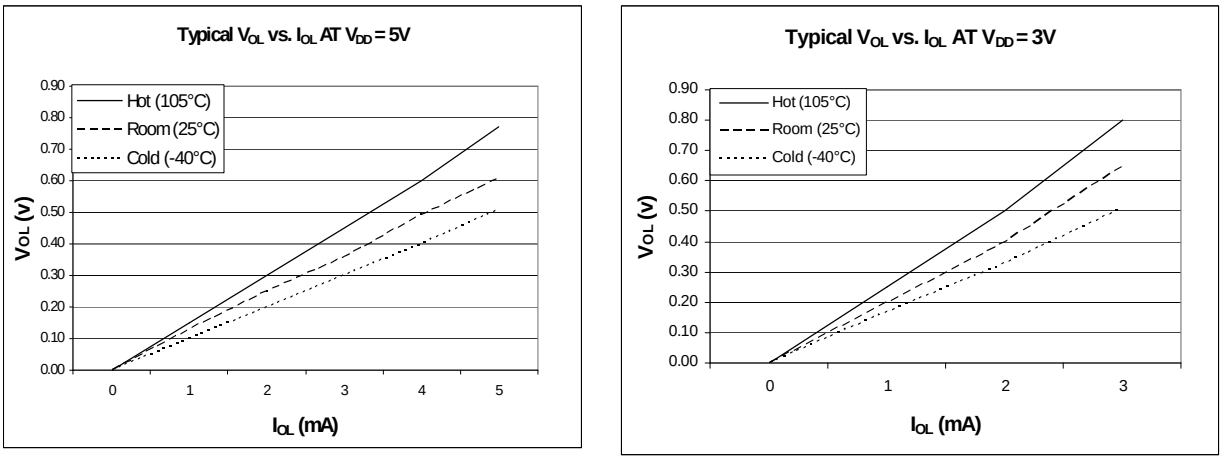


Figure 6. Typical Low-side Drive (sink) characteristics – Low Drive (PTxDSn = 0)

2.10 MCG Specifications

Table 16. MCG Frequency Specifications (Temperature Range = –40 to 125°C Ambient)

Num	C	Rating		Symbol	Min	Typical[1]	Max	Unit
1	P	Internal reference frequency - factory trimmed at V_{DD} = 5 V and temperature = 25 °C		f_{int_ft}	—	32.768	—	kHz
2	P	Average internal reference frequency – untrimmed		f_{int_ut}	31.25	—	39.0625	kHz
3	T	Internal reference startup time		t_{irefst}	—	60	100	µs
4	P	DCO output frequency range - untrimmed [2]	Low range (DRS=00)	f_{dco_ut}	16	—	20	MHz
	P		Mid range (DRS=01)		32	—	40	
	P		High range (DRS=10)		48	—	60	
5	P	DCO output frequency[2] Reference =32768Hz and DMX32 = 1	Low range (DRS=00)	f_{dco_DMX32}	—	19.92	—	MHz
	P		Mid range (DRS=01)		—	39.85	—	
	P		High range (DRS=10)		—	59.77	—	
6	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
7	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	$\%f_{dco}$
8	D	Total deviation of trimmed DCO output frequency over voltage and temperature		Δf_{dco_t}	—	0.5 –1.0	±2	$\%f_{dco}$
9	D	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 – 70 °C		Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$
10	D	FLL acquisition time [3]		$t_{fll\_acquire}$	—	—	1	ms
11	D	PLL acquisition time [4]		$t_{pll\_acquire}$	—	—	1	ms
12	D	Long term Jitter of DCO output clock (averaged over 2ms interval) [5]		C_{Jitter}	—	0.02	0.2	$\%f_{dco}$
13	D	VCO operating frequency		f_{vco}	7.0	—	55.0	MHz
14	D	Jitter of PLL output clock measured over 625 ns[6]		$f_{pll\_jitter\_625ns}$	—	0.566[5]	—	$\%f_{pll}$
15	D	Lock entry frequency tolerance [7]		D_{lock}	±1.49	—	±2.98	%
16	D	Lock exit frequency tolerance [8]		D_{unl}	±4.47	—	±5.97	%
17	D	Lock time — FLL		t_{fll_lock}	—	—	$t_{fll\_acquire}$+ 1075(1/f_{int_t})	s
18	D	Lock time — PLL		t_{pll_lock}	—	—	$t_{pll\_acquire}$+ 1075(1/f_{pll_ref})	s
19	D	Loss of external clock minimum frequency – RANGE = 0		f_{loc_low}	(3/5) x f_{int}	—	—	kHz

1 Data in Typical column was characterized at 5.0 V, 25C or is typical recommended value

2 The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

3 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

5 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

6 625 ns represents 5 time quanta for CAN applications, under worst case conditions of 8 MHz CAN bus clock, 1 Mbps CAN bus speed, and 8 time quanta per bit for bit time settings. 5 time quanta is the minimum time between a synchronization edge and the sample point of a bit using 8 time quanta per bit.

7 Below D_{lock} minimum, the MCG is guaranteed to enter lock. Above D_{lock} maximum, the MCG will not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.

8 Below D_{unl} minimum, the MCG will not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.

2.11 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

2.11.1 Control Timing

Table 17. Control Timing

Num	C	Parameter	Symbol	Min	Typ[1]	Max	Unit
1		Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	dc	—	24	MHz
2		Internal low-power oscillator period	t_{LPO}	700		1300	µs
3		External reset pulse width[2] ($t_{cyc} = 1/f_{Self\_reset}$)	t_{extrst}	100		—	ns
4		Reset low drive	t_{rstdrv}	66 x t_{cyc}		—	ns
5		Active background debug mode latch setup time	t_{MSSU}	500		—	ns
6		Active background debug mode latch hold time	t_{MSH}	100		—	ns
7		IRQ pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}, t_{IHIL}	 100 1.5 x t_{cyc}	—	—	ns
8		KBIPx pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}, t_{IHIL}	 100 1.5 x t_{cyc}	—	—	ns
9		Port rise and fall time (load = 50 pF)[4] Slew rate control disabled (PTxSE = 0) High drive Slew rate control enabled (PTxSE = 1) High drive Slew rate control disabled (PTxSE = 0) Low drive Slew rate control enabled (PTxSE = 1) Low drive	t_{Rise}, t_{Fall}	 — — 	 11 35 40 75		ns

1 Typical values are based on characterization data at V_{DD} = 5.0V, 25°C unless otherwise stated.

2 This is the shortest pulse guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

3 This is the minimum pulse width guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

4 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 105°C.

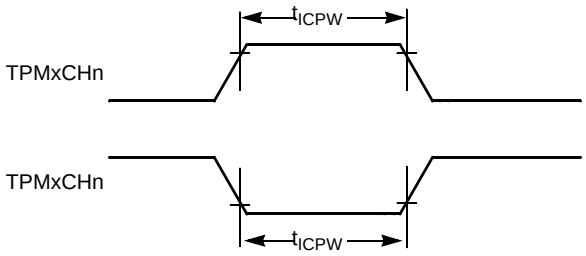


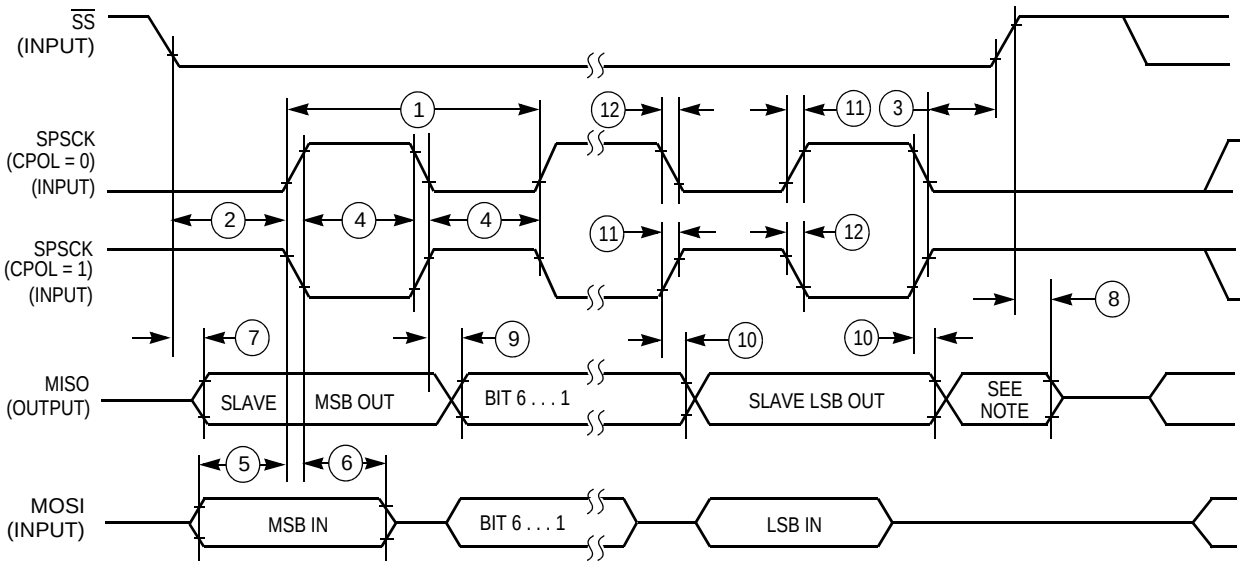
Figure 13. Timer Input Capture Pulse

2.11.3 MSCAN

Table 19. MSCAN Wake-up Pulse Characteristics

Num	C	Parameter	Symbol	Min	Typ[1]	Max	Unit
1	D	MSCAN Wake-up dominant pulse filtered	t_{WUP}			2	µs
2	D	MSCAN Wake-up dominant pulse pass	t_{WUP}	5		5	µs

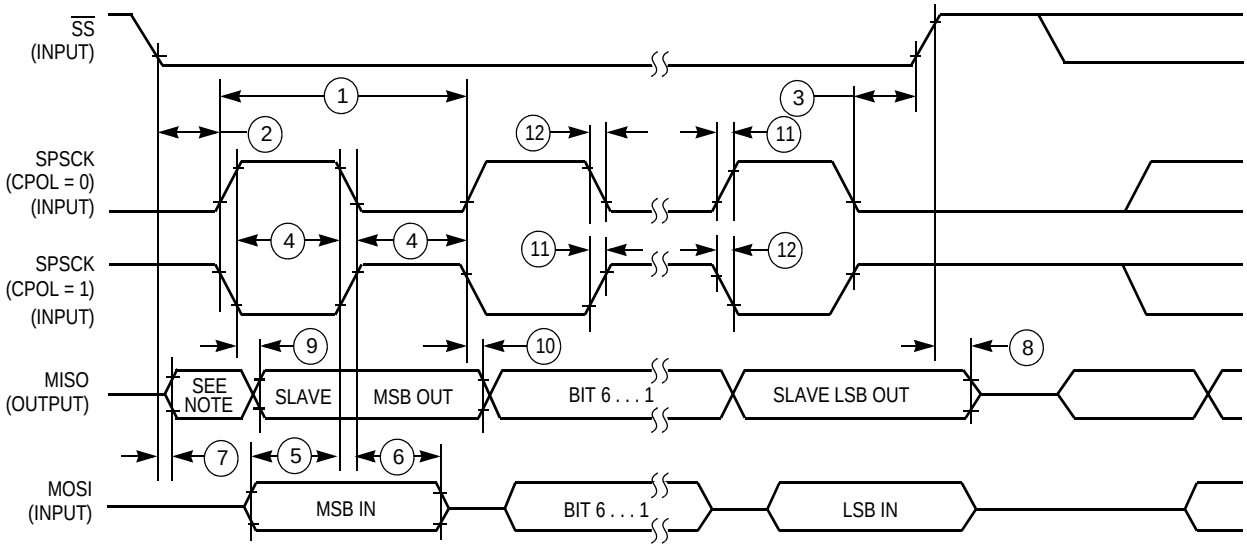
1 Typical values are based on characterization data at V_{DD} = 5.0V, 25°C unless otherwise stated.



NOTE:

1. Not defined but normally MSB of character just received

Figure 16. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined but normally LSB of character just received

Figure 17. SPI Slave Timing (CPHA = 1)

2.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply.

Table 21. Flash Characteristics

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1		Supply voltage for program/erase	$V_{prog/erase}$	2.7		5.5	V
2		Supply voltage for read operation	V_{Read}	2.7		5.5	V
3		Internal FCLK frequency[2]	f_{FCLK}	150		200	kHz
4		Internal FCLK period (1/FCLK)	t_{Fcyc}	5		6.67	µs
5		Byte program time (random location)(2)	t_{prog}	9			t_{Fcyc}
6		Byte program time (burst mode)(2)	t_{Burst}	4			t_{Fcyc}
7		Page erase time[3]	t_{Page}	4000			t_{Fcyc}
8		Mass erase time(2)	t_{Mass}	20,000			t_{Fcyc}
9	C	Program/erase endurance[4] T_L to T_H = –40°C to + 105°C T = 25°C		10,000 —	— 100,000	— —	cycles
10		Data retention[5]	t_{D_ret}	15	100	—	years

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25°C unless otherwise stated.

2 The frequency of this clock is controlled by a software setting.

3 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

4 Typical endurance for Flash was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale Semiconductor defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory*.

5 Typical data retention values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale Semiconductor defines typical data retention, please refer to Engineering Bulletin EB618/D, Typical Data Retention for Nonvolatile Memory.

2.14 USB Electricals

The USB electricals for the USBOTG module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit http://www.usb.org.

If the Freescale USBOTG implementation requires additional or deviant electrical characteristics, this space would be used to communicate that information.

3.3 64-pin QFP

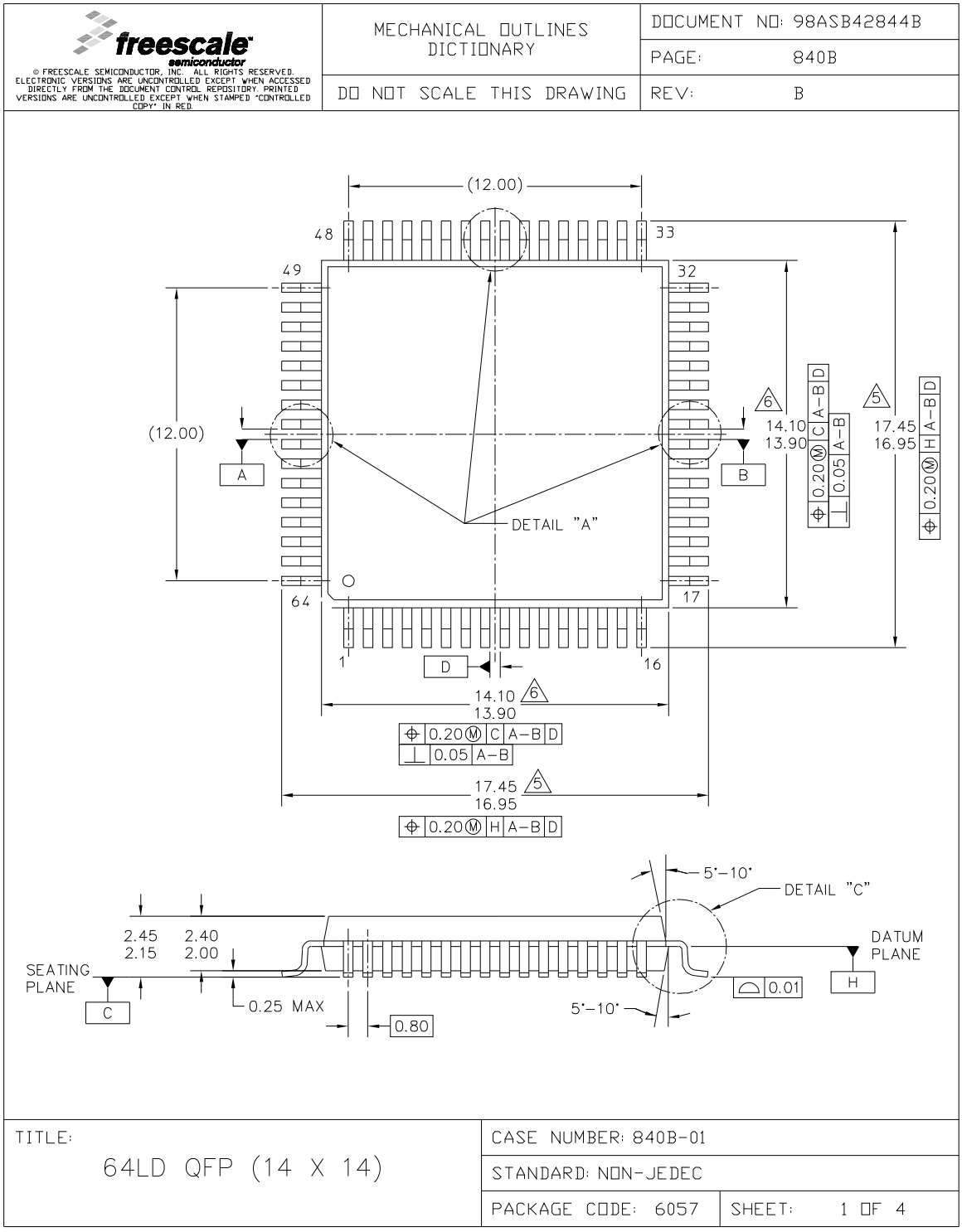


Figure 24. 64-pin QFP Diagram - I

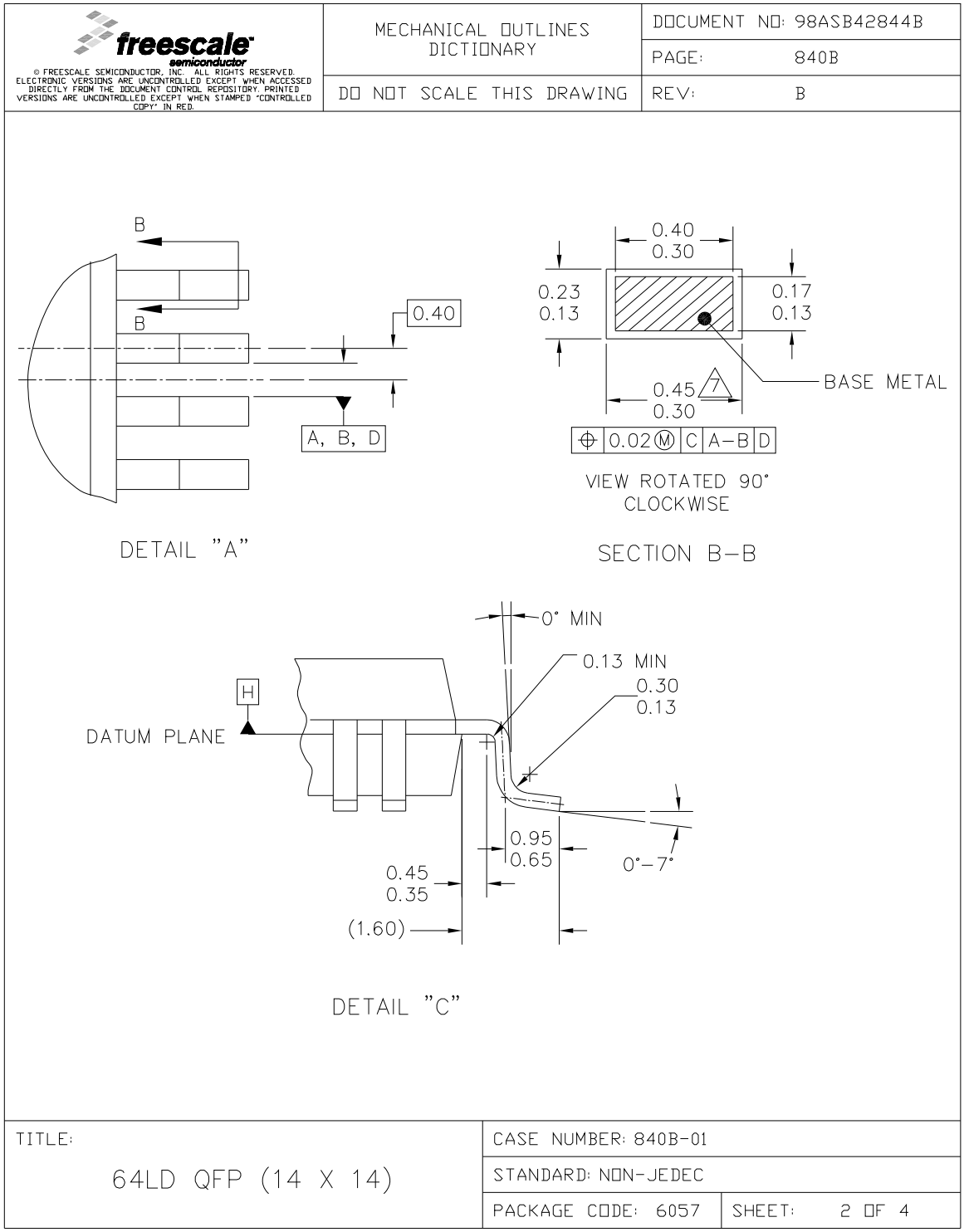


Figure 25. 64-pin QFP Diagram - II

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASB42844B
		PAGE: 840B
	DO NOT SCALE THIS DRAWING	REV: B

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE −H− IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A−B AND −D− TO BE DETERMINED AT DATUM PLANE −H−.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE −C−.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE −H−.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDICTION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

TITLE: 64LD QFP (14 X 14)	CASE NUMBER: 840B−01	
	STANDARD: NON−JEDEC	
	PACKAGE CODE: 6057	SHEET: 3 OF 4

Figure 26. 64-pin QFP Diagram - III

3.4 44-pin LQFP

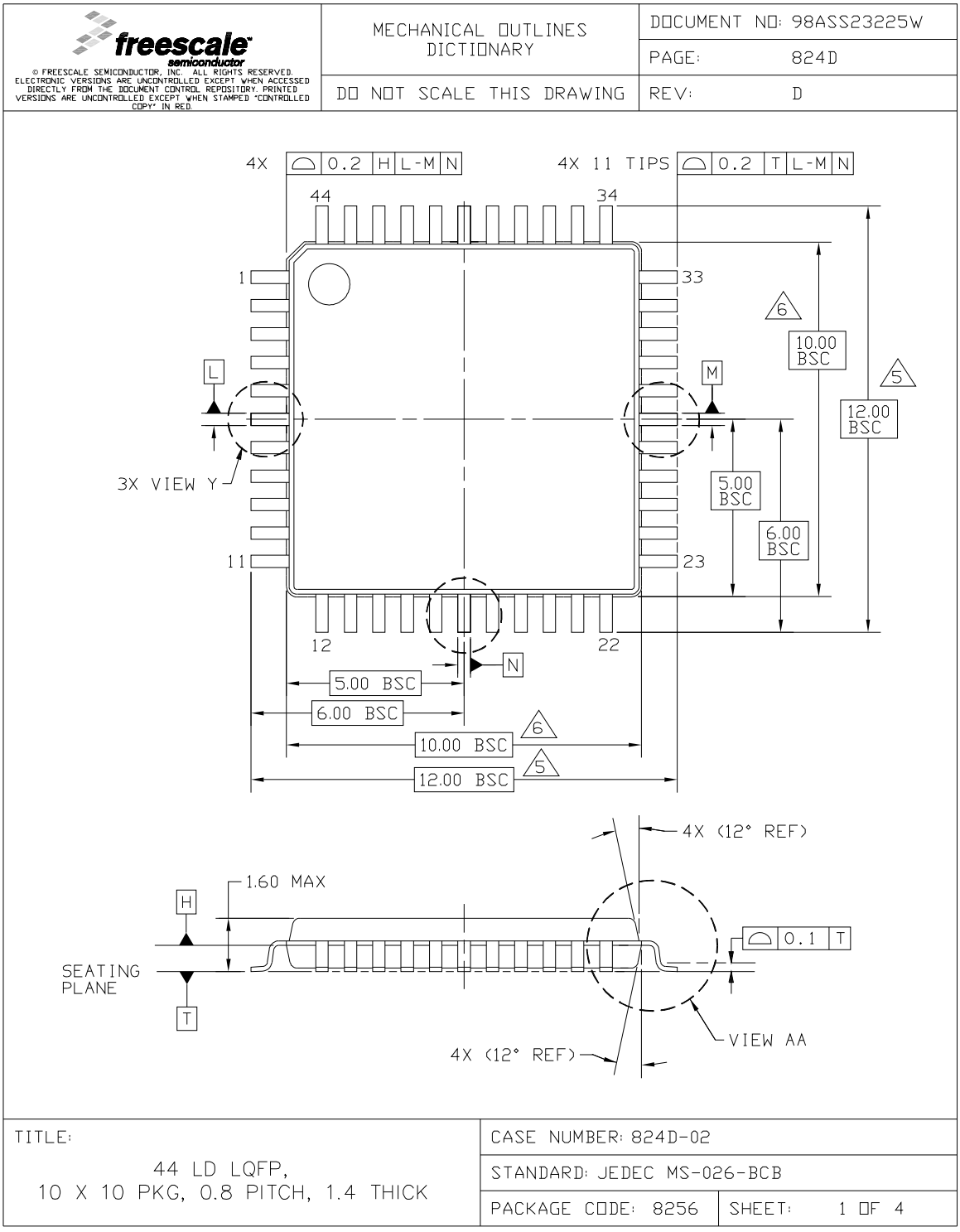


Figure 27. 44-pin LQFP Diagram - I

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23225W
		PAGE: 824D
	DO NOT SCALE THIS DRAWING	REV: D

NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DATUM PLANE H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS L, M AND N TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE T.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE DIMENSION TO EXCEED 0.53. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

TITLE: 44 LD LQFP, 10 X 10 PKG, 0.8 PITCH, 1.4 THICK	CASE NUMBER: 824D-02	
	STANDARD: JEDEC MS-026 BCB	
	PACKAGE CODE: 8256	SHEET: 3 OF 4

Figure 29. 44-pin LQFP Diagram - III

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