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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, I ² C, SCI, SPI, USB OTG
Peripherals	LVD, PWM, WDT
Number of I/O	66
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf51jm128vlkr

Table of Contents

1	MCF51JM128 Family Configurations	3
1.1	Device Comparison	3
1.2	Block Diagram	4
1.3	Features	5
1.4	Part Numbers	8
1.5	Pinouts and Packaging	10
2	Preliminary Electrical Characteristics	15
2.1	Parameter Classification	15
2.2	Absolute Maximum Ratings	15
2.3	Thermal Characteristics	16
2.4	Electrostatic Discharge (ESD) Protection Characteristics	17
2.5	DC Characteristics	18
2.6	Supply Current Characteristics	21
2.7	Analog Comparator (ACMP) Electricals	23
2.8	ADC Characteristics	23
2.9	External Oscillator (XOSC) Characteristics	26
2.10	MCG Specifications	27
2.11	AC Characteristics	28
2.12	SPI Characteristics	31
2.13	Flash Specifications	34
2.14	USB Electricals	34
2.15	EMC Performance	35
3	Mechanical Outline Drawings	36
3.1	80-pin LQFP	36
3.2	64-pin LQFP	39
3.3	64-pin QFP	42
3.4	44-pin LQFP	45
4	Revision History	48

List of Figures

Figure 1.	MCF51JM128 Block Diagram	4
Figure 2.	80-pin LQFP	10
Figure 3.	64-pin QFP and LQFP	11
Figure 4.	44-pin LQFP	12
Figure 5.	Typical Low-side Drive (sink) characteristics – High Drive (PTxDSn = 1)	20
Figure 6.	Typical Low-side Drive (sink) characteristics – Low Drive (PTxDSn = 0)	20
Figure 7.	Typical High-side Drive (source) characteristics – High Drive (PTxDSn = 1)	21
Figure 8.	Typical High-side Drive (source) characteristics – Low Drive (PTxDSn = 0)	21
Figure 9.	ADC Input Impedance Equivalency Diagram	24
Figure 10.	Reset Timing	29
Figure 11.	IRQ/KBIPx Timing	29
Figure 12.	Timer External Clock	29

Figure 13.	Timer Input Capture Pulse	30
Figure 14.	SPI Master Timing (CPHA = 0)	32
Figure 15.	SPI Master Timing (CPHA = 1)	32
Figure 16.	SPI Slave Timing (CPHA = 0)	33
Figure 17.	SPI Slave Timing (CPHA = 1)	33
Figure 18.	80-pin LQFP Diagram - I	36
Figure 19.	80-pin LQFP Diagram - II	37
Figure 20.	80-pin LQFP Diagram - III	38
Figure 21.	64-pin LQFP Diagram - I	39
Figure 22.	64-pin LQFP Diagram - II	40
Figure 23.	64-pin LQFP Diagram - III	41
Figure 24.	64-pin QFP Diagram - I	42
Figure 25.	64-pin QFP Diagram - II	43
Figure 26.	64-pin QFP Diagram - III	44
Figure 27.	44-pin LQFP Diagram - I	45
Figure 28.	44-pin LQFP Diagram - II	46
Figure 29.	44-pin LQFP Diagram - III	47

List of Tables

Table 1.	MCF51JM128 Series Device Comparison	3
Table 2.	MCF51JM128 Series Functional Units	5
Table 3.	Orderable Part Number Summary	8
Table 4.	Pin Assignments by Package and Pin Sharing Priority	12
Table 5.	Parameter Classifications	15
Table 6.	Absolute Maximum Ratings	16
Table 7.	Thermal Characteristics	16
Table 8.	ESD and Latch-up Test Conditions	17
Table 9.	ESD and Latch-Up Protection Characteristics	18
Table 10.	DC Characteristics	18
Table 11.	Supply Current Characteristics	21
Table 12.	Analog Comparator Electrical Specifications	23
Table 13.	5 Volt 12-bit ADC Operating Conditions	23
Table 14.	5 Volt 12-bit ADC Characteristics (VREFH = VDPA, VREFL = VSSA)	24
Table 15.	Oscillator Electrical Specifications (Temperature Range = –40 to 105°C Ambient)	26
Table 16.	MCG Frequency Specifications (Temperature Range = –40 to 125°C Ambient)	27
Table 17.	Control Timing	28
Table 18.	TPM Input Timing	29
Table 19.	MSCAN Wake-up Pulse Characteristics	30
Table 20.	SPI Timing	31
Table 21.	Flash Characteristics	34
Table 22.	Internal USB 3.3V Voltage Regulator Characteristics	35
Table 23.	Internal Revision History	50
Table 24.	Changes Between Revisions	51

1 MCF51JM128 Family Configurations

1.1 Device Comparison

The MCF51JM128 series consists of the devices compared in [Table 1](#).

Table 1. MCF51JM128 Series Device Comparison

Feature	MCF51JM128			MCF51JM64			MCF51JM32		
	80-pin	64-pin	44-pin	80-pin	64-pin	44-pin	80-pin	64-pin	44-pin
Flash memory size (KB)	128			64			32		
RAM size (KB)	16			16			16		
V1 ColdFire core with BDM (background debug module)	Yes								
ACMP (analog comparator)	Yes								
ADC channels (12-bit)	12		8	12		8	12		8
CAN (controller area network)	Yes	Yes	No	Yes	Yes	No	Yes	Yes	No
RNGA + CAU	Yes ¹								
CMT (carrier modulator timer)	Yes								
COP (computer operating properly)	Yes								
IIC1 (inter-integrated circuit)	Yes								
IIC2	Yes	No		Yes	No		Yes	No	
IRQ (interrupt request input)	Yes								
KBI (keyboard interrupts)	8	8	6	8	8	6	8	8	6
LVD (low-voltage detector)	Yes								
MCG (multipurpose clock generator)	Yes								
Port I/O ²	66	51	33	66	51	33	66	51	33
RGPIO (rapid general-purpose I/O)	16	6	0	16	6	0	16	6	0
RTC (real-time counter)	Yes								
SCI1 (serial communications interface)	Yes								
SCI2	Yes								
SPI1 (serial peripheral interface)	Yes								
SPI2	Yes								
TPM1 (timer/pulse-width modulator) channels	6	6	4	6	6	4	6	6	4
TPM2 channels	2								
USBOTG (USB On-The-Go dual-role controller)	Yes								
XOSC (crystal oscillator)	Yes								

¹ Only existed on special part number

² Up to 16 pins on Ports A, H, and J are shared with the ColdFire Rapid GPIO module.

1.2 Block Diagram

Figure 1 shows the connections between the MCF51JM128 series pins and modules.

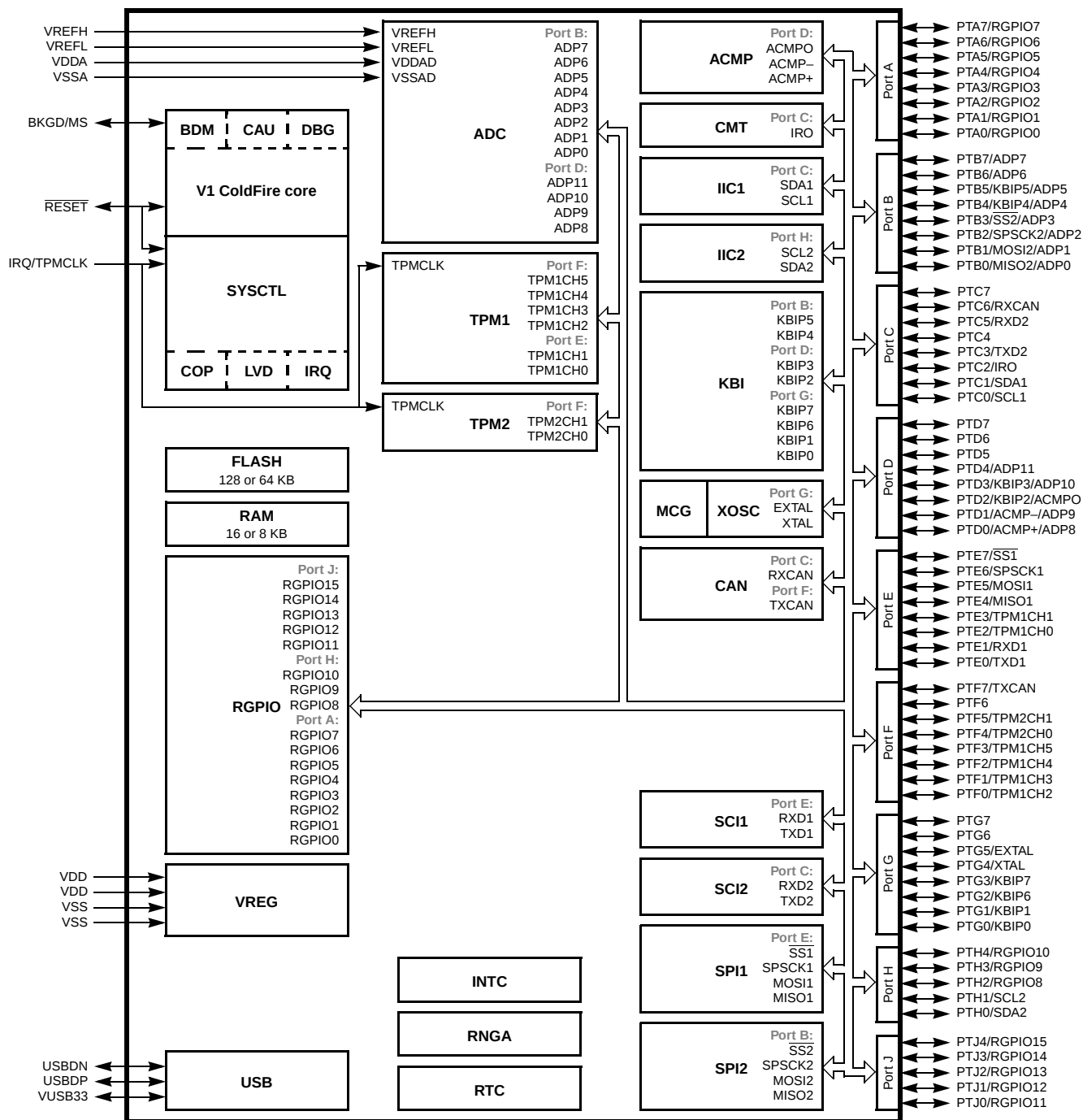


Figure 1. MCF51JM128 Block Diagram

Table 6. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	−0.3 to + 5.8	V
Input voltage	V_{In}	− 0.3 to $V_{DD} + 0.3$	V
Instantaneous maximum current Single pin limit (applies to all port pins) ^{1, 2, 3}	I_D	± 25	mA
Maximum current into V_{DD}	I_{DD}	120	mA
Storage temperature	T_{stg}	−55 to +150	°C
Maximum junction temperature	T_J	150	°C

¹ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

² All functional non-supply pins are internally clamped to V_{SS} and V_{DD} .

³ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load shunt current is greater than maximum injection current. This is the greatest risk when the MCU is not consuming power. Examples: if no system clock is present or if the clock rate is low, which would reduce overall power consumption.

2.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} is small.

Table 7. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	−40 to +105	°C
Thermal resistance ^{1,2,3,4}			
80-pin LQFP			
	1s	52	
	2s2p	40	
64-pin LQFP			
	1s	65	
	2s2p	47	
64-pin QFP			
	1s	54	
	2s2p	40	
44-pin LQFP			
	1s	69	
	2s2p	48	

¹ Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

² Junction to Ambient Natural Convection

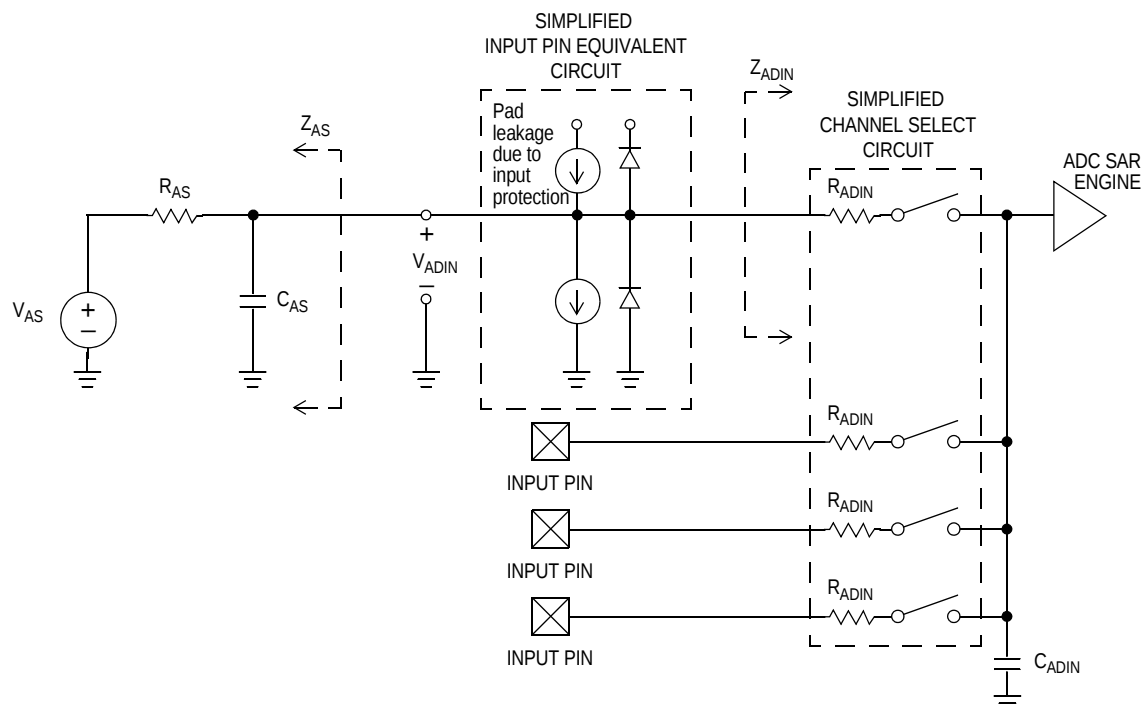


Figure 9. ADC Input Impedance Equivalency Diagram

Table 14. 5 Volt 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Characteristic	Conditions	C	Symb	Min	Typ ¹	Max	Unit	Comment
Supply Current ADLPC=1 ADLSMP=1 ADCO=1		T	I_{DDAD}	—	133	—	μA	
Supply Current ADLPC=1 ADLSMP=0 ADCO=1		T	I_{DDAD}	—	218	—	μA	
Supply Current ADLPC=0 ADLSMP=1 ADCO=1		T	I_{DDAD}	—	327	—	μA	
Supply Current ADLPC=0 ADLSMP=0 ADCO=1		P	I_{DDAD}	—	0.582	1	mA	
Supply Current	Stop, Reset, Module Off		I_{DDAD}	—	0.011	1	μA	
ADC Asynchronous Clock Source	High Speed (ADLPC=0)	T	f_{ADACK}	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
	Low Power (ADLPC=1)			1.25	2	3.3		

2.10 MCG Specifications

Table 16. MCG Frequency Specifications (Temperature Range = –40 to 125°C Ambient)

Num	C	Rating		Symbol	Min	Typical ¹	Max	Unit
1	P	Internal reference frequency - factory trimmed at V _{DD} = 5 V and temperature = 25 °C		f _{int_ft}	—	32.768	—	kHz
2	P	Average internal reference frequency – untrimmed		f _{int_ut}	31.25	—	39.0625	kHz
3	T	Internal reference startup time		t _{irefst}	—	60	100	μs
4	P	DCO output frequency range - untrimmed ²	Low range (DRS=00)	f _{dco_ut}	16	—	20	MHz
	P		Mid range (DRS=01)		32	—	40	
	P		High range (DRS=10)		48	—	60	
5	P	DCO output frequency ² Reference = 32768Hz and DMX32 = 1	Low range (DRS=00)	f _{dco_DMx32}	—	19.92	—	MHz
	P		Mid range (DRS=01)		—	39.85	—	
	P		High range (DRS=10)		—	59.77	—	
6	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		Δf _{dco_res_t}	—	±0.1	±0.2	%f _{dco}
7	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		Δf _{dco_res_t}	—	±0.2	±0.4	%f _{dco}
8	D	Total deviation of trimmed DCO output frequency over voltage and temperature		Δf _{dco_t}	—	0.5 –1.0	±2	%f _{dco}
9	D	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 – 70 °C		Δf _{dco_t}	—	±0.5	±1	%f _{dco}
10	D	FLL acquisition time ³		t _{fill_acquire}	—	—	1	ms
11	D	PLL acquisition time ⁴		t _{pll_acquire}	—	—	1	ms
12	D	Long term Jitter of DCO output clock (averaged over 2ms interval) ⁵		C _{jitter}	—	0.02	0.2	%f _{dco}
13	D	VCO operating frequency		f _{vco}	7.0	—	55.0	MHz
14	D	Jitter of PLL output clock measured over 625 ns ⁶		f _{pll_jitter_625ns}	—	0.566 ⁵	—	%f _{pll}
15	D	Lock entry frequency tolerance ⁷		D _{lock}	±1.49	—	±2.98	%
16	D	Lock exit frequency tolerance ⁸		D _{unl}	±4.47	—	±5.97	%
17	D	Lock time — FLL		t _{fill_lock}	—	—	t _{fill_acquire} + 1075(1/f _{int_t})	s
18	D	Lock time — PLL		t _{pll_lock}	—	—	t _{pll_acquire} + 1075(1/f _{pll_ref})	s
19	D	Loss of external clock minimum frequency – RANGE = 0		f _{loc_low}	(3/5) × f _{int}	—	—	kHz

¹ Data in Typical column was characterized at 5.0 V, 25C or is typical recommended value

² The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

³ This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

⁴ This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

Preliminary Electrical Characteristics

- ⁵ Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS} . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.
- ⁶ 625 ns represents 5 time quanta for CAN applications, under worst case conditions of 8 MHz CAN bus clock, 1 Mbps CAN bus speed, and 8 time quanta per bit for bit time settings. 5 time quanta is the minimum time between a synchronization edge and the sample point of a bit using 8 time quanta per bit.
- ⁷ Below D_{lock} minimum, the MCG is guaranteed to enter lock. Above D_{lock} maximum, the MCG will not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.
- ⁸ Below D_{unl} minimum, the MCG will not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.

2.11 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

2.11.1 Control Timing

Table 17. Control Timing

Num	C	Parameter	Symbol	Min	Typ ¹	Max	Unit
1		Bus frequency ($t_{cyc} = 1/f_{BUS}$)	f_{BUS}	dc	—	24	MHz
2		Internal low-power oscillator period	t_{LPO}	700		1300	μs
3		External reset pulse width ² ($t_{cyc} = 1/f_{Self_reset}$)	t_{extrst}	100		—	ns
4		Reset low drive	t_{rstdrv}	$66 \times t_{cyc}$		—	ns
5		Active background debug mode latch setup time	t_{MSSU}	500		—	ns
6		Active background debug mode latch hold time	t_{MSH}	100		—	ns
7		IRQ pulse width Asynchronous path ² Synchronous path ³	t_{ILIH}, t_{IHIL}	100 $1.5 \times t_{cyc}$	—	—	ns
8		KBIPx pulse width Asynchronous path ² Synchronous path ³	t_{ILIH}, t_{IHIL}	100 $1.5 \times t_{cyc}$	—	—	ns
9		Port rise and fall time (load = 50 pF) ⁴ Slew rate control disabled (PTxSE = 0) High drive Slew rate control enabled (PTxSE = 1) High drive Slew rate control disabled (PTxSE = 0) Low drive Slew rate control enabled (PTxSE = 1) Low drive	t_{Rise}, t_{Fall}	— —	11 35 40 75		ns

¹ Typical values are based on characterization data at $V_{DD} = 5.0V$, 25°C unless otherwise stated.

² This is the shortest pulse guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

³ This is the minimum pulse width guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

⁴ Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 105°C.

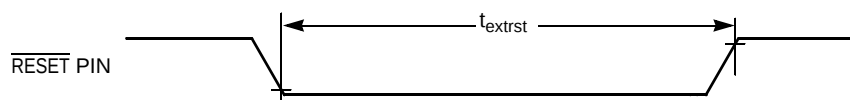


Figure 10. Reset Timing

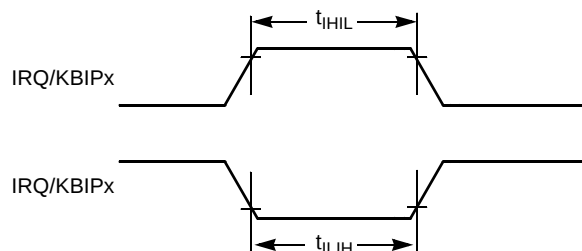


Figure 11. IRQ/KBIPx Timing

2.11.2 Timer/PWM (TPM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 18. TPM Input Timing

NUM	C	Function	Symbol	Min	Max	Unit
1	—	External clock frequency	f_{TPMext}	dc	$f_{\text{Bus}}/4$	MHZ
2	—	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

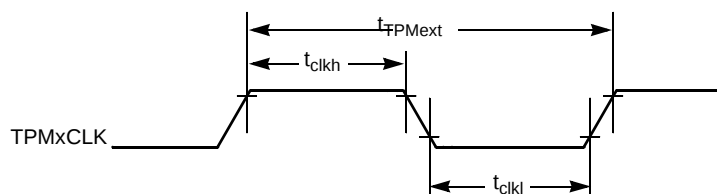


Figure 12. Timer External Clock

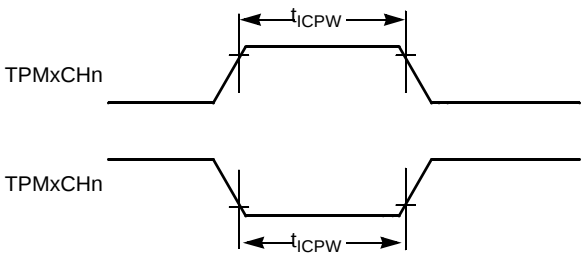


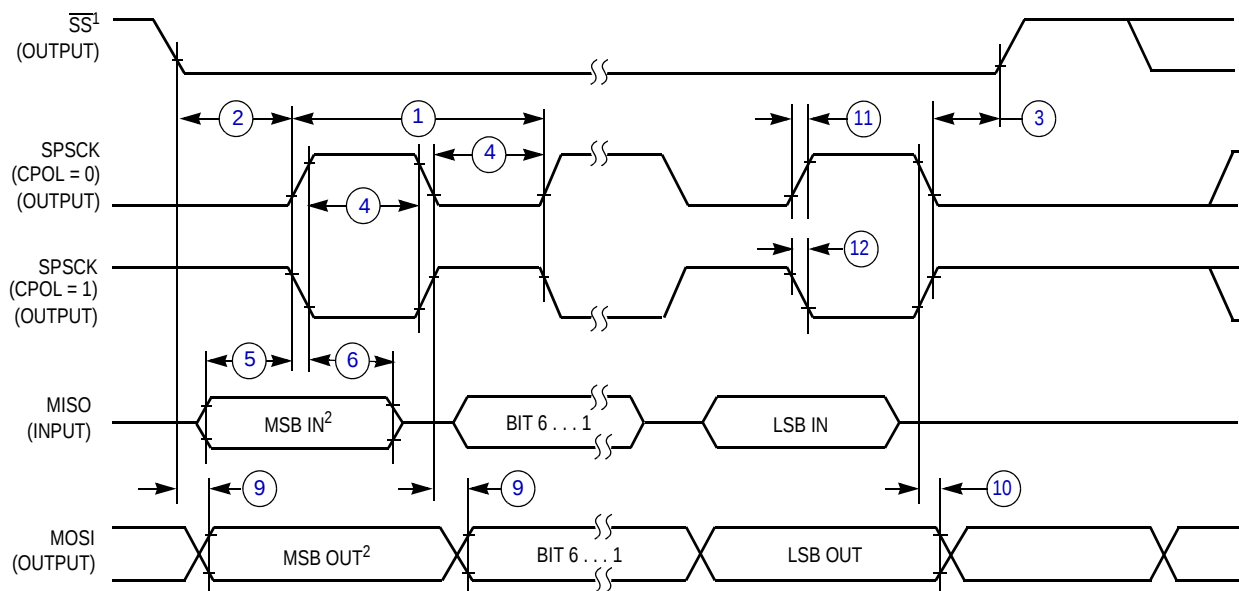
Figure 13. Timer Input Capture Pulse

2.11.3 MSCAN

Table 19. MSCAN Wake-up Pulse Characteristics

Num	C	Parameter	Symbol	Min	Typ ¹	Max	Unit
1	D	MSCAN Wake-up dominant pulse filtered	t_{WUP}			2	μs
2	D	MSCAN Wake-up dominant pulse pass	t_{WUP}	5		5	μs

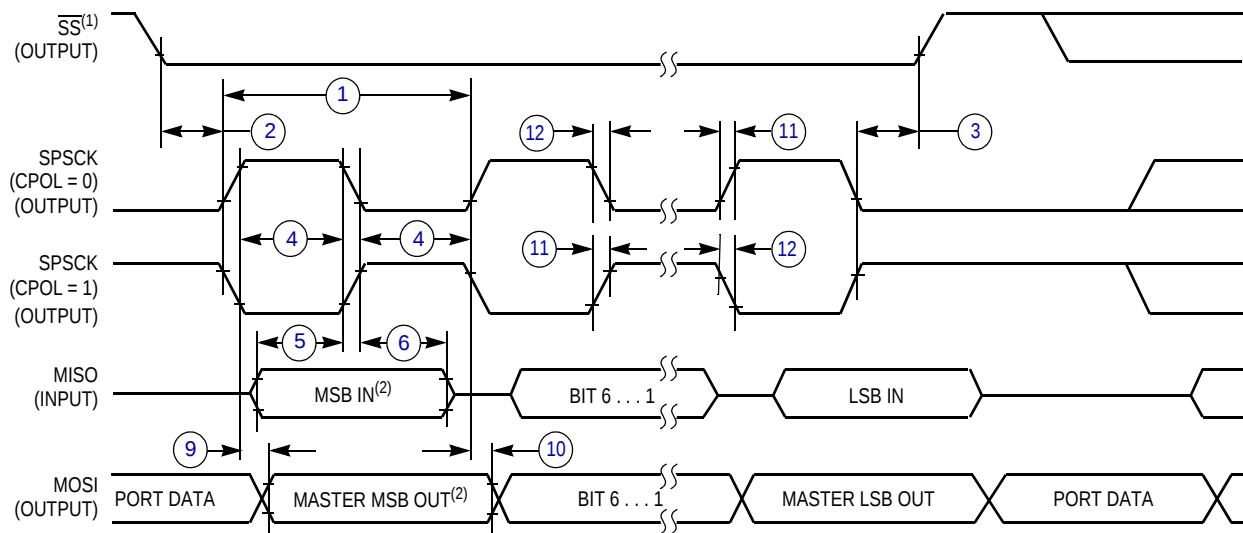
¹ Typical values are based on characterization data at $V_{DD} = 5.0\text{V}$, 25°C unless otherwise stated.



NOTES:

1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 14. SPI Master Timing (CPHA = 0)



NOTES:

1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 15. SPI Master Timing (CPHA = 1)

2.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply.

Table 21. Flash Characteristics

Num	C	Characteristic	Symbol	Min	Typ ¹	Max	Unit
1		Supply voltage for program/erase	$V_{\text{prog/erase}}$	2.7		5.5	V
2		Supply voltage for read operation	V_{Read}	2.7		5.5	V
3		Internal FCLK frequency ²	f_{FCLK}	150		200	kHz
4		Internal FCLK period (1/FCLK)	t_{Fcyc}	5		6.67	μs
5		Byte program time (random location) ⁽²⁾	t_{prog}	9			t_{Fcyc}
6		Byte program time (burst mode) ⁽²⁾	t_{Burst}	4			t_{Fcyc}
7		Page erase time ³	t_{Page}	4000			t_{Fcyc}
8		Mass erase time ⁽²⁾	t_{Mass}	20,000			t_{Fcyc}
9	C	Program/erase endurance ⁴ T_L to $T_H = -40^\circ\text{C}$ to $+105^\circ\text{C}$ $T = 25^\circ\text{C}$		10,000 —	— 100,000	— —	cycles
10		Data retention ⁵	$t_{\text{D_ret}}$	15	100	—	years

¹ Typical values are based on characterization data at $V_{DD} = 5.0\text{ V}$, 25°C unless otherwise stated.

² The frequency of this clock is controlled by a software setting.

³ These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

⁴ Typical endurance for Flash was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale Semiconductor defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory*.

⁵ Typical data retention values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale Semiconductor defines typical data retention, please refer to Engineering Bulletin EB618/D, *Typical Data Retention for Nonvolatile Memory*.

2.14 USB Electricals

The USB electricals for the USBOTG module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit <http://www.usb.org>.

If the Freescale USBOTG implementation requires additional or deviant electrical characteristics, this space would be used to communicate that information.

3 Mechanical Outline Drawings

3.1 80-pin LQFP

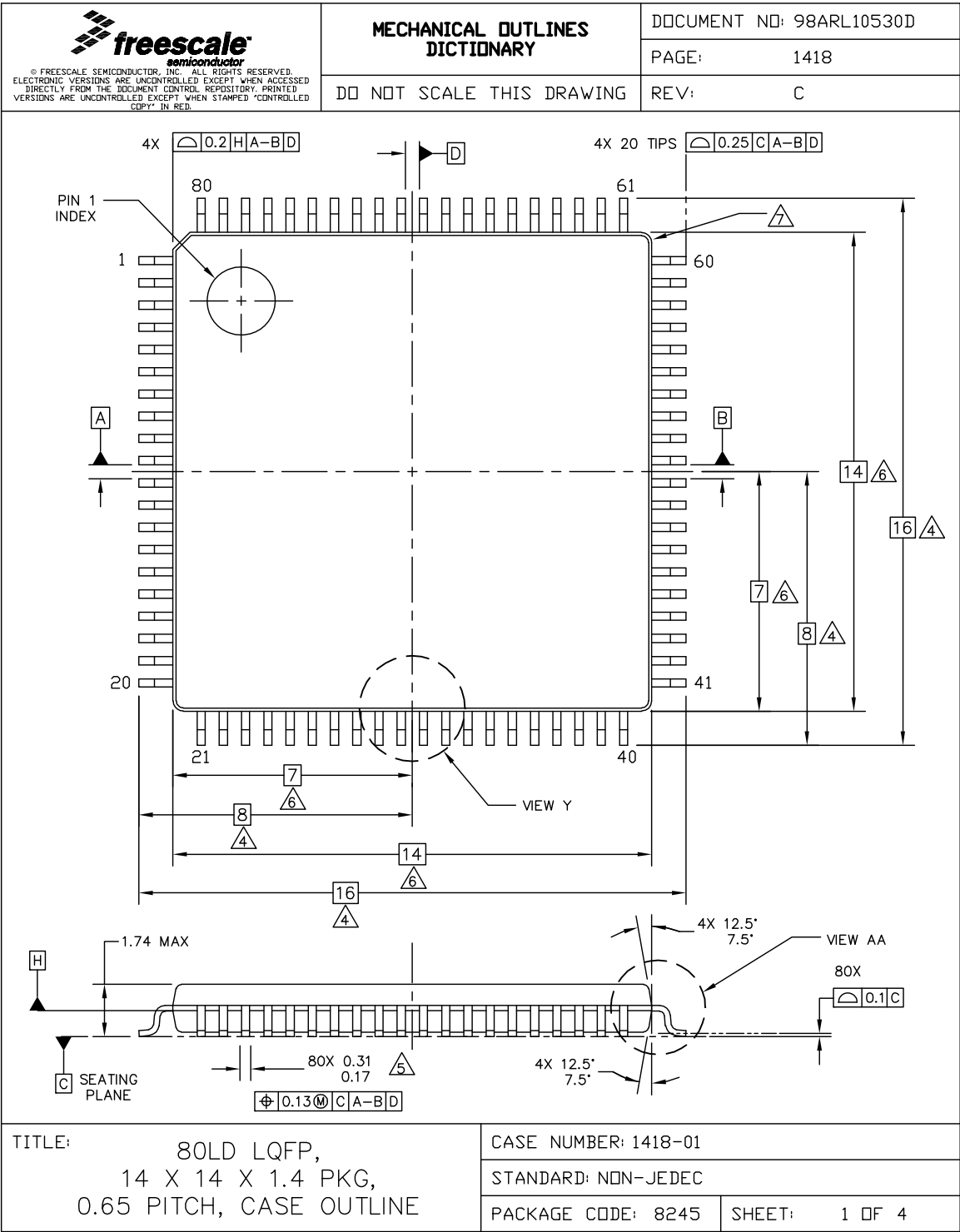


Figure 18. 80-pin LQFP Diagram - I

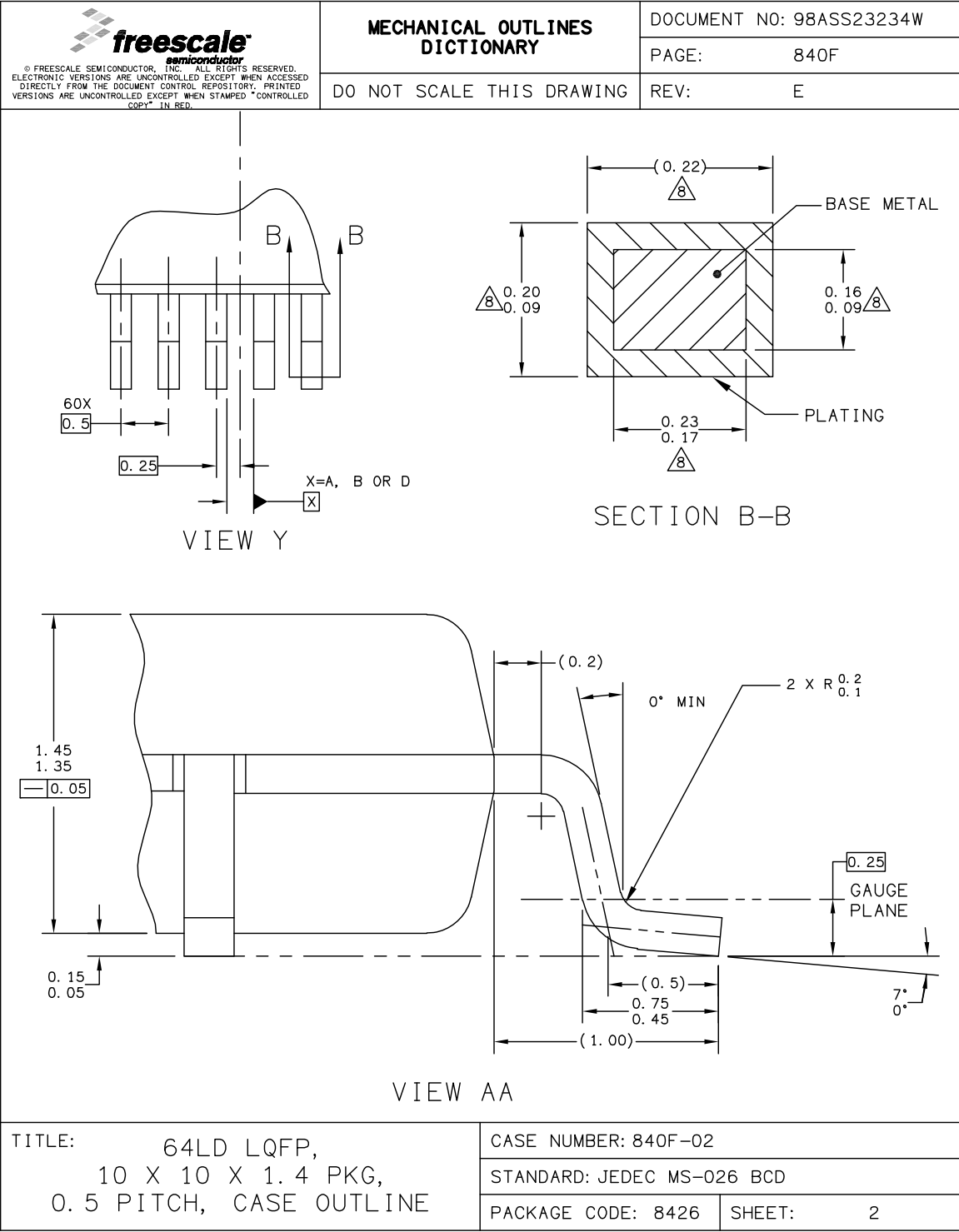


Figure 22. 64-pin LQFP Diagram - II

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			PAGE:	840F
	DO NOT SCALE THIS DRAWING		REV:	E
NOTES:				
1. DIMENSIONS ARE IN MILLIMETERS.				
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.				
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.				
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.				
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.				
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.				
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.				
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.				

Figure 23. 64-pin LQFP Diagram - III

3.3 64-pin QFP

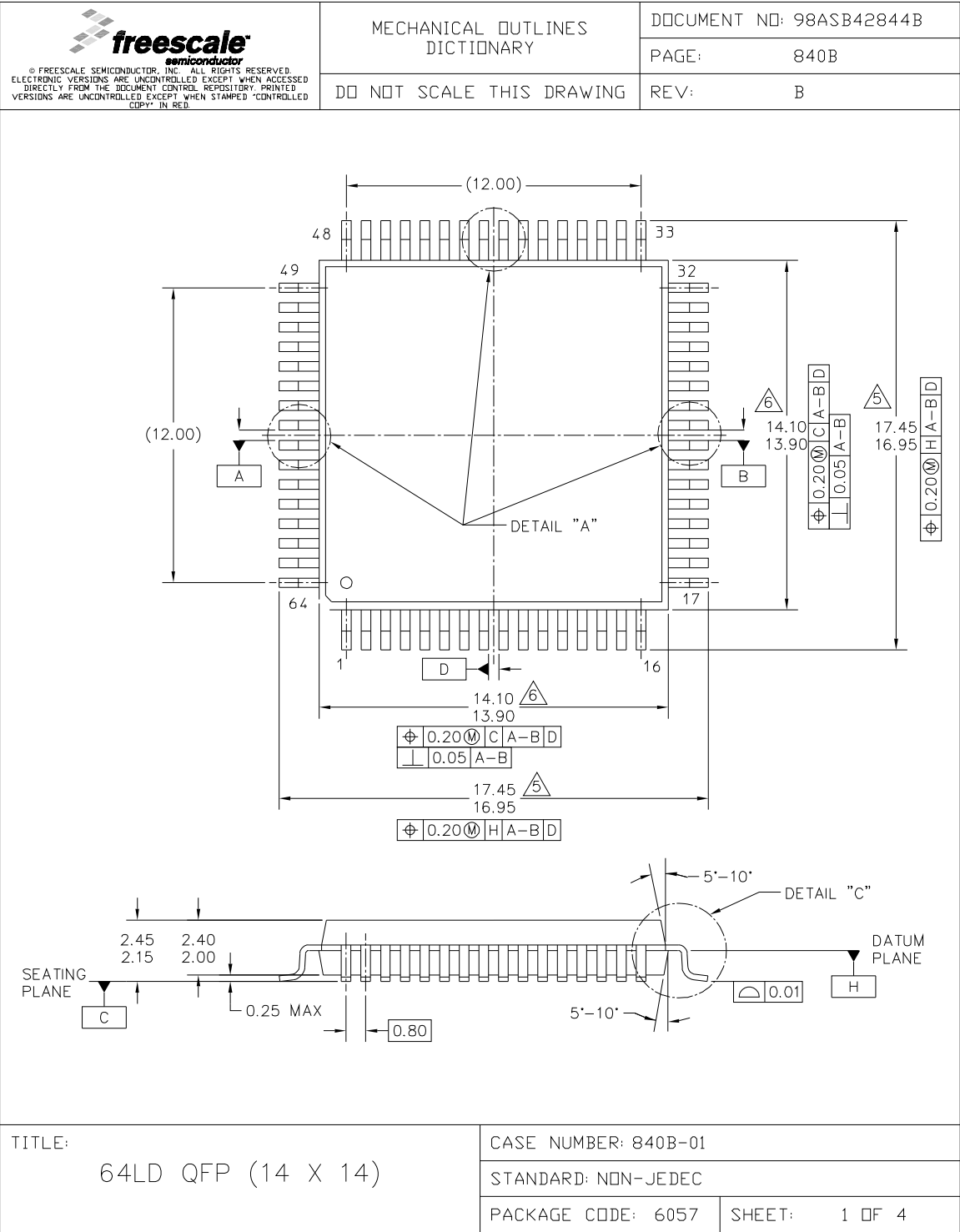


Figure 24. 64-pin QFP Diagram - I

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	DO NOT SCALE THIS DRAWING	PAGE:	840B
		REV:	B

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

2. CONTROLLING DIMENSION: MILLIMETER.

3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.

4. DATUMS A-B AND -D- TO BE DETERMINED AT DATUM PLANE -H-.

5.

DIMENSIONS TO BE DETERMINED AT SEATING PLANE -C-.

6.

DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.

7.

DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDICTION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

TITLE: 64LD QFP (14 X 14)	CASE NUMBER: 840B-01		
	STANDARD: NON-JEDEC		
	PACKAGE CODE: 6057	SHEET:	3 OF 4

Figure 26. 64-pin QFP Diagram - III

3.4 44-pin LQFP

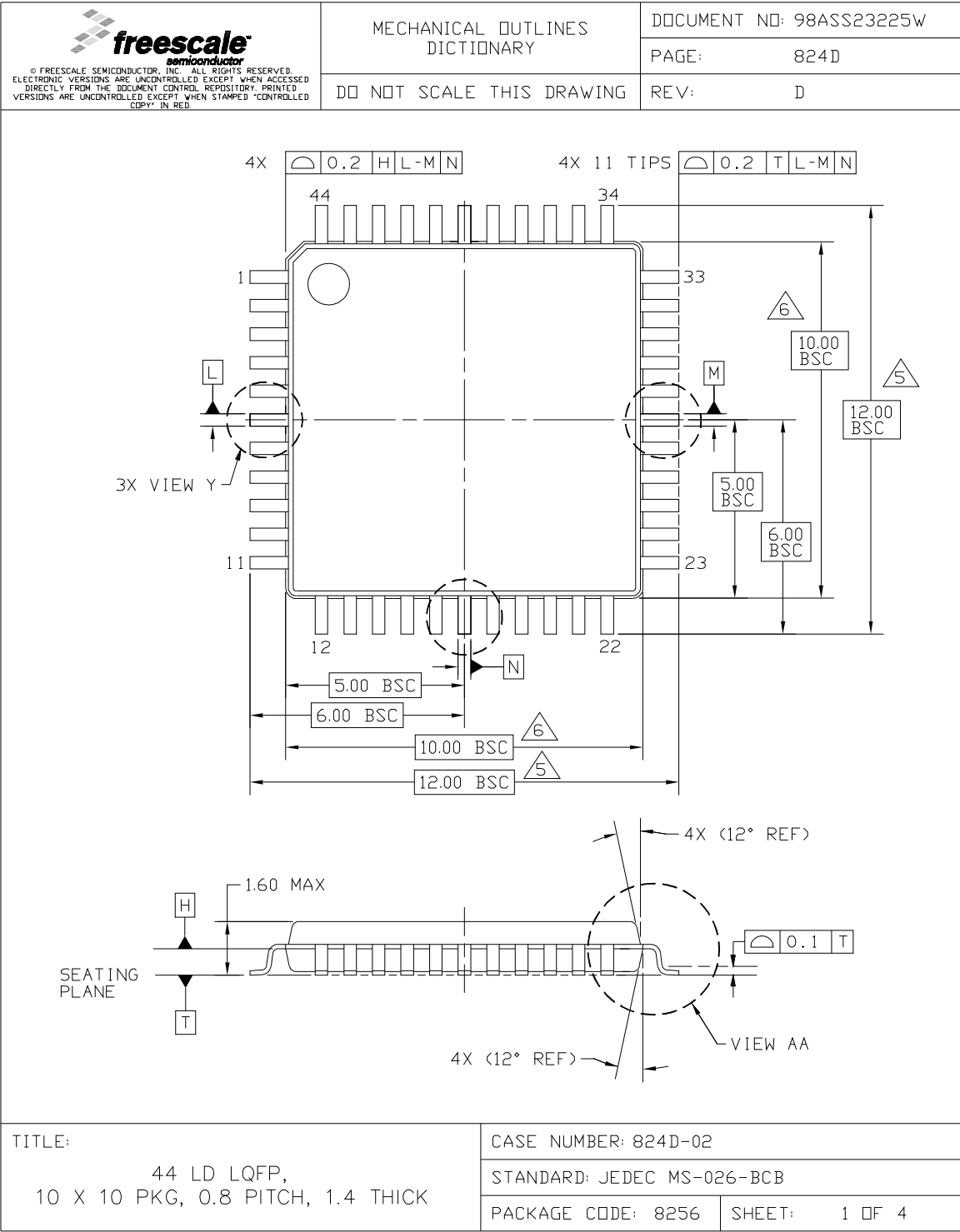


Figure 27. 44-pin LQFP Diagram - I

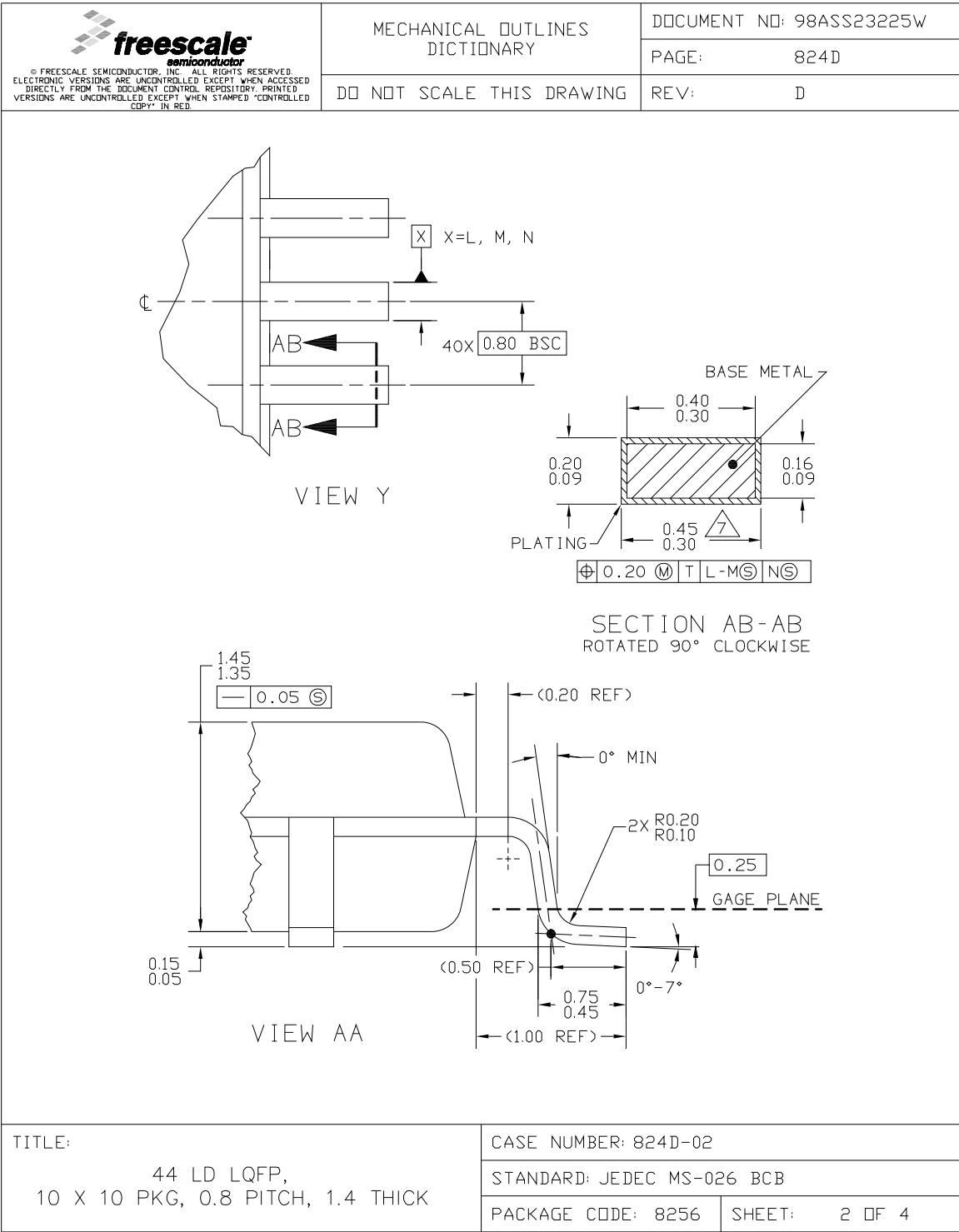


Figure 28. 44-pin LQFP Diagram - II

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		PAGE:	824D
	DO NOT SCALE THIS DRAWING	REV:	D
NOTES: 1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M-1994. 2. CONTROLLING DIMENSION: MILLIMETER 3. DATUM PLANE H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE. 4. DATUMS L, M AND N TO BE DETERMINED AT DATUM PLANE H. 5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE T. 6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H. 7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE DIMENSION TO EXCEED 0.53. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.			
TITLE:		CASE NUMBER: 824D-02	
44 LD LQFP, 10 X 10 PKG, 0.8 PITCH, 1.4 THICK		STANDARD: JEDEC MS-026 BCB	
		PACKAGE CODE: 8256	SHEET: 3 OF 4

Figure 29. 44-pin LQFP Diagram - III

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