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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, I²C, SCI, SPI, USB OTG
Peripherals	LVD, PWM, WDT
Number of I/O	51
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf51jm32vlh

1.3 Features

Table 2 describes the functional units of the MCF51JM128 series.

Table 2. MCF51JM128 Series Functional Units

Unit	Function
CF1CORE (V1 ColdFire core)	Executes programs and interrupt handlers
BDM (background debug module)	Provides a single-pin debugging interface (part of the V1 ColdFire core)
DBG (debug)	Provides debugging and emulation capabilities (part of the V1 ColdFire core)
SYSCTL (system control)	Provides LVD, COP, external interrupt request, and so on
FLASH (flash memory)	Provides storage for program code and constants
RAM (random-access memory)	Provides storage for program code, constants, and variables
RGPIO (rapid general-purpose input/output)	Allows I/O port access at CPU clock speeds
VREG (voltage regulator)	Controls power management throughout the device
USBOTG (USB On-The-Go)	Supports the USB On-The-Go dual-role controller
ADC (analog-to-digital converter)	Measures analog voltages at up to 12 bits of resolution
TPM1, TPM2 (timer/pulse-width modulators)	Provide a variety of timing-based features
CF1_INTC (interrupt controller)	Controls and prioritizes all device interrupts
CAU (cryptographic acceleration unit)	Co-processor support for DES, 3DES, AES, MD5, and SHA-1
RNGA (random number generator accelerator)	32-bit random number generator that complies with FIPS-140
RTC (real-time counter)	Provides a constant-time base with optional interrupt
ACMP (analog comparator)	Compares two analog inputs
CMT (carrier modulator timer)	Infrared output used for the Remote Controller
IIC1, IIC2 (inter-integrated circuits)	Supports the standard IIC communications protocol
KBI (keyboard interrupt)	Provides pin interrupt capabilities
MCG (multipurpose clock generator)	Provides clocking options for the device, including a phase-locked loop (PLL) and frequency-locked loop (FLL) for multiplying slower reference clock sources
XOSC (crystal oscillator)	Supports low/high range crystals
CAN (controller area network)	Supports standard CAN communications protocol
SCI1, SCI2 (serial communications interfaces)	Serial communications UARTs that can support RS-232 and LIN protocols
SPI1, SPI2 (serial peripheral interfaces)	Provide a 4-pin synchronous serial interface

1.3.1 Feature List

- 32-bit Version 1 ColdFire Central Processor Unit (CPU)
  - Up to 50.33 MHz at 2.7 V – 5.5 V
  - Performance (Dhrystone 2.1):
    - 0.94 Dhrystone 2.1 MIPS per MHz when running from internal RAM
    - 0.76 Dhrystone 2.1 MIPS per MHz when running from flash
  - Implements Instruction Set Revision C (ISA_C)
  - Supports up to 30 peripheral interrupt requests and seven software interrupts
- On-chip memory
  - Up to 128 KB Flash memory with read/program/erase over full operating voltage and temperature range
  - Up to 16 KB static random access memory (RAM)
  - Security circuitry to prevent unauthorized access to RAM and flash contents
- Power-saving modes
  - Two low-power stop plus wait modes
  - Peripheral clock enable register can disable clocks to unused modules, thereby reducing currents; this behavior allows clocks to remain enabled to specific perhipherals in Stop3 mode
  - Very lower power real-time counter for use in run, wait, and stop modes with internal and external clock sources
- Four Clock Source Options
  - Oscillator (XOSC) — Loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - FLL/PLL controlled by internal or external reference
  - Trimmable internal reference allows 0.2% resolution and 2% deviation
- System protection features
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock
  - Low-voltage detection with reset or interrupt; selectable trip points
  - Illegal opcode and illegal address detection with programmable reset or exception response
  - Flash block protection
- Debug support
  - Single-wire Background debug interface
  - 4 Program Counters plus two address (optional data) breakpoint registers with programmable 1- or 2-level trigger response
  - 64-entry processor status and debug data trace buffer with programmable start/stop conditions
- Universal Serial Bus (USB) On-The-Go dual-role controller
  - Full-speed USB device controller
    - Fully compliant with USB specification 1.1 and 2.0
    - 16 bidirectional endpoints, with double buffering to provide the maximum throughput
    - Supports control, bulk, interrupt, and isochronous endpoints
    - Supports bus-powered capability with low-power consumption
  - Full-speed / low-speed host controller
    - Host mode allows control, bulk, interrupt, and isochronous transfers
  - OTG protocol logic
  - On-chip USB transceiver
  - On-chip 3.3 V USB regulator and pull-up resistors save system cost

- Controller area network (MSCAN)
  - Implementation of the CAN protocol — Version 2.0A/B
  - Five receive buffers with FIFO storage scheme
  - Three transmit buffers with internal prioritization using a “local priority” concept
  - Flexible maskable identifier filter programmable as 2x32-bit, 4x16-bit, or 8x8-bit
  - Programmable wakeup functionality with integrated low-pass filter
  - Programmable loopback mode supports self-test operation
  - Programmable bus-off recovery functionality
  - Internal timer for time-stamping of received and transmitted messages
- Cryptographic acceleration unit (CAU)
  - Co-processor support of DES, 3DES, AES, MD5, and SHA-1
- Random number generator accelerator (RNGA)
  - 32-bit random number generator that complies with FIPS-140
- Analog-to-digital converter (ADC)
  - 12-channel, 12-bit resolution
  - Output formatted in 12-, 10-, or 8-bit right-justified format
  - Single or continuous conversion, and selectable asynchronous hardware conversion trigger
  - Operation in Stop3 mode
  - Automatic compare function
  - Internal temperature sensor
- Analog comparators (ACMP)
  - Selectable interrupt on rising edge, falling edge, or either rising or falling edges of comparator output
  - Option to compare to fixed internal bandgap reference voltage
  - Option to route output to TPM module
  - Operation in Stop3 mode
- Inter-integrated circuit (IIC)
  - Up to 100 kbps with maximum bus loading
  - Multi-master operation
  - Programmable slave address
  - Supports broadcast mode and 10-bit address extension
- Serial communications interfaces (SCI)
  - Two SCIs with full-duplex, non-return-to-zero (NRZ) format
  - LIN master extended break generation
  - LIN slave extended break detection
  - Programmable 8-bit or 9-bit character length
  - Wake up on active edge
- Serial peripheral interfaces (SPI)
  - Two serial peripheral interfaces with full-duplex or single-wire bidirectional
  - Double-buffered transmit and receive
  - Programmable transmit bit rate, phase, polarity, and Slave Select output
  - MSB-first or LSB-first shifting
- Timer/pulse width modulator (TPM)
  - 16-bit free-running or modulo up/down count operation
  - Up to eight channels, where each channel can be an input capture, output compare, or edge-aligned PWM
  - One interrupt per channel plus terminal count interrupt

Table 3. Orderable Part Number Summary (continued)

MCF51JM64EVLD	MCF51JM64 ColdFire Microcontroller with CAU and RNGA Enabled	64 / 16	44 LQFP	–40 to +105 °C
MCF51JM64VLD	MCF51JM64 ColdFire Microcontroller	64 / 16	44 LQFP	–40 to +105 °C
MCF51JM32EVLK	MCF51JM32 ColdFire Microcontroller with CAU and RNGA Enabled	32 / 16	80 LQFP	–40 to +105 °C
MCF51JM32VLK	MCF51JM32 ColdFire Microcontroller	32 / 16	80 LQFP	–40 to +105 °C
MCF51JM32EVLH	MCF51JM32 ColdFire Microcontroller with CAU and RNGA Enabled	32 / 16	64 LQFP	–40 to +105 °C
MCF51JM32VLH	MCF51JM32 ColdFire Microcontroller	32 / 16	64 LQFP	–40 to +105 °C
MCF51JM32EVQH	MCF51JM32 ColdFire Microcontroller with CAU and RNGA Enabled	32 / 16	64 QFP	–40 to +105 °C
MCF51JM32VQH	MCF51JM32 ColdFire Microcontroller	32 / 16	64 QFP	–40 to +105 °C
MCF51JM32EVLD	MCF51JM32 ColdFire Microcontroller with CAU and RNGA Enabled	32 / 16	44 LQFP	–40 to +105 °C
MCF51JM32VLD	MCF51JM32 ColdFire Microcontroller	32 / 16	44 LQFP	–40 to +105 °C

Table 4. Pin Assignments by Package and Pin Sharing Priority (continued)

Pin Number			<-- Lowest **Priority** --> Highest		
80	**64**	**44**	**Port Pin**	**Alt 1**	**Alt 2**
49	41	—	PTB7	ADP7	—
50	42	29	PTD0	ADP8	ACMP+
51	43	30	PTD1	ADP9	ACMP–
52	44	31	—	—	VDDA
53	45		—	—	VREFH
54	46	32	—	—	VREFL
55	47		—	—	VSSA
56	48	33	PTD2	KBIP2	ACMPO
57	—	—	PTJ0	RGPIO11	—
58	—	—	PTJ1	RGPIO12	—
59	—	—	PTJ2	RGPIO13	—
60	—	—	PTJ3	RGPIO14	—
61	—	—	PTJ4	RGPIO15	—
62	49	—	PTD3	KBIP3	ADP10
63	50	—	PTD4	ADP11	—
64	51	—	PTD5	—	—
65	52	—	PTD6	—	—
66	53	—	PTD7	—	—
67	54	34	PTG2	KBIP6	—
68	55	35	PTG3	KBIP7	—
69	56	36	—	BKGD	MS
70	57	37	PTG4	XTAL	
71	58	38	PTG5	EXTAL	
72	59	39	—	—	VSS
73	—	—	—	—	VDD
74	—	—	PTG6	—	—
75	—	—	PTG7	—	—
76	60	40	PTC0	SCL1	—
77	61	41	PTC1	SDA1	—
78	62	42	PTC2	IRO	—
79	63	43	PTC3	TXD2	—
80	64	44	PTC5	RXD2	—

2 Preliminary Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MCF51JM128 microcontroller, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 5. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled C in the parameter tables where appropriate.

2.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 6 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, V_{SS} or V_{DD}).

Table 9. ESD and Latch-Up Protection Characteristics

Num	Rating	Symbol	Min	Max	Unit
1	Human Body Model (HBM)	V_{HBM}	+/– 2000	—	V
2	Charge Device Model (CDM)	V_{CDM}	+/– 500	—	V
3	Latch-up Current at T_A = 105°C	I_{LAT}	+/– 100	—	mA

2.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 10. DC Characteristics

Num	C	Parameter	Symbol	Min	Typ[1]	Max	Unit
1		Operating voltage[2]		2.7	—	5.5	V
2	P	Output high voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = –4 mA 3 V, I_{Load} = –2 mA 5 V, I_{Load} = –2 mA 3 V, I_{Load} = –1 mA	V_{OH}	 V_{DD} – 1.5 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.8	 — — — —	 — — — —	V
		Output high voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = –15 mA 3 V, I_{Load} = –8 mA 5 V, I_{Load} = –8 mA 3 V, I_{Load} = –4 mA		 V_{DD} – 1.5 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.8	 — — — —	 — — — —	
3	P	Output low voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = 4mA 3 V, I_{Load} = 2 mA 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 1 mA	V_{OL}		 — — — —	 1.5 1.5 0.8 0.8	V
		Output low voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = 15 mA 3 V, I_{Load} = 8 mA 5 V, I_{Load} = 8 mA 3 V, I_{Load} = 4 mA			 — — — —	 1.5 1.5 0.8 0.8	
4	P	Output high current — Max total I_{OH} for all ports 5V 3V	I_{OHT}	 — —	 — —	 100 60	mA
5	P	Output low current — Max total I_{OL} for all ports 5V 3V	I_{OLT}	 — —	 — —	 100 60	mA
6	P	Input high voltage; all digital inputs	V_{IH}				V
		V_{DD} = 5V V_{DD} = 3V		3.25 2.10	— —	— —	

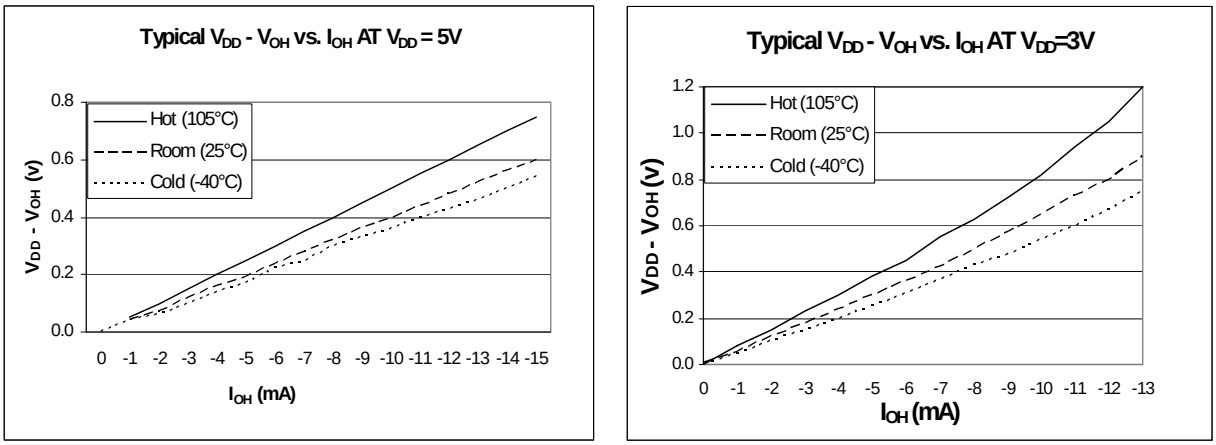


Figure 7. Typical High-side Drive (source) characteristics – High Drive (PTxDSn = 1)

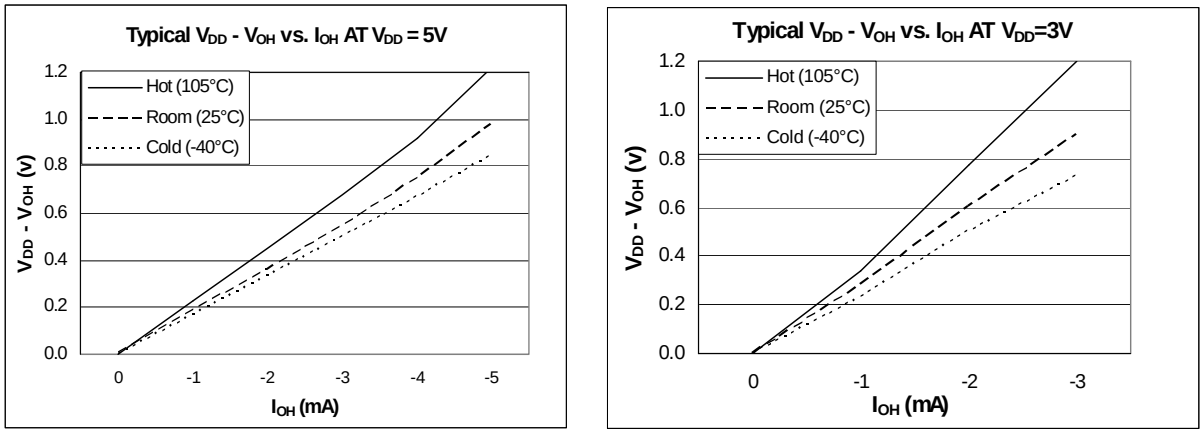


Figure 8. Typical High-side Drive (source) characteristics – Low Drive (PTxDSn = 0)

2.6 Supply Current Characteristics

Table 11. Supply Current Characteristics

Num	C	Parameter	Symbol	V_{DD} (V)	Typical[1]	Max[2]	Unit
1	C	Run supply current[3] measured at (CPU clock = 2 MHz, f_{Bus} = 1 MHz)	RI_{DD}	5	4.0	7	mA
				3	4.0	7	
2	P	Run supply current[3] measured at (CPU clock = 16 MHz, f_{Bus} = 8 MHz)		5	19	30	mA
				3	18.7	30	
3	C	Run supply current[3] measured at (CPU clock = 48 MHz, f_{Bus} = 24 MHz)		5	45	70	mA
				3	44	70	

Table 11. Supply Current Characteristics

Num	C	Parameter	Symbol	V_{DD} (V)	Typical[1]	Max[2]	Unit
4	C	Wait mode supply current[3] measured at (CPU clock = 2 MHz, f_{Bus} = 1 MHz)	WI_{DD}	5	2.03	3	mA
				3	2	3	
5	C	Wait mode supply current[3] measured at (CPU clock = 16 MHz, f_{Bus} = 8 MHz)		5	7.73	12	mA
				3	7.7	12	
6	C	Wait mode supply current[3] measured at (CPU clock = 48 MHz, f_{Bus} = 24 MHz)		5	22	30	mA
				3	21.9	30	
7	C	Stop2 mode supply current –40 °C 25 °C 105 °C	$S2I_{DD}$	5	1.35	3 3 35	µA
		–40 °C 25 °C 105 °C		3	1.25	3 3 35	µA
8	P	Stop3 mode supply current –40 °C 25 °C 105 °C	$S3I_{DD}$	5	1.41	3 3 35	µA
		–40 °C 25 °C 105 °C		3	1.35	3 3 35	µA
9	C	Stop4 mode supply current –40 °C 25 °C 105 °C	$S4I_{DD}$	5	106	200	µA
		–40 °C 25 °C 105 °C		3	96	200	µA
10	P	RTC adder to stop2 or stop3[4], 25°C	$S23I_{DDRTC}$	5	300	—	nA
				3	300	—	nA
11	P	Adder to stop3 for oscillator enabled[5] (ERCLKEN =1 and EREFSTEN = 1)	$S23I_{DDOSC}$	5	5	—	µA
				3	5	—	µA

1 Typicals are measured at 25°C.

2 Values given here are preliminary estimates prior to completing characterization.

3 All modules' clocks are switched on, code runs from flash, in FEI mode, and there are no DC loads on port pins.

4 Most customers are expected to find that auto-wakeup from stop2 or stop3 can be used instead of the higher current wait mode.

5 Values given under the following conditions: low range operation (RANGE = 0), low power mode (HGO = 0)

Table 14. 5 Volt 12-bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Comment
Conversion Time (Including sample time)	Short Sample (ADLSMP=0)	T	t_{ADC}	—	20	—	ADCK cycles	See Table 9 for conversion time variances
	Long Sample (ADLSMP=1)			—	40	—		
Sample Time	Short Sample (ADLSMP=0)	T	t_{ADS}	—	3.5	—	ADCK cycles	
	Long Sample (ADLSMP=1)			—	23.5	—		
Total Unadjusted Error	12 bit mode	T	E_{TUE}	—	±3.0	—	LSB[2]	Includes quantization
	10 bit mode	P		—	±1	±2.5		
	8 bit mode	T		—	±0.5	±1.0		
Differential Non-Linearity	12 bit mode	T	DNL	—	±1.75	—	LSB[2]	
	10 bit mode[3]	P		—	±0.5	±1.0		
	8 bit mode[3]	T		—	±0.3	±0.5		
Integral Non-Linearity	12 bit mode	T	INL	—	±1.5	—	LSB[2]	
	10 bit mode	T		—	±0.5	±1.0		
	8 bit mode	T		—	±0.3	±0.5		
Zero-Scale Error	12 bit mode	T	E_{ZS}	—	±1.5	—	LSB[2]	V_{ADIN} = V_{SSAD}
	10 bit mode	P		—	±0.5	±1.5		
	8 bit mode	T		—	±0.5	±0.5		
Full-Scale Error	12 bit mode	T	E_{FS}	—	±1	—	LSB[2]	V_{ADIN} = V_{DDAD}
	10 bit mode	T		—	±0.5	±1		
	8 bit mode	T		—	±0.5	±0.5		
Quantization Error	12 bit mode	D	E_Q	—	-1 to 0	—	LSB[2]	
	10 bit mode			—	—	±0.5		
	8 bit mode			—	—	±0.5		
Input Leakage Error	12 bit mode	D	E_{IL}	—	±1	—	LSB[2]	Pad leakage[4] * R_{AS}
	10 bit mode			—	±0.2	±2.5		
	8 bit mode			—	±0.1	±1		
Temp Sensor Voltage	25°C	D	V_{TEMP25}	—	1.396	—	V	
Temp Sensor Slope	-40°C - 25°C	D	m	—	3.266	—	mV/°C	
	25°C - 125°C			—	3.638	—		

1 Typical values assume V_{DDA} = 5.0V, Temp = 25°C, f_{ADCK}=1.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Monotonicity and No-Missing-Codes guaranteed in 10 bit and 8 bit modes

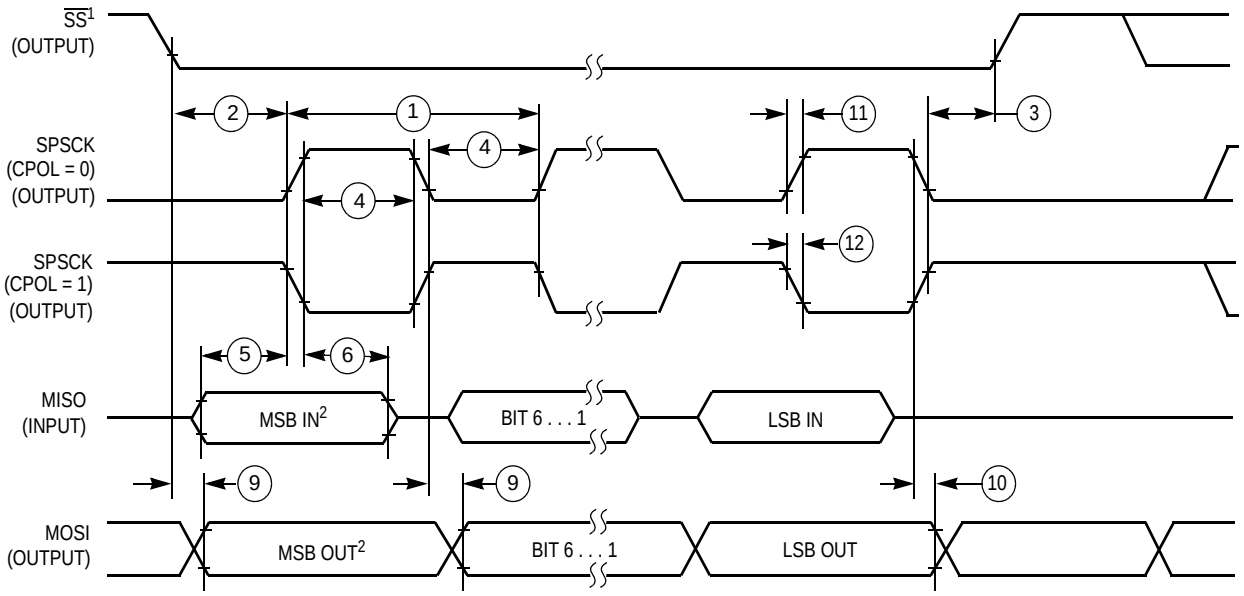
4 Based on input pad leakage current. Refer to pad electricals.

2.12 SPI Characteristics

Table 20 and Figure 14 through Figure 17 describe the timing requirements for the SPI system.

Table 20. SPI Timing

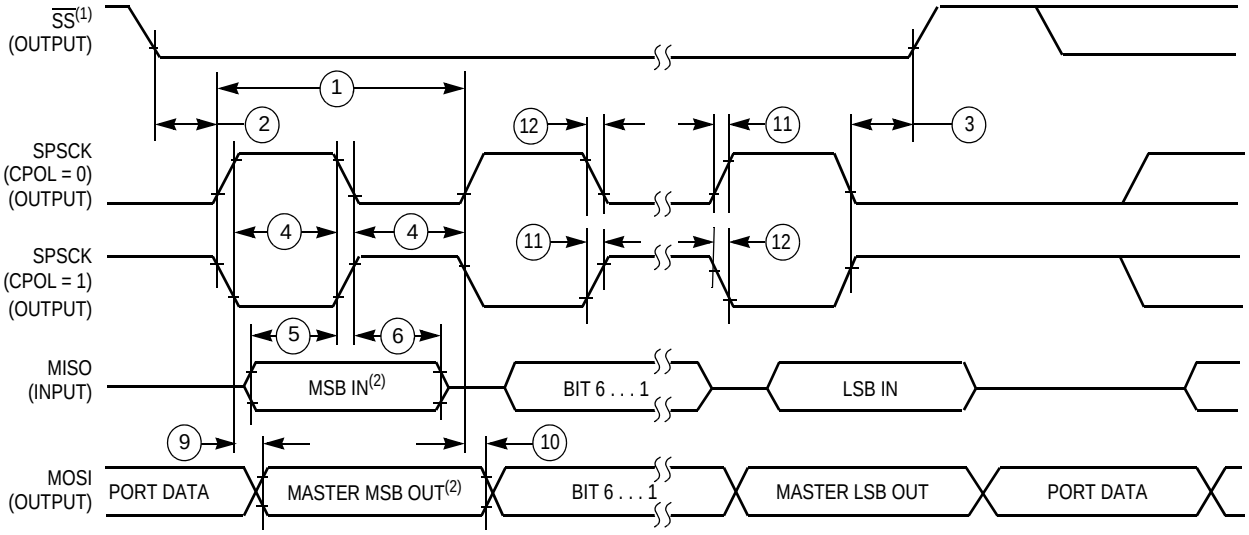
No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	$f_{Bus}/2048$ 0	$f_{Bus}/2$ $f_{Bus}/4$	Hz
1	D	SPSCK period Master Slave	t_{SPSCK}	2 4	2048 —	t_{cyc} t_{cyc}
2	D	Enable lead time Master Slave	t_{Lead}	1/2 1	— —	t_{SPSCK} t_{cyc}
3	D	Enable lag time Master Slave	t_{Lag}	1/2 1	— —	t_{SPSCK} t_{cyc}
4	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	$t_{cyc} - 30$ $t_{cyc} - 30$	1024 t_{cyc} —	ns ns
5	D	Data setup time (inputs) Master Slave	t_{SU}	15 15	— —	ns ns
6	D	Data hold time (inputs) Master Slave	t_{HI}	0 25	— —	ns ns
7	D	Slave access time	t_a	—	1	t_{cyc}
8	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
9	D	Data valid (after SPSCK edge) Master Slave	t_v	— —	25 25	ns ns
10	D	Data hold time (outputs) Master Slave	t_{HO}	0 0	— —	ns ns
11	D	Rise time Input Output	t_{RI} t_{RO}	— —	$t_{cyc} - 25$ 25	ns ns
12	D	Fall time Input Output	t_{FI} t_{FO}	— —	$t_{cyc} - 25$ 25	ns ns



NOTES:

1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

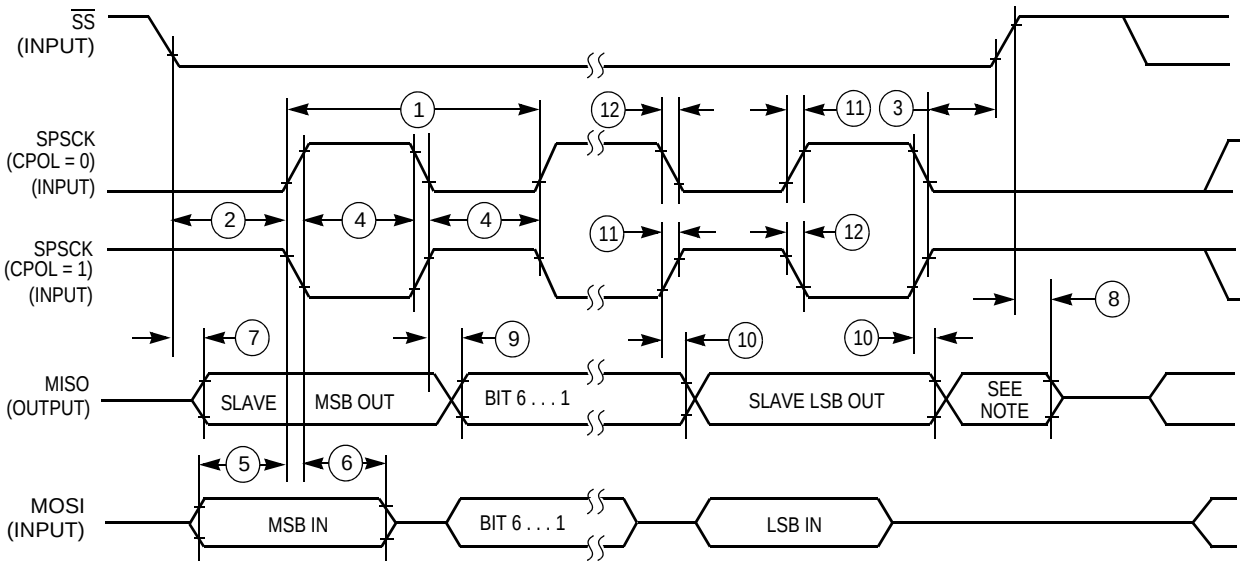
Figure 14. SPI Master Timing (CPHA = 0)



NOTES:

1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

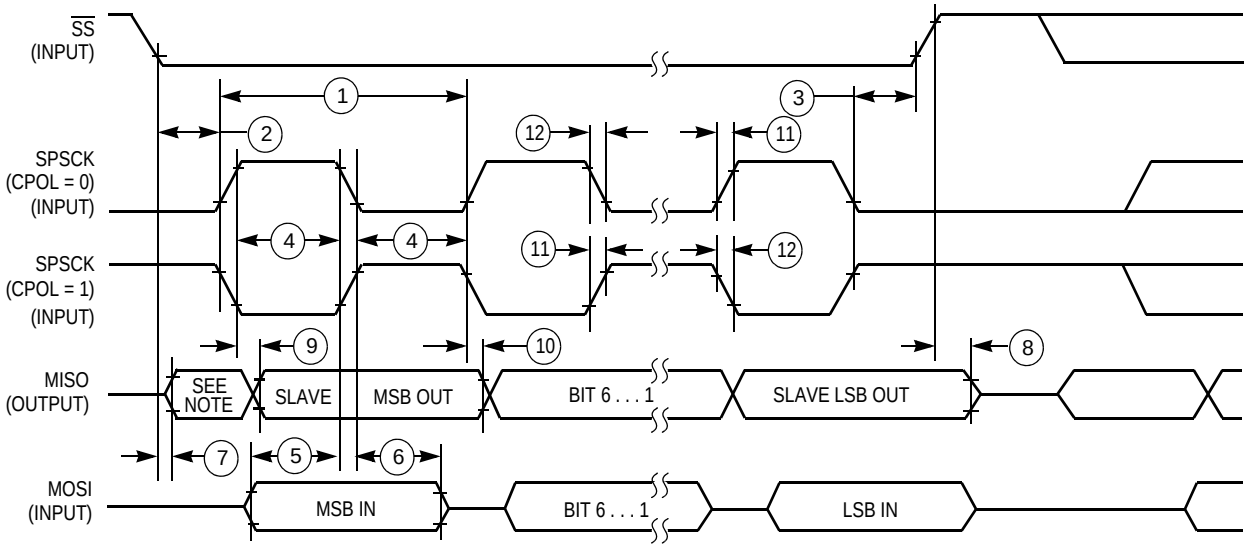
Figure 15. SPI Master Timing (CPHA = 1)



NOTE:

1. Not defined but normally MSB of character just received

Figure 16. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined but normally LSB of character just received

Figure 17. SPI Slave Timing (CPHA = 1)

2.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply.

Table 21. Flash Characteristics

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1		Supply voltage for program/erase	$V_{prog/erase}$	2.7		5.5	V
2		Supply voltage for read operation	V_{Read}	2.7		5.5	V
3		Internal FCLK frequency[2]	f_{FCLK}	150		200	kHz
4		Internal FCLK period (1/FCLK)	t_{Fcyc}	5		6.67	µs
5		Byte program time (random location)(2)	t_{prog}	9			t_{Fcyc}
6		Byte program time (burst mode)(2)	t_{Burst}	4			t_{Fcyc}
7		Page erase time[3]	t_{Page}	4000			t_{Fcyc}
8		Mass erase time(2)	t_{Mass}	20,000			t_{Fcyc}
9	C	Program/erase endurance[4] T_L to T_H = –40°C to + 105°C T = 25°C		10,000 —	— 100,000	— —	cycles
10		Data retention[5]	t_{D_ret}	15	100	—	years

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25°C unless otherwise stated.

2 The frequency of this clock is controlled by a software setting.

3 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

4 Typical endurance for Flash was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale Semiconductor defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory*.

5 Typical data retention values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale Semiconductor defines typical data retention, please refer to Engineering Bulletin EB618/D, Typical Data Retention for Nonvolatile Memory.

2.14 USB Electricals

The USB electricals for the USBOTG module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit http://www.usb.org.

If the Freescale USBOTG implementation requires additional or deviant electrical characteristics, this space would be used to communicate that information.

3 Mechanical Outline Drawings

3.1 80-pin LQFP

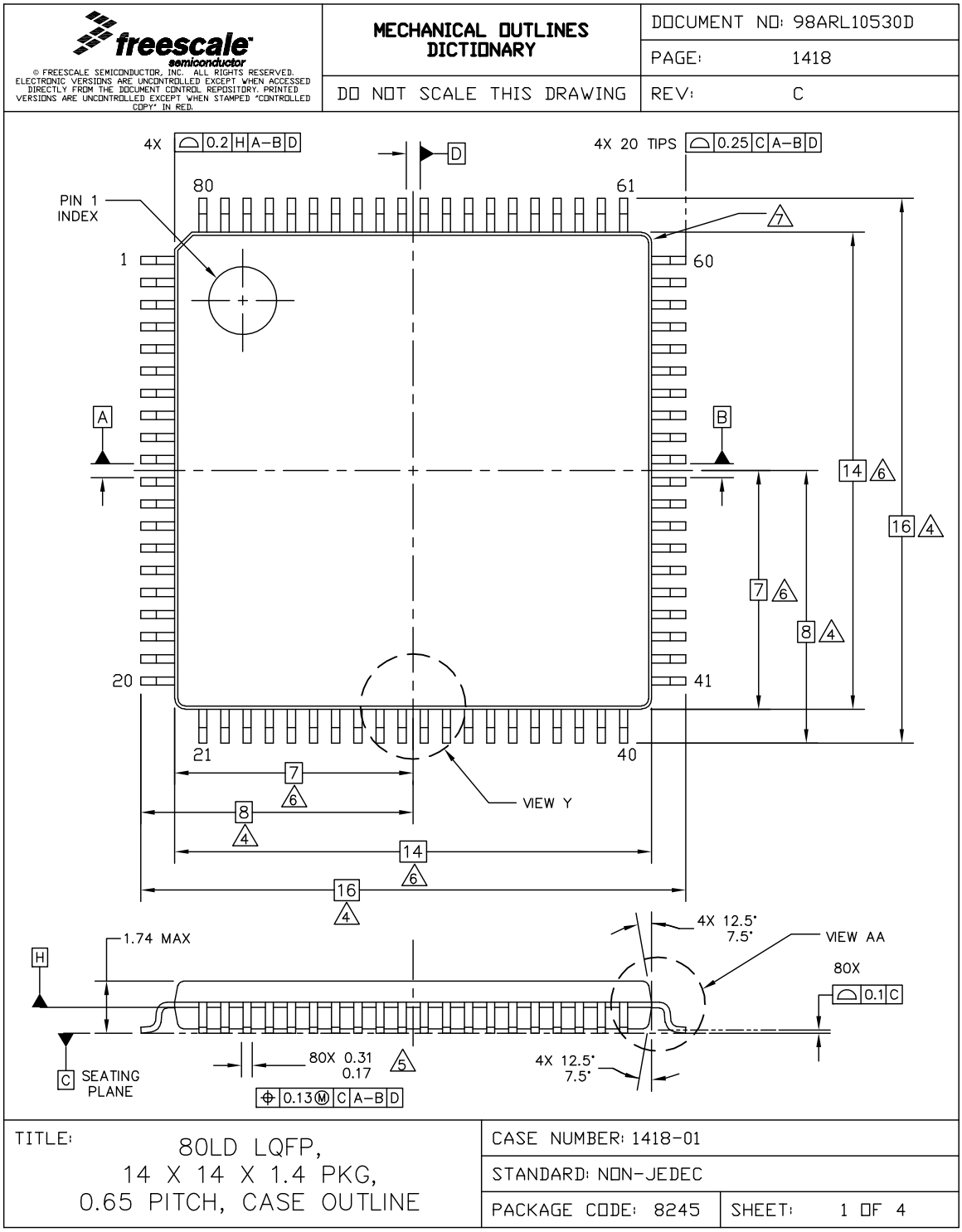


Figure 18. 80-pin LQFP Diagram - I

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASB42844B
		PAGE: 840B
	DO NOT SCALE THIS DRAWING	REV: B

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE −H− IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A−B AND −D− TO BE DETERMINED AT DATUM PLANE −H−.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE −C−.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE −H−.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDICTION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

TITLE: 64LD QFP (14 X 14)	CASE NUMBER: 840B−01	
	STANDARD: NON−JEDEC	
	PACKAGE CODE: 6057	SHEET: 3 OF 4

Figure 26. 64-pin QFP Diagram - III

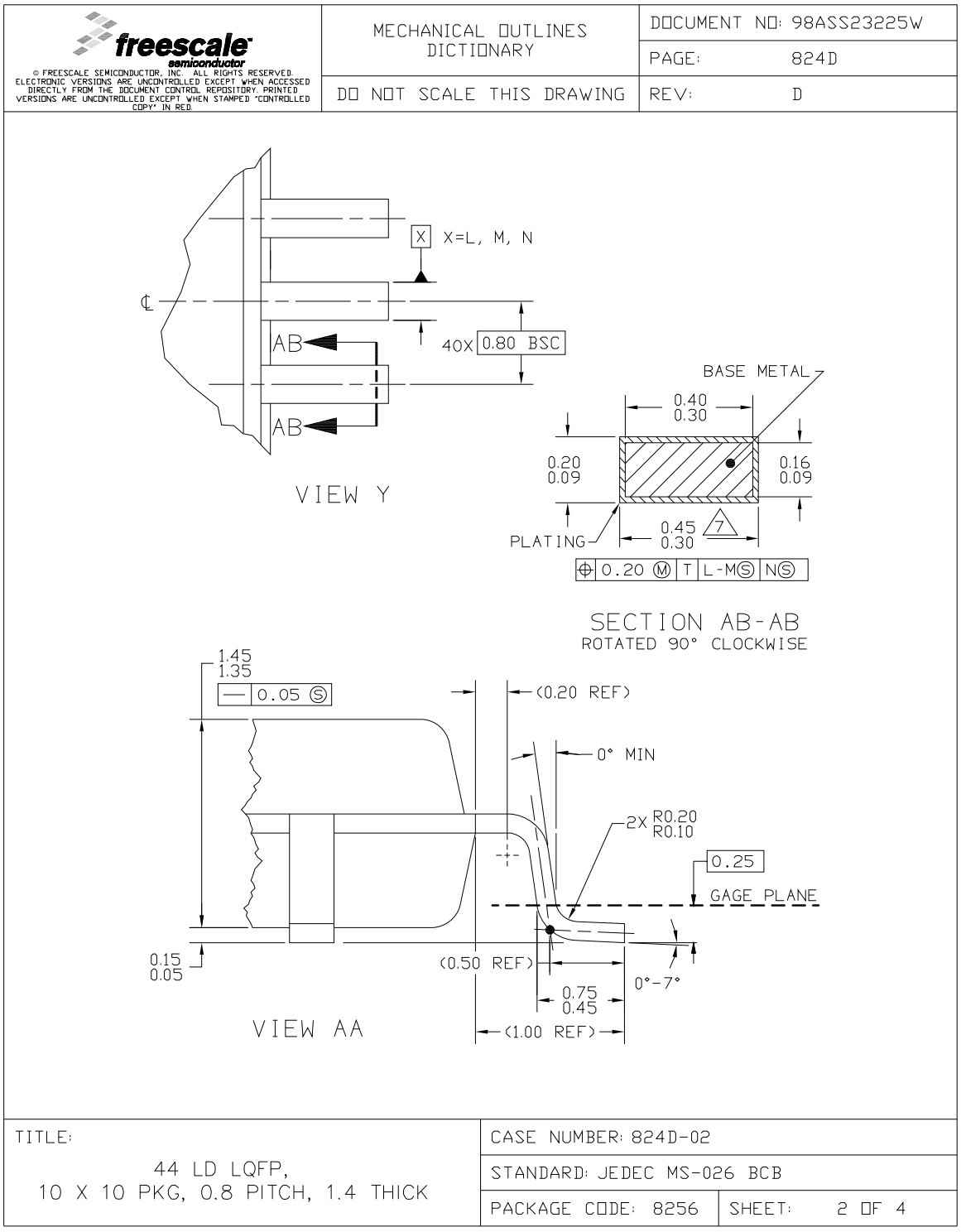


Figure 28. 44-pin LQFP Diagram - II

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23225W
		PAGE: 824D
	DO NOT SCALE THIS DRAWING	REV: D

NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DATUM PLANE H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS L, M AND N TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE T.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE DIMENSION TO EXCEED 0.53. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

TITLE: 44 LD LQFP, 10 X 10 PKG, 0.8 PITCH, 1.4 THICK	CASE NUMBER: 824D-02	
	STANDARD: JEDEC MS-026 BCB	
	PACKAGE CODE: 8256	SHEET: 3 OF 4

Figure 29. 44-pin LQFP Diagram - III

4 Revision History

This section lists major changes between versions of the MCF51JM128 Data Sheet document.

Table 23. Changes Between Revisions

Revision	Description
1	Updated features list Updated the figures Typical Low-side Drive (sink) characteristics – High Drive (PTxDSn = 1), Typical Low-side Drive (sink) characteristics – Low Drive (PTxDSn = 0), and Typical High-side Drive (source) characteristics – High Drive (PTxDSn = 1) Added the figure Typical High-side Drive (source) characteristics – Low Drive (PTxDSn = 0) Updated the table Supply Current Characteristics Updated the table Oscillator Electrical Specifications (Temperature Range = –40 to 105×C Ambient) Updated the table SPI Electrical Characteristic, DC Characteristics
2	Updated the table Orderable Part Number Summary, DC Characteristics, and Supply Current Characteristics
3	Updated the table Orderable Part Number Summary, MCG Characteristics, SPI Characteristics, and Supply Current Characteristics Changed V_{DDAD} to V_{DDA}, V_{SSAD} to V_{SSA} Updated the table Device comparison
4	Added “RAM retention voltage” parameter in “DC Characteristics” table, alongwith a table note. Added “Temp sensor voltage” parameter in “5 Volt 12-bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})” table. Added “ “Temp sensor slope” parameter in 5 Volt 12-bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) table. Also, corrected unit of “Temp sensor voltage” parameter in 5 Volt 12-bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) table.

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