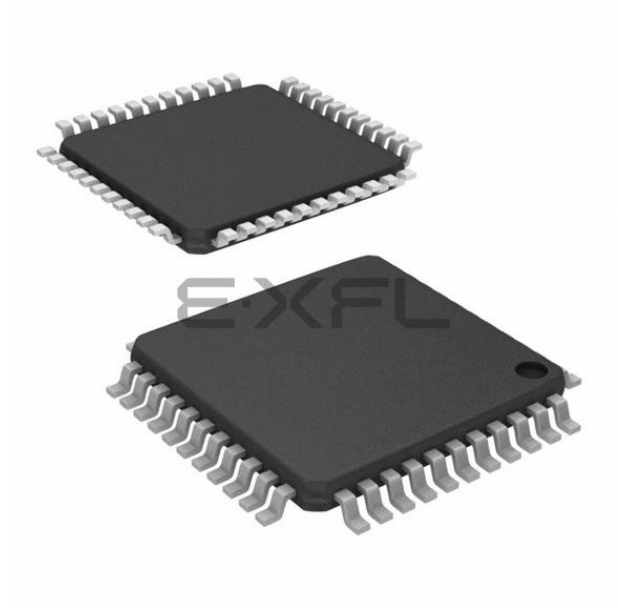

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SCI, SPI, USB OTG
Peripherals	LVD, PWM, WDT
Number of I/O	33
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf51jm64vld

1.3 Features

Table 2 describes the functional units of the MCF51JM128 series.

Table 2. MCF51JM128 Series Functional Units

Unit	Function
CF1CORE (V1 ColdFire core)	Executes programs and interrupt handlers
BDM (background debug module)	Provides a single-pin debugging interface (part of the V1 ColdFire core)
DBG (debug)	Provides debugging and emulation capabilities (part of the V1 ColdFire core)
SYSCTL (system control)	Provides LVD, COP, external interrupt request, and so on
FLASH (flash memory)	Provides storage for program code and constants
RAM (random-access memory)	Provides storage for program code, constants, and variables
RGPIO (rapid general-purpose input/output)	Allows I/O port access at CPU clock speeds
VREG (voltage regulator)	Controls power management throughout the device
USBOTG (USB On-The-Go)	Supports the USB On-The-Go dual-role controller
ADC (analog-to-digital converter)	Measures analog voltages at up to 12 bits of resolution
TPM1, TPM2 (timer/pulse-width modulators)	Provide a variety of timing-based features
CF1_INTC (interrupt controller)	Controls and prioritizes all device interrupts
CAU (cryptographic acceleration unit)	Co-processor support for DES, 3DES, AES, MD5, and SHA-1
RNGA (random number generator accelerator)	32-bit random number generator that complies with FIPS-140
RTC (real-time counter)	Provides a constant-time base with optional interrupt
ACMP (analog comparator)	Compares two analog inputs
CMT (carrier modulator timer)	Infrared output used for the Remote Controller
IIC1, IIC2 (inter-integrated circuits)	Supports the standard IIC communications protocol
KBI (keyboard interrupt)	Provides pin interrupt capabilities
MCG (multipurpose clock generator)	Provides clocking options for the device, including a phase-locked loop (PLL) and frequency-locked loop (FLL) for multiplying slower reference clock sources
XOSC (crystal oscillator)	Supports low/high range crystals
CAN (controller area network)	Supports standard CAN communications protocol
SCI1, SCI2 (serial communications interfaces)	Serial communications UARTs that can support RS-232 and LIN protocols
SPI1, SPI2 (serial peripheral interfaces)	Provide a 4-pin synchronous serial interface

1.3.1 Feature List

- 32-bit Version 1 ColdFire Central Processor Unit (CPU)
  - Up to 50.33 MHz at 2.7 V – 5.5 V
  - Performance (Dhrystone 2.1):
    - 0.94 Dhrystone 2.1 MIPS per MHz when running from internal RAM
    - 0.76 Dhrystone 2.1 MIPS per MHz when running from flash
  - Implements Instruction Set Revision C (ISA_C)
  - Supports up to 30 peripheral interrupt requests and seven software interrupts
- On-chip memory
  - Up to 128 KB Flash memory with read/program/erase over full operating voltage and temperature range
  - Up to 16 KB static random access memory (RAM)
  - Security circuitry to prevent unauthorized access to RAM and flash contents
- Power-saving modes
  - Two low-power stop plus wait modes
  - Peripheral clock enable register can disable clocks to unused modules, thereby reducing currents; this behavior allows clocks to remain enabled to specific perhipherals in Stop3 mode
  - Very lower power real-time counter for use in run, wait, and stop modes with internal and external clock sources
- Four Clock Source Options
  - Oscillator (XOSC) — Loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - FLL/PLL controlled by internal or external reference
  - Trimmable internal reference allows 0.2% resolution and 2% deviation
- System protection features
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock
  - Low-voltage detection with reset or interrupt; selectable trip points
  - Illegal opcode and illegal address detection with programmable reset or exception response
  - Flash block protection
- Debug support
  - Single-wire Background debug interface
  - 4 Program Counters plus two address (optional data) breakpoint registers with programmable 1- or 2-level trigger response
  - 64-entry processor status and debug data trace buffer with programmable start/stop conditions
- Universal Serial Bus (USB) On-The-Go dual-role controller
  - Full-speed USB device controller
    - Fully compliant with USB specification 1.1 and 2.0
    - 16 bidirectional endpoints, with double buffering to provide the maximum throughput
    - Supports control, bulk, interrupt, and isochronous endpoints
    - Supports bus-powered capability with low-power consumption
  - Full-speed / low-speed host controller
    - Host mode allows control, bulk, interrupt, and isochronous transfers
  - OTG protocol logic
  - On-chip USB transceiver
  - On-chip 3.3 V USB regulator and pull-up resistors save system cost

- Controller area network (MSCAN)
  - Implementation of the CAN protocol — Version 2.0A/B
  - Five receive buffers with FIFO storage scheme
  - Three transmit buffers with internal prioritization using a “local priority” concept
  - Flexible maskable identifier filter programmable as 2x32-bit, 4x16-bit, or 8x8-bit
  - Programmable wakeup functionality with integrated low-pass filter
  - Programmable loopback mode supports self-test operation
  - Programmable bus-off recovery functionality
  - Internal timer for time-stamping of received and transmitted messages
- Cryptographic acceleration unit (CAU)
  - Co-processor support of DES, 3DES, AES, MD5, and SHA-1
- Random number generator accelerator (RNGA)
  - 32-bit random number generator that complies with FIPS-140
- Analog-to-digital converter (ADC)
  - 12-channel, 12-bit resolution
  - Output formatted in 12-, 10-, or 8-bit right-justified format
  - Single or continuous conversion, and selectable asynchronous hardware conversion trigger
  - Operation in Stop3 mode
  - Automatic compare function
  - Internal temperature sensor
- Analog comparators (ACMP)
  - Selectable interrupt on rising edge, falling edge, or either rising or falling edges of comparator output
  - Option to compare to fixed internal bandgap reference voltage
  - Option to route output to TPM module
  - Operation in Stop3 mode
- Inter-integrated circuit (IIC)
  - Up to 100 kbps with maximum bus loading
  - Multi-master operation
  - Programmable slave address
  - Supports broadcast mode and 10-bit address extension
- Serial communications interfaces (SCI)
  - Two SCIs with full-duplex, non-return-to-zero (NRZ) format
  - LIN master extended break generation
  - LIN slave extended break detection
  - Programmable 8-bit or 9-bit character length
  - Wake up on active edge
- Serial peripheral interfaces (SPI)
  - Two serial peripheral interfaces with full-duplex or single-wire bidirectional
  - Double-buffered transmit and receive
  - Programmable transmit bit rate, phase, polarity, and Slave Select output
  - MSB-first or LSB-first shifting
- Timer/pulse width modulator (TPM)
  - 16-bit free-running or modulo up/down count operation
  - Up to eight channels, where each channel can be an input capture, output compare, or edge-aligned PWM
  - One interrupt per channel plus terminal count interrupt

Figure 4 shows the pinout of the 44-pin LQFP.

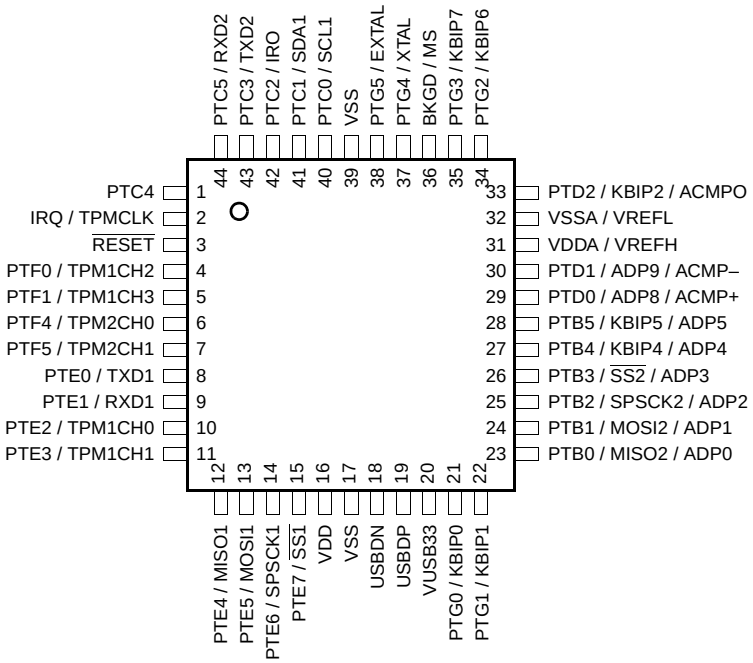


Figure 4. 44-pin LQFP

Table 4 shows the package pin assignments.

Table 4. Pin Assignments by Package and Pin Sharing Priority

Pin Number			<-- Lowest **Priority** --> Highest		
80	**64**	**44**	**Port Pin**	**Alt 1**	**Alt 2**
1	1	1	PTC4		—
2	2	2	—	IRQ	TPMCLK
3	3	3	—	$\overline{\text{RESET}}$	—
4	4	4	PTF0	TPM1CH2	—
5	5	5	PTF1	TPM1CH3	—
6	6	—	PTF2	TPM1CH4	—
7	7	—	PTF3	TPM1CH5	—
8	8	6	PTF4	TPM2CH0	BUSCLK_OUT
9	9	—	PTC6	RXCAN	—
10	10	—	PTF7	TXCAN	—
11	11	7	PTF5	TPM2CH1	—
12	12	—	PTF6	—	—
13	13	8	PTE0	TXD1	—
14	14	9	PTE1	RXD1	—
15	15	10	PTE2	TPM1CH0	—

Table 4. Pin Assignments by Package and Pin Sharing Priority (continued)

Pin Number			<-- Lowest **Priority** --> Highest		
80	**64**	**44**	**Port Pin**	**Alt 1**	**Alt 2**
49	41	—	PTB7	ADP7	—
50	42	29	PTD0	ADP8	ACMP+
51	43	30	PTD1	ADP9	ACMP–
52	44	31	—	—	VDDA
53	45		—	—	VREFH
54	46	32	—	—	VREFL
55	47		—	—	VSSA
56	48	33	PTD2	KBIP2	ACMPO
57	—	—	PTJ0	RGPIO11	—
58	—	—	PTJ1	RGPIO12	—
59	—	—	PTJ2	RGPIO13	—
60	—	—	PTJ3	RGPIO14	—
61	—	—	PTJ4	RGPIO15	—
62	49	—	PTD3	KBIP3	ADP10
63	50	—	PTD4	ADP11	—
64	51	—	PTD5	—	—
65	52	—	PTD6	—	—
66	53	—	PTD7	—	—
67	54	34	PTG2	KBIP6	—
68	55	35	PTG3	KBIP7	—
69	56	36	—	BKGD	MS
70	57	37	PTG4	XTAL	
71	58	38	PTG5	EXTAL	
72	59	39	—	—	VSS
73	—	—	—	—	VDD
74	—	—	PTG6	—	—
75	—	—	PTG7	—	—
76	60	40	PTC0	SCL1	—
77	61	41	PTC1	SDA1	—
78	62	42	PTC2	IRO	—
79	63	43	PTC3	TXD2	—
80	64	44	PTC5	RXD2	—

Table 9. ESD and Latch-Up Protection Characteristics

Num	Rating	Symbol	Min	Max	Unit
1	Human Body Model (HBM)	V_{HBM}	+/– 2000	—	V
2	Charge Device Model (CDM)	V_{CDM}	+/– 500	—	V
3	Latch-up Current at T_A = 105°C	I_{LAT}	+/– 100	—	mA

2.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 10. DC Characteristics

Num	C	Parameter	Symbol	Min	Typ[1]	Max	Unit
1		Operating voltage[2]		2.7	—	5.5	V
2	P	Output high voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = –4 mA 3 V, I_{Load} = –2 mA 5 V, I_{Load} = –2 mA 3 V, I_{Load} = –1 mA	V_{OH}	 V_{DD} – 1.5 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.8	 — — — —	 — — — —	V
		Output high voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = –15 mA 3 V, I_{Load} = –8 mA 5 V, I_{Load} = –8 mA 3 V, I_{Load} = –4 mA		 V_{DD} – 1.5 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.8	 — — — —	 — — — —	
3	P	Output low voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = 4mA 3 V, I_{Load} = 2 mA 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 1 mA	V_{OL}		 — — — —	 1.5 1.5 0.8 0.8	V
		Output low voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = 15 mA 3 V, I_{Load} = 8 mA 5 V, I_{Load} = 8 mA 3 V, I_{Load} = 4 mA			 — — — —	 1.5 1.5 0.8 0.8	
4	P	Output high current — Max total I_{OH} for all ports 5V 3V	I_{OHT}	 — —	 — —	 100 60	mA
5	P	Output low current — Max total I_{OL} for all ports 5V 3V	I_{OLT}	 — —	 — —	 100 60	mA
6	P	Input high voltage; all digital inputs	V_{IH}				V
		V_{DD} = 5V V_{DD} = 3V		3.25 2.10	— —	— —	

1 Typical values are based on characterization data at 25°C unless otherwise stated.
2 Operating voltage with USB enabled can be found in Section 2.14, “USB Electricals.”
3 Measured with $V_{In} = V_{DD}$ or V_{SS}.
4 Measured with $V_{In} = V_{SS}$.
5 Measured with $V_{In} = V_{DD}$.
6 This is the voltage below which the contents of RAM are not guaranteed to be maintained.

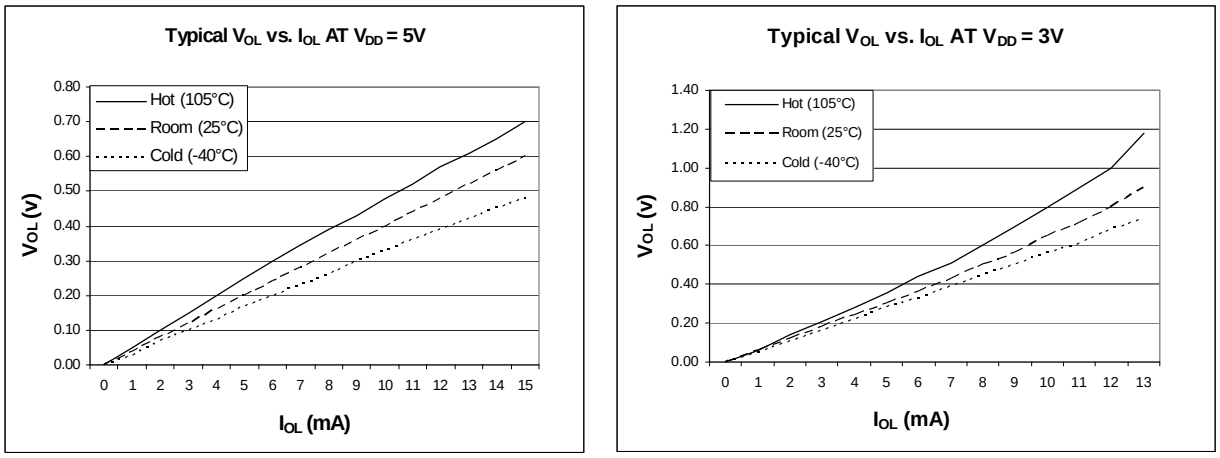


Figure 5. Typical Low-side Drive (sink) characteristics – High Drive (PTxDSn = 1)

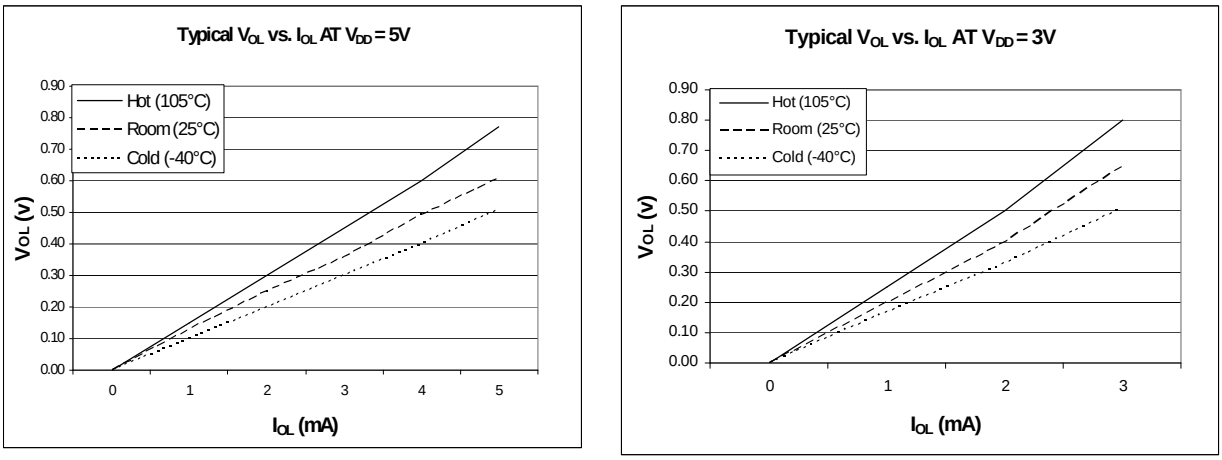


Figure 6. Typical Low-side Drive (sink) characteristics – Low Drive (PTxDSn = 0)

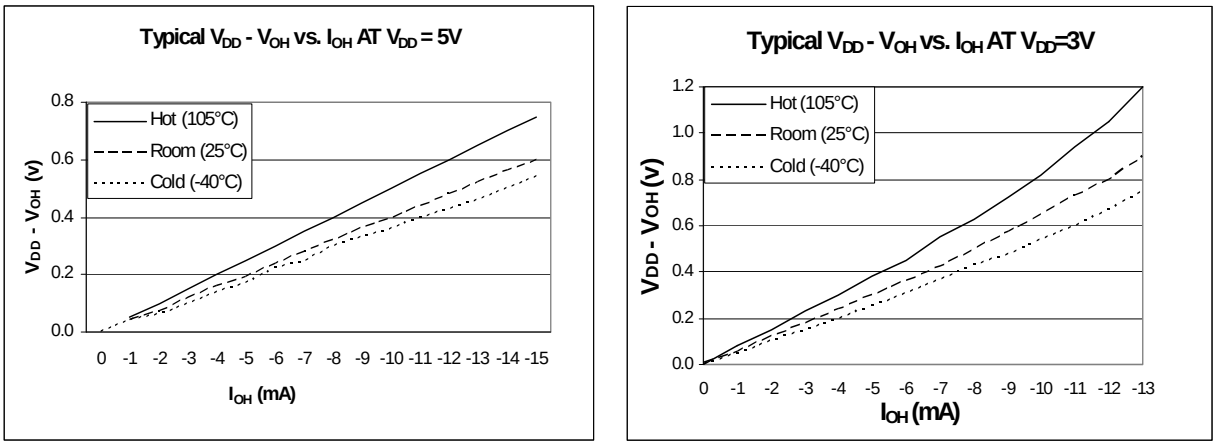


Figure 7. Typical High-side Drive (source) characteristics – High Drive (PTxDSn = 1)

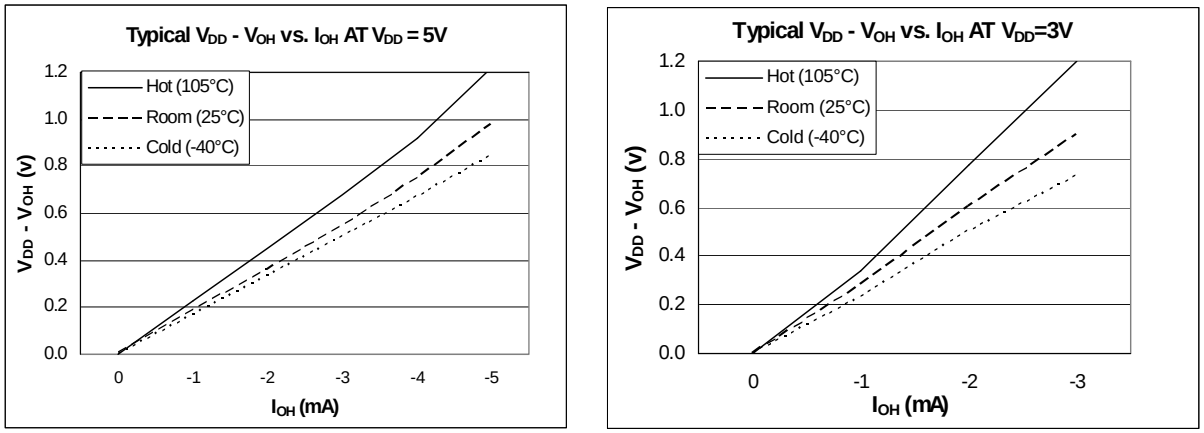


Figure 8. Typical High-side Drive (source) characteristics – Low Drive (PTxDSn = 0)

2.6 Supply Current Characteristics

Table 11. Supply Current Characteristics

Num	C	Parameter	Symbol	V_{DD} (V)	Typical[1]	Max[2]	Unit
1	C	Run supply current[3] measured at (CPU clock = 2 MHz, f_{Bus} = 1 MHz)	RI_{DD}	5	4.0	7	mA
				3	4.0	7	
2	P	Run supply current[3] measured at (CPU clock = 16 MHz, f_{Bus} = 8 MHz)		5	19	30	mA
				3	18.7	30	
3	C	Run supply current[3] measured at (CPU clock = 48 MHz, f_{Bus} = 24 MHz)		5	45	70	mA
				3	44	70	

2.10 MCG Specifications

Table 16. MCG Frequency Specifications (Temperature Range = –40 to 125°C Ambient)

Num	C	Rating		Symbol	Min	Typical[1]	Max	Unit
1	P	Internal reference frequency - factory trimmed at V_{DD} = 5 V and temperature = 25 °C		f_{int_ft}	—	32.768	—	kHz
2	P	Average internal reference frequency – untrimmed		f_{int_ut}	31.25	—	39.0625	kHz
3	T	Internal reference startup time		t_{irefst}	—	60	100	µs
4	P	DCO output frequency range - untrimmed [2]	Low range (DRS=00)	f_{dco_ut}	16	—	20	MHz
	P		Mid range (DRS=01)		32	—	40	
	P		High range (DRS=10)		48	—	60	
5	P	DCO output frequency[2] Reference =32768Hz and DMX32 = 1	Low range (DRS=00)	f_{dco_DMX32}	—	19.92	—	MHz
	P		Mid range (DRS=01)		—	39.85	—	
	P		High range (DRS=10)		—	59.77	—	
6	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
7	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	$\%f_{dco}$
8	D	Total deviation of trimmed DCO output frequency over voltage and temperature		Δf_{dco_t}	—	0.5 –1.0	±2	$\%f_{dco}$
9	D	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 – 70 °C		Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$
10	D	FLL acquisition time [3]		$t_{fll\_acquire}$	—	—	1	ms
11	D	PLL acquisition time [4]		$t_{pll\_acquire}$	—	—	1	ms
12	D	Long term Jitter of DCO output clock (averaged over 2ms interval) [5]		C_{Jitter}	—	0.02	0.2	$\%f_{dco}$
13	D	VCO operating frequency		f_{vco}	7.0	—	55.0	MHz
14	D	Jitter of PLL output clock measured over 625 ns[6]		$f_{pll\_jitter\_625ns}$	—	0.566[5]	—	$\%f_{pll}$
15	D	Lock entry frequency tolerance [7]		D_{lock}	±1.49	—	±2.98	%
16	D	Lock exit frequency tolerance [8]		D_{unl}	±4.47	—	±5.97	%
17	D	Lock time — FLL		t_{fll_lock}	—	—	$t_{fll\_acquire}$+ 1075(1/f_{int_t})	s
18	D	Lock time — PLL		t_{pll_lock}	—	—	$t_{pll\_acquire}$+ 1075(1/f_{pll_ref})	s
19	D	Loss of external clock minimum frequency – RANGE = 0		f_{loc_low}	(3/5) x f_{int}	—	—	kHz

1 Data in Typical column was characterized at 5.0 V, 25C or is typical recommended value

2 The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

3 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

5 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

6 625 ns represents 5 time quanta for CAN applications, under worst case conditions of 8 MHz CAN bus clock, 1 Mbps CAN bus speed, and 8 time quanta per bit for bit time settings. 5 time quanta is the minimum time between a synchronization edge and the sample point of a bit using 8 time quanta per bit.

7 Below D_{lock} minimum, the MCG is guaranteed to enter lock. Above D_{lock} maximum, the MCG will not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.

8 Below D_{unl} minimum, the MCG will not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.

2.11 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

2.11.1 Control Timing

Table 17. Control Timing

Num	C	Parameter	Symbol	Min	Typ[1]	Max	Unit
1		Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	dc	—	24	MHz
2		Internal low-power oscillator period	t_{LPO}	700		1300	µs
3		External reset pulse width[2] ($t_{cyc} = 1/f_{Self\_reset}$)	t_{extrst}	100		—	ns
4		Reset low drive	t_{rstdrv}	66 x t_{cyc}		—	ns
5		Active background debug mode latch setup time	t_{MSSU}	500		—	ns
6		Active background debug mode latch hold time	t_{MSH}	100		—	ns
7		IRQ pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}, t_{IHIL}	 100 1.5 x t_{cyc}	—	—	ns
8		KBIPx pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}, t_{IHIL}	 100 1.5 x t_{cyc}	—	—	ns
9		Port rise and fall time (load = 50 pF)[4] Slew rate control disabled (PTxSE = 0) High drive Slew rate control enabled (PTxSE = 1) High drive Slew rate control disabled (PTxSE = 0) Low drive Slew rate control enabled (PTxSE = 1) Low drive	t_{Rise}, t_{Fall}	 — — 	 11 35 40 75		ns

1 Typical values are based on characterization data at V_{DD} = 5.0V, 25°C unless otherwise stated.

2 This is the shortest pulse guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

3 This is the minimum pulse width guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

4 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 105°C.

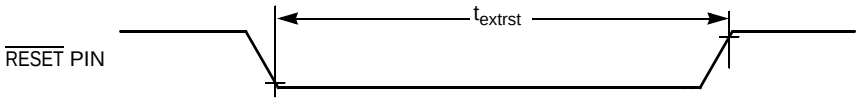


Figure 10. Reset Timing

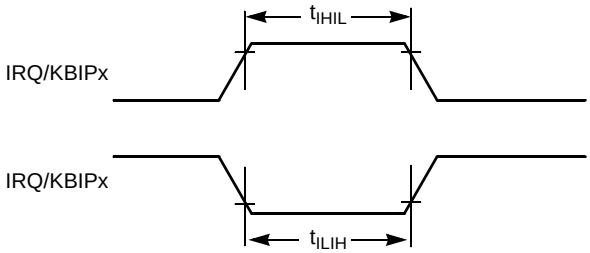


Figure 11. IRQ/KBIPx Timing

2.11.2 Timer/PWM (TPM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 18. TPM Input Timing

NUM	C	Function	Symbol	Min	Max	Unit
1	—	External clock frequency	f_{TPMext}	dc	$f_{Bus}/4$	MHz
2	—	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

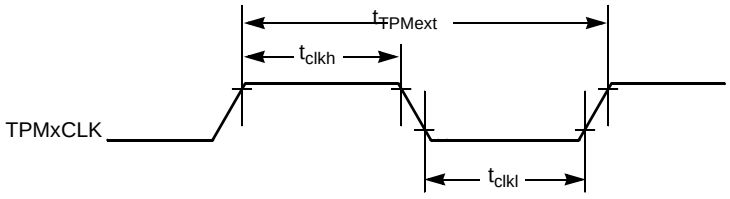
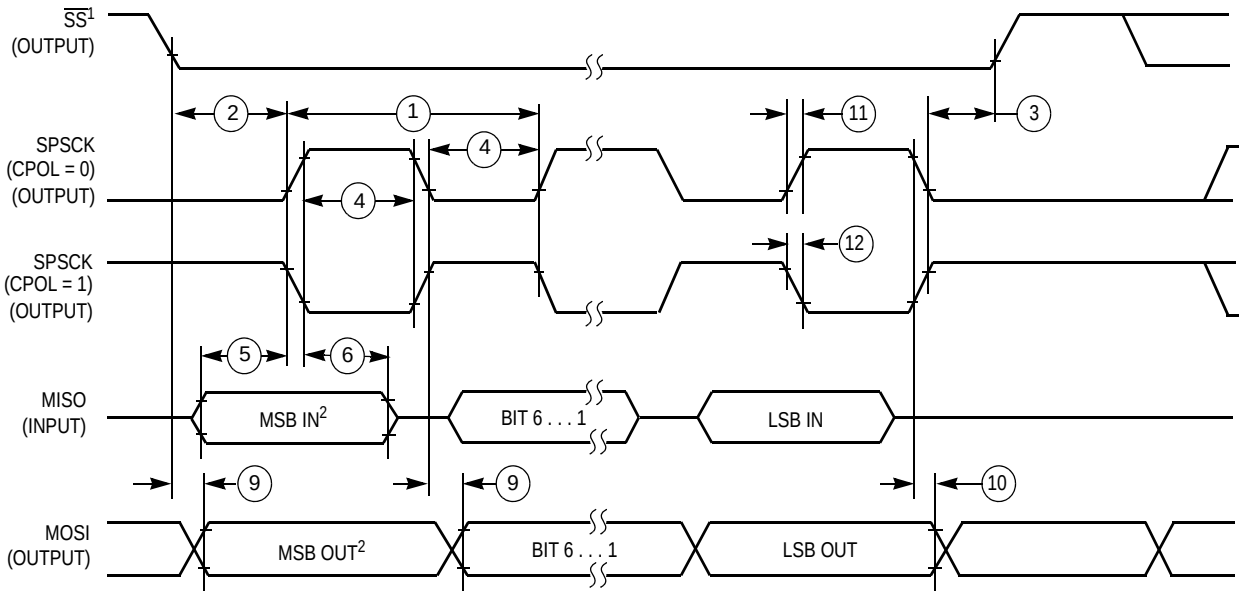


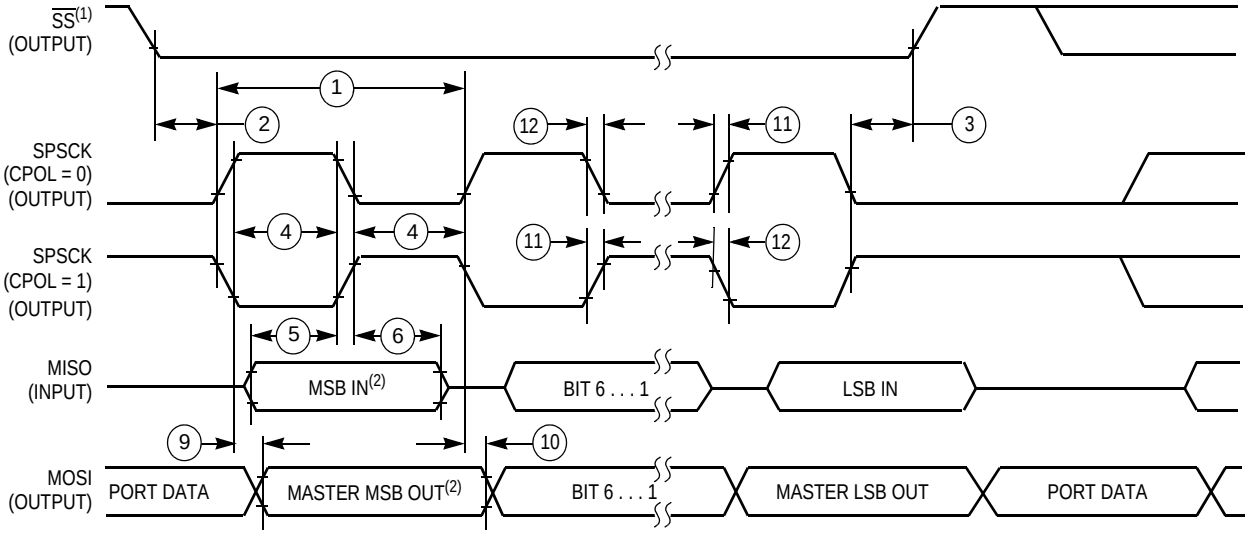
Figure 12. Timer External Clock



NOTES:

1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 14. SPI Master Timing (CPHA = 0)



NOTES:

1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 15. SPI Master Timing (CPHA = 1)

2.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply.

Table 21. Flash Characteristics

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1		Supply voltage for program/erase	$V_{prog/erase}$	2.7		5.5	V
2		Supply voltage for read operation	V_{Read}	2.7		5.5	V
3		Internal FCLK frequency[2]	f_{FCLK}	150		200	kHz
4		Internal FCLK period (1/FCLK)	t_{Fcyc}	5		6.67	µs
5		Byte program time (random location)(2)	t_{prog}	9			t_{Fcyc}
6		Byte program time (burst mode)(2)	t_{Burst}	4			t_{Fcyc}
7		Page erase time[3]	t_{Page}	4000			t_{Fcyc}
8		Mass erase time(2)	t_{Mass}	20,000			t_{Fcyc}
9	C	Program/erase endurance[4] T_L to T_H = –40°C to + 105°C T = 25°C		10,000 —	— 100,000	— —	cycles
10		Data retention[5]	t_{D_ret}	15	100	—	years

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25°C unless otherwise stated.

2 The frequency of this clock is controlled by a software setting.

3 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

4 Typical endurance for Flash was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale Semiconductor defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory*.

5 Typical data retention values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale Semiconductor defines typical data retention, please refer to Engineering Bulletin EB618/D, Typical Data Retention for Nonvolatile Memory.

2.14 USB Electricals

The USB electricals for the USBOTG module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit http://www.usb.org.

If the Freescale USBOTG implementation requires additional or deviant electrical characteristics, this space would be used to communicate that information.

3 Mechanical Outline Drawings

3.1 80-pin LQFP

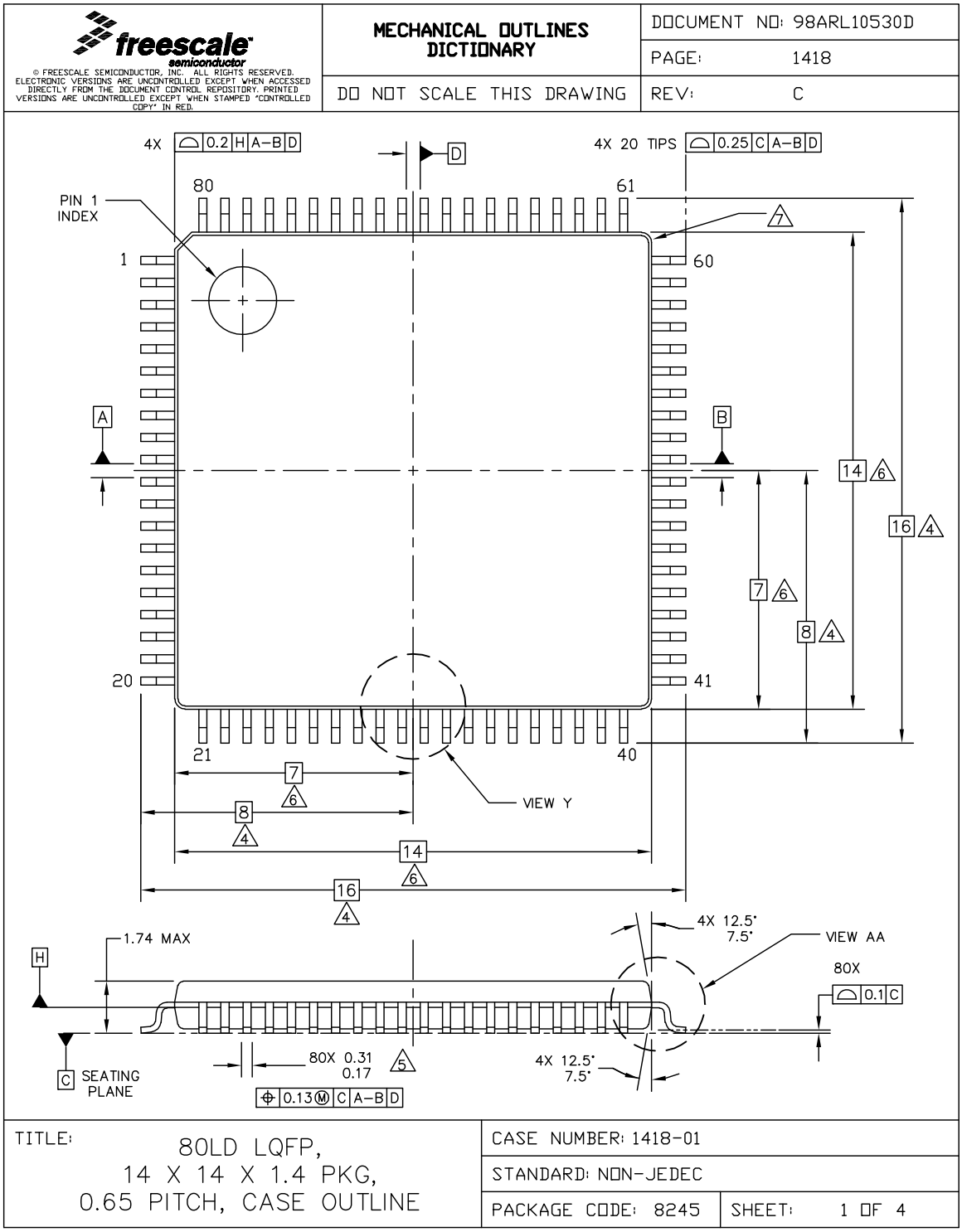


Figure 18. 80-pin LQFP Diagram - I

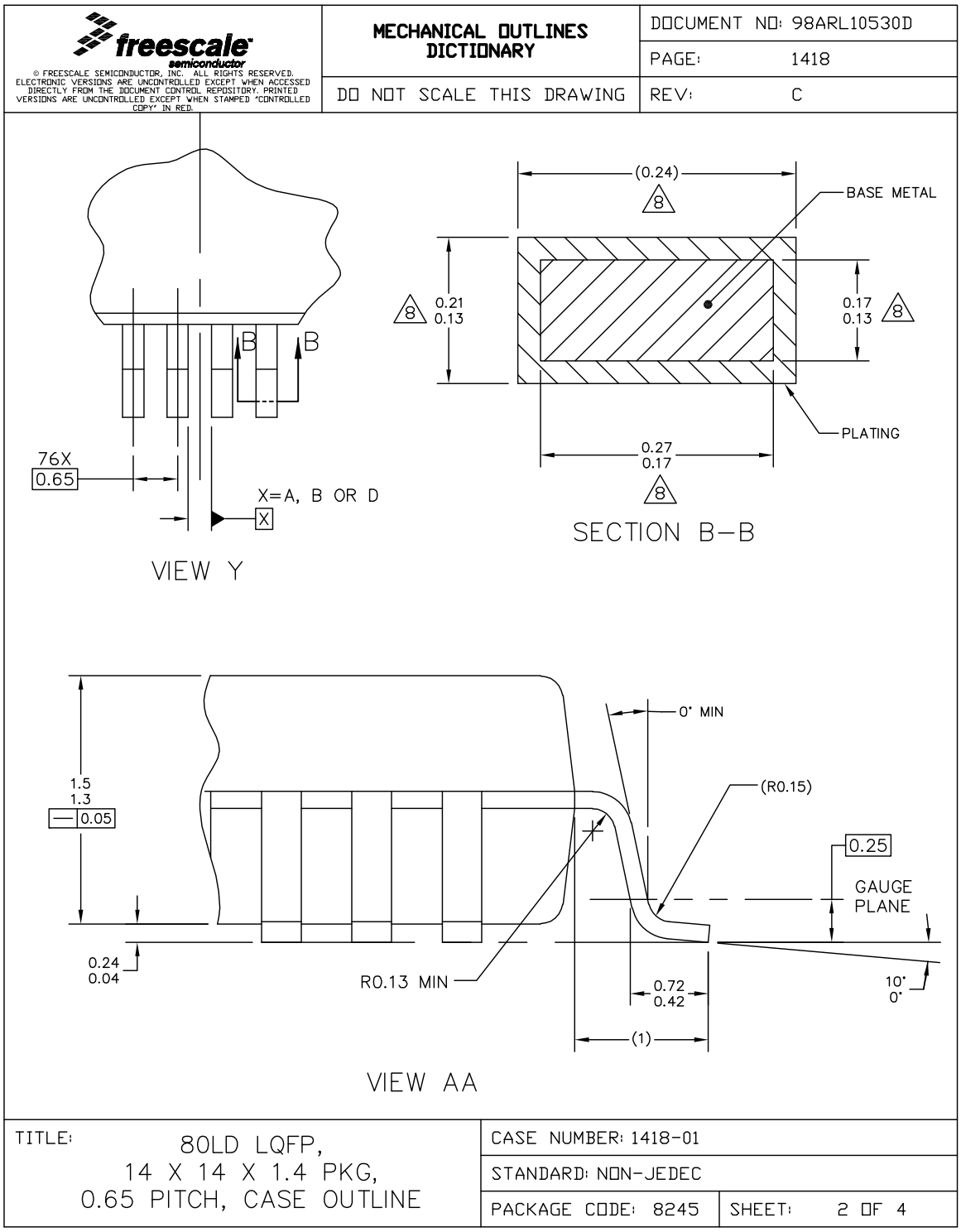
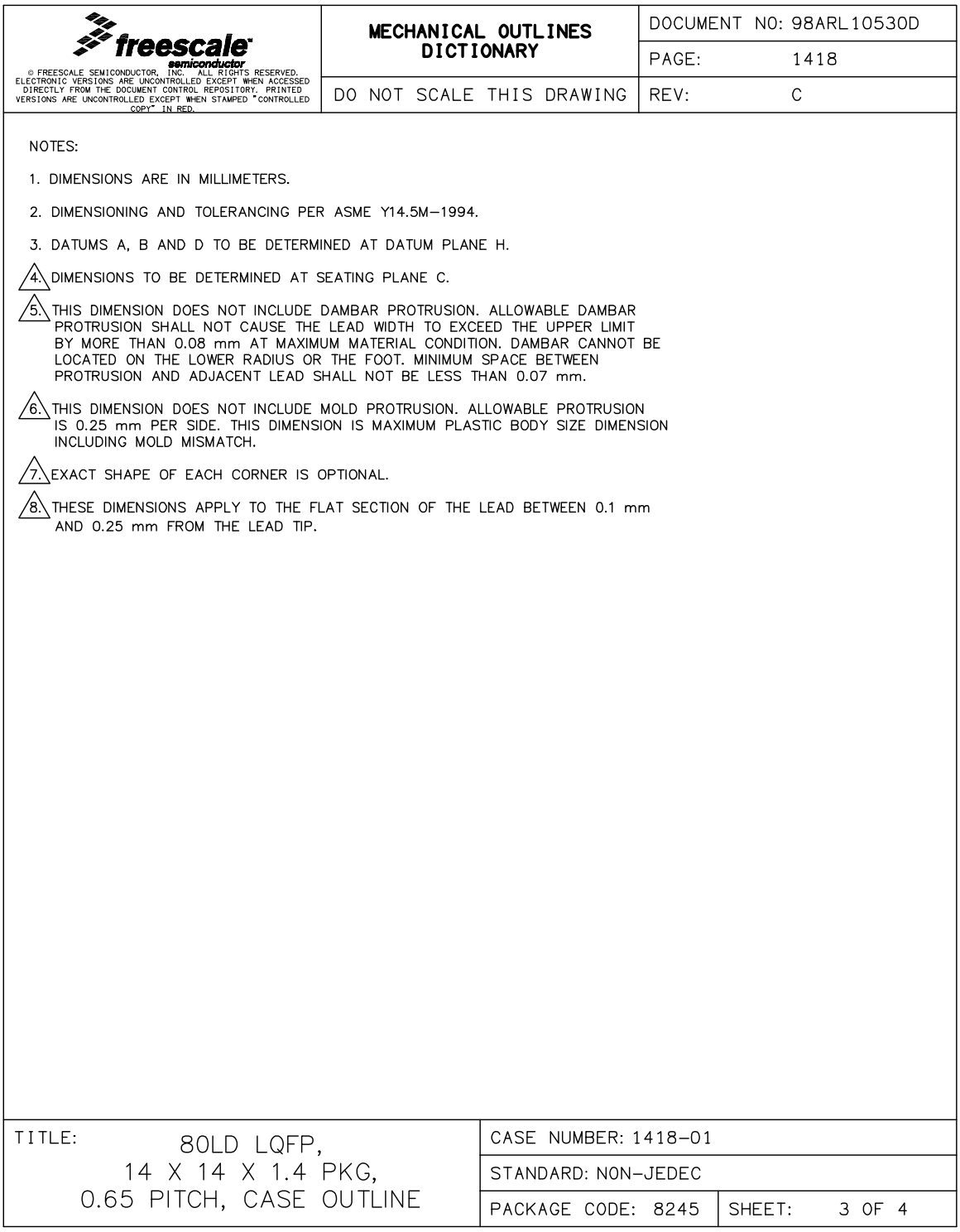


Figure 19. 80-pin LQFP Diagram - II



freescale semiconductor

MECHANICAL OUTLINES DICTIONARY

DOCUMENT NO: 98ARL10530D

PAGE: 1418

DO NOT SCALE THIS DRAWING

REV: C

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

TITLE: 80LD LQFP, 14 X 14 X 1.4 PKG, 0.65 PITCH, CASE OUTLINE

CASE NUMBER: 1418–01

STANDARD: NON–JEDEC

PACKAGE CODE: 8245

SHEET: 3 OF 4

Figure 20. 80-pin LQFP Diagram - III

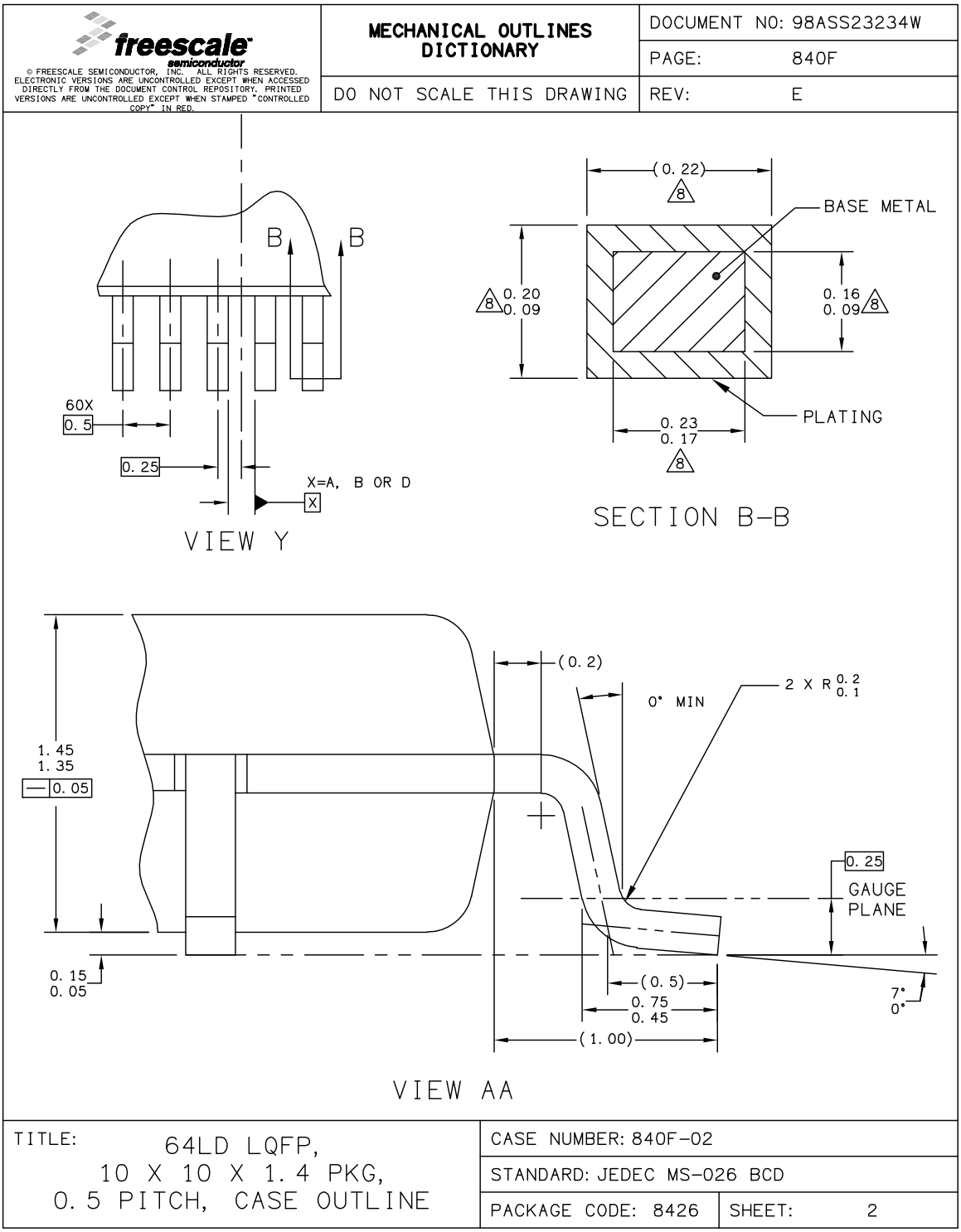


Figure 22. 64-pin LQFP Diagram - II

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23234W
		PAGE: 840F
	DO NOT SCALE THIS DRAWING	REV: E

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	CASE NUMBER: 840F–02	
	STANDARD: JEDEC MS–026 BCD	
	PACKAGE CODE: 8426	SHEET: 3

Figure 23. 64-pin LQFP Diagram - III

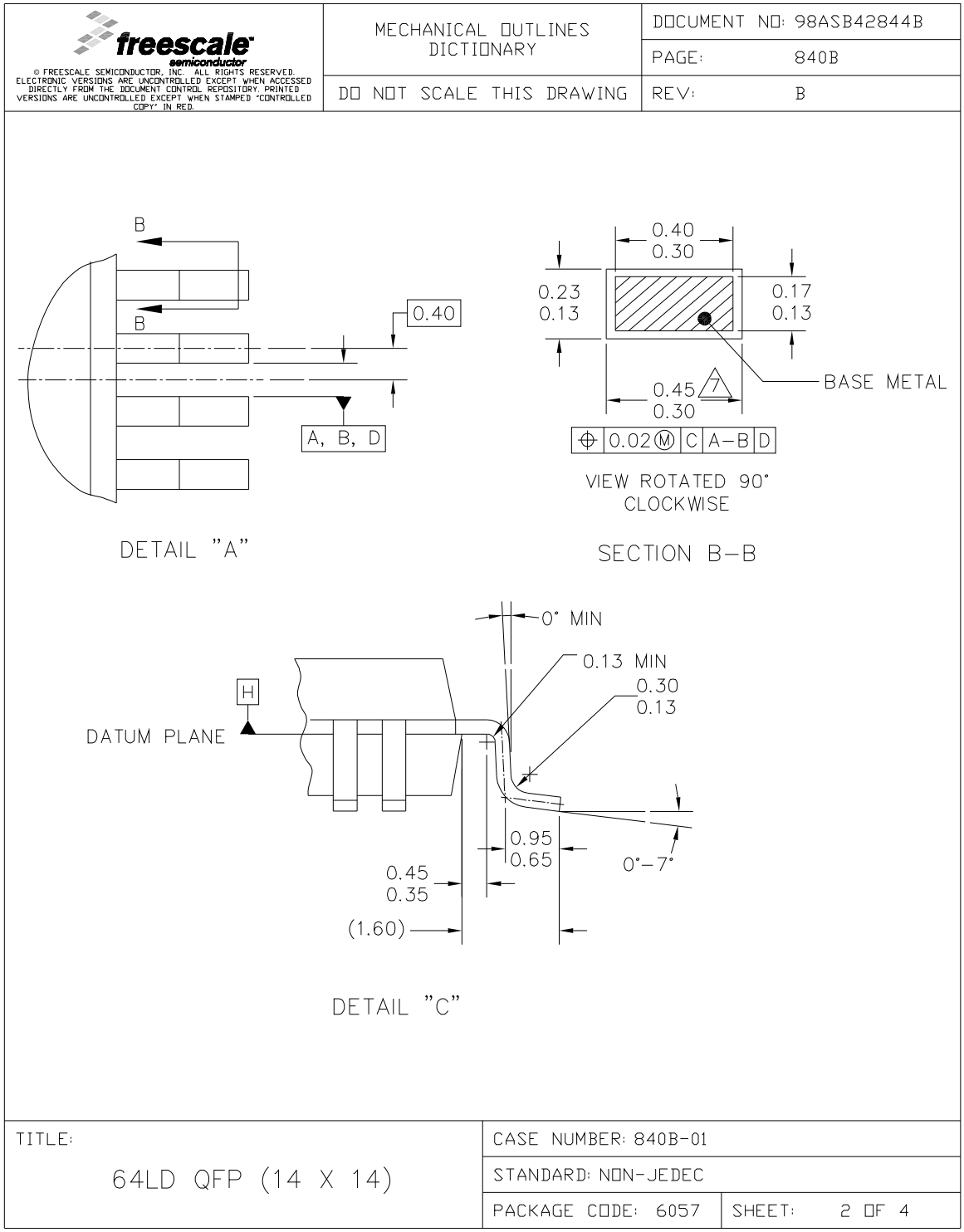


Figure 25. 64-pin QFP Diagram - II

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASB42844B
		PAGE: 840B
	DO NOT SCALE THIS DRAWING	REV: B

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE −H− IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A−B AND −D− TO BE DETERMINED AT DATUM PLANE −H−.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE −C−.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE −H−.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDICTION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

TITLE: 64LD QFP (14 X 14)	CASE NUMBER: 840B−01	
	STANDARD: NON−JEDEC	
	PACKAGE CODE: 6057	SHEET: 3 OF 4

Figure 26. 64-pin QFP Diagram - III