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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, I²C, SCI, SPI, USB OTG
Peripherals	LVD, PWM, WDT
Number of I/O	66
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/pcf51jm64evlk

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1 MCF51JM128 Family Configurations

1.1 Device Comparison

The MCF51JM128 series consists of the devices compared in Table 1.

Table 1. MCF51JM128 Series Device Comparison

Feature	MCF51JM128			MCF51JM64			MCF51JM32		
	80-pin	64-pin	44-pin	80-pin	64-pin	44-pin	80-pin	64-pin	44-pin
Flash memory size (KB)	128			64			32		
RAM size (KB)	16			16			16		
V1 ColdFire core with BDM (background debug module)	Yes								
ACMP (analog comparator)	Yes								
ADC channels (12-bit)	12		8	12		8	12		8
CAN (controller area network)	Yes	Yes	No	Yes	Yes	No	Yes	Yes	No
RNGA + CAU	Yes[1]								
CMT (carrier modulator timer)	Yes								
COP (computer operating properly)	Yes								
IIC1 (inter-integrated circuit)	Yes								
IIC2	Yes	No		Yes	No		Yes	No	
IRQ (interrupt request input)	Yes								
KBI (keyboard interrupts)	8	8	6	8	8	6	8	8	6
LVD (low-voltage detector)	Yes								
MCG (multipurpose clock generator)	Yes								
Port I/O[2]	66	51	33	66	51	33	66	51	33
RGPIO (rapid general-purpose I/O)	16	6	0	16	6	0	16	6	0
RTC (real-time counter)	Yes								
SCI1 (serial communications interface)	Yes								
SCI2	Yes								
SPI1 (serial peripheral interface)	Yes								
SPI2	Yes								
TPM1 (timer/pulse-width modulator) channels	6	6	4	6	6	4	6	6	4
TPM2 channels	2								
USBOTG (USB On-The-Go dual-role controller)	Yes								
XOSC (crystal oscillator)	Yes								

[1] Only existed on special part number

1.3 Features

Table 2 describes the functional units of the MCF51JM128 series.

Table 2. MCF51JM128 Series Functional Units

Unit	Function
CF1CORE (V1 ColdFire core)	Executes programs and interrupt handlers
BDM (background debug module)	Provides a single-pin debugging interface (part of the V1 ColdFire core)
DBG (debug)	Provides debugging and emulation capabilities (part of the V1 ColdFire core)
SYSCTL (system control)	Provides LVD, COP, external interrupt request, and so on
FLASH (flash memory)	Provides storage for program code and constants
RAM (random-access memory)	Provides storage for program code, constants, and variables
RGPIO (rapid general-purpose input/output)	Allows I/O port access at CPU clock speeds
VREG (voltage regulator)	Controls power management throughout the device
USBOTG (USB On-The-Go)	Supports the USB On-The-Go dual-role controller
ADC (analog-to-digital converter)	Measures analog voltages at up to 12 bits of resolution
TPM1, TPM2 (timer/pulse-width modulators)	Provide a variety of timing-based features
CF1_INTC (interrupt controller)	Controls and prioritizes all device interrupts
CAU (cryptographic acceleration unit)	Co-processor support for DES, 3DES, AES, MD5, and SHA-1
RNGA (random number generator accelerator)	32-bit random number generator that complies with FIPS-140
RTC (real-time counter)	Provides a constant-time base with optional interrupt
ACMP (analog comparator)	Compares two analog inputs
CMT (carrier modulator timer)	Infrared output used for the Remote Controller
IIC1, IIC2 (inter-integrated circuits)	Supports the standard IIC communications protocol
KBI (keyboard interrupt)	Provides pin interrupt capabilities
MCG (multipurpose clock generator)	Provides clocking options for the device, including a phase-locked loop (PLL) and frequency-locked loop (FLL) for multiplying slower reference clock sources
XOSC (crystal oscillator)	Supports low/high range crystals
CAN (controller area network)	Supports standard CAN communications protocol
SCI1, SCI2 (serial communications interfaces)	Serial communications UARTs that can support RS-232 and LIN protocols
SPI1, SPI2 (serial peripheral interfaces)	Provide a 4-pin synchronous serial interface

- RTC
  - — 8-bit modulus counter with binary- or decimal-based prescaler
  - — External clock source for precise time base, time-of-day, calendar or task scheduling functions
  - — Free running on-chip low power oscillator (1 kHz) for cyclic wake-up without external components
- Carrier modulator timer (CMT)
  - — carrier generator, modulator, and transmitter drive the infrared out (IRO) pin
  - — operation in independent high/low time control, baseband, FSK, and direct IRO control modes
- Input/Output
  - — 66 GPIOs
  - — Eight keyboard interrupt pins with selectable polarity
  - — Hysteresis and configurable pull-up device on all input pins; configurable slew rate and drive strength on all output pins
  - — 16 bits of Rapid GPIO connected to the processor's local 32-bit platform bus with set, clear, and faster toggle functionality

1.4 Part Numbers

Table 3. Orderable Part Number Summary

Freescale Part Number	Description	Flash / SRAM (KB)	Package	Temperature
MCF51JM128EVLK	MCF51JM128 ColdFire Microcontroller with CAU and RNGA Enabled	128 / 16	80 LQFP	–40 to +105 °C
MCF51JM128VLK	MCF51JM128 ColdFire Microcontroller	128 / 16	80 LQFP	–40 to +105 °C
MCF51JM128EVLH	MCF51JM128 ColdFire Microcontroller with CAU and RNGA Enabled	128 / 16	64 LQFP	–40 to +105 °C
MCF51JM128VLH	MCF51JM128 ColdFire Microcontroller	128 / 16	64 LQFP	–40 to +105 °C
MCF51JM128EVQH	MCF51JM128 ColdFire Microcontroller with CAU and RNGA Enabled	128 / 16	64 QFP	–40 to +105 °C
MCF51JM128VQH	MCF51JM128 ColdFire Microcontroller	128 / 16	64 QFP	–40 to +105 °C
MCF51JM128EVLD	MCF51JM128 ColdFire Microcontroller with CAU and RNGA Enabled	128 / 16	44 LQFP	–40 to +105 °C
MCF51JM128VLD	MCF51JM128 ColdFire Microcontroller	128 / 16	44 LQFP	–40 to +105 °C
MCF51JM64EVLK	MCF51JM64 ColdFire Microcontroller with CAU and RNGA Enabled	64 / 16	80 LQFP	–40 to +105 °C
MCF51JM64VLK	MCF51JM64 ColdFire Microcontroller	64 / 16	80 LQFP	–40 to +105 °C
MCF51JM64EVLH	MCF51JM64 ColdFire Microcontroller with CAU and RNGA Enabled	64 / 16	64 LQFP	–40 to +105 °C
MCF51JM64VLH	MCF51JM64 ColdFire Microcontroller	64 / 16	64 LQFP	–40 to +105 °C
MCF51JM64EVQH	MCF51JM64 ColdFire Microcontroller with CAU and RNGA Enabled	64 / 16	64 QFP	–40 to +105 °C
MCF51JM64VQH	MCF51JM64 ColdFire Microcontroller	64 / 16	64 QFP	–40 to +105 °C

Figure 3 shows the pinout of the 64-pin LQFP and QFP.

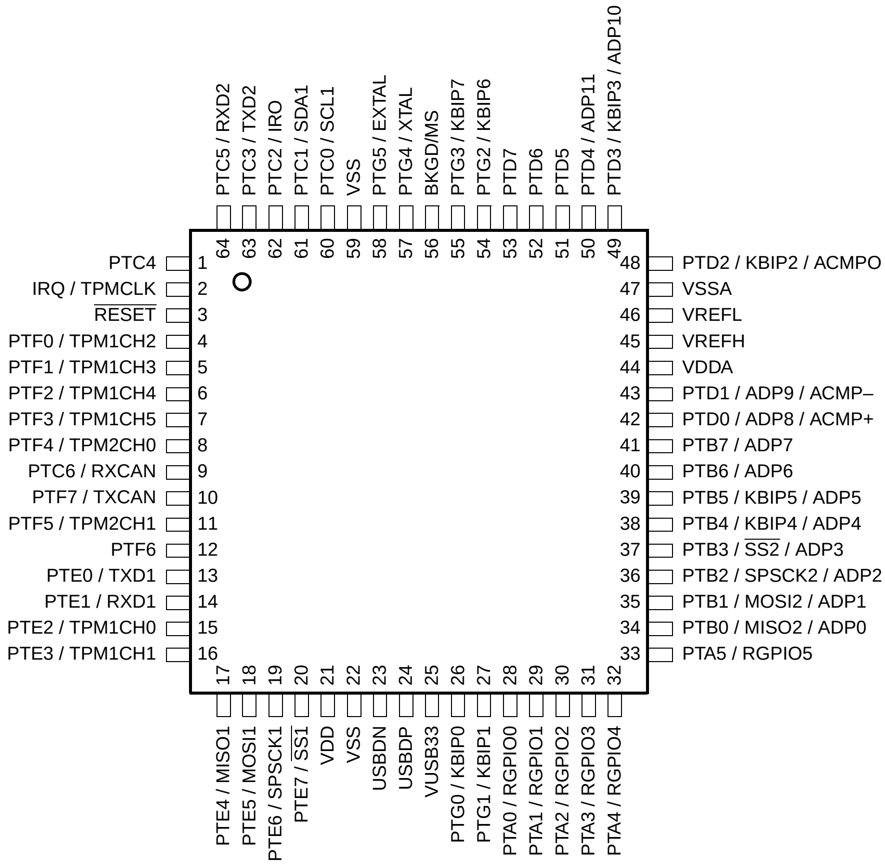

Figure 3. 64-pin QFP and LQFP

2 Preliminary Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MCF51JM128 microcontroller, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 5. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled C in the parameter tables where appropriate.

2.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 6 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, V_{SS} or V_{DD}).

[3] 1s - Single Layer Board, one signal layer
[4] 2s2p - Four Layer Board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °Cθ_{JA} = Package thermal resistance, junction-to-ambient, °C/WP_D = P_{int} + $P_{I/O}$$P_{int}$ = $I_{DD} \times V_{DD}$, Watts — chip internal power$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations 1 and 2 iteratively for any value of T_A.

2.4 Electrostatic Discharge (ESD) Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (http://www.aecouncil.com/) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 8. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulse per pin	–	3	
Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table 10. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typ[1]	Max	Unit
7	P	Input low voltage; all digital inputs V_{DD} = 5V V_{DD} = 3V	V_{IL}	—	—	1.75 1.05	V
8	P	Input hysteresis; all digital inputs	V_{hys}	0.06 x V_{DD}			mV
9	P	Input leakage current; input only pins[3]	$\|I_{In}\|$	—	0.1	1	μA
10	P	High Impedance (off-state) leakage current[3]	$\|I_{OZ}\|$	—	0.1	1	μA
11	P	Internal pullup resistors[4]	R_{PU}	20	45	65	kΩ
12	P	Internal pulldown resistors[5]	R_{PD}	20	45	65	kΩ
13		Internal pullup resistor to USBDP (to V_{USB33}) Idle Transmit	R_{PUPD}	900 1425	1300 2400	1575 3090	kΩ
14	C	Input Capacitance; all non-supply pins	C_{In}	—	—	8	pF
15	D	RAM retention voltage[6]	V_{RAM}	—	0.6	1.0	V
16	P	POR rearm voltage	V_{POR}	0.9	1.4	2.0	V
17	D	POR rearm time	t_{POR}	10	—	—	μs
18	P	Low-voltage detection threshold — high range V_{DD} falling V_{DD} rising	V_{LVD1}	3.9 4.0	4.0 4.1	4.1 4.2	V
19	P	Low-voltage detection threshold — low range V_{DD} falling V_{DD} rising	V_{LVD0}	2.48 2.54	2.56 2.62	2.64 2.70	V
20	C	Low-voltage warning threshold — high range 1 V_{DD} falling V_{DD} rising	V_{LVW3}	4.5 4.6	4.6 4.7	4.7 4.8	V
21	P	Low-voltage warning threshold — high range 0 V_{DD} falling V_{DD} rising	V_{LVW2}	4.2 4.3	4.3 4.4	4.4 4.5	V
22	P	Low-voltage warning threshold low range 1 V_{DD} falling V_{DD} rising	V_{LVW1}	2.84 2.90	2.92 2.98	3.00 3.06	V
23	C	Low-voltage warning threshold — low range 0 V_{DD} falling V_{DD} rising	V_{LVW0}	2.66 2.72	2.74 2.80	2.82 2.88	V
24	T	Low-voltage inhibit reset/recover hysteresis 5 V 3 V	V_{hys}	— —	100 60	— —	mV

2.7 Analog Comparator (ACMP) Electricals

Table 12. Analog Comparator Electrical Specifications

Num	C	Rating	Symbol	Min	Typical	Max	Unit
1		Supply voltage	V_{DD}	2.7	—	5.5	V
2		Supply current (active)	I_{DDAC}	—	20	35	µA
3		Analog input voltage	V_{AIN}	$V_{SS} - 0.3$	—	V_{DD}	V
4		Analog input offset voltage	V_{AIO}		20	40	mV
5		Analog Comparator hysteresis	V_H	3.0	6.0	20.0	mV
6		Analog input leakage current	I_{ALKG}	--	--	1.0	µA
7		Analog Comparator initialization delay	t_{AINIT}	—	—	1.0	µs
8		Bandgap Voltage Reference Factory trimmed at V_{DD} = 3.0 V, Temp = 25°C	V_{BG}	1.19	1.20	1.21	V

2.8 ADC Characteristics

Table 13. 5 Volt 12-bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	
	Delta to V_{DD} (V_{DD}-V_{DDA})[2]	ΔV_{DDA}	–100	0	+100	mV	
Ground voltage	Delta to V_{SS} (V_{SS}-V_{SSA})[2]	ΔV_{SSA}	–100	0	+100	mV	
Ref Voltage High		V_{REFH}	2.7	V_{DDA}	V_{DDA}	V	
Ref Voltage Low		V_{REFL}	V_{SSA}	V_{SSA}	V_{SSA}	V	
Input Voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
Input Capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input Resistance		R_{ADIN}	—	3	5	kΩ	
Analog Source Resistance	12 bit mode $f_{ADCK} > 4$MHz $f_{ADCK} < 4$MHz	R_{AS}	 — —	 — —	 2 5	kΩ	External to MCU
	10 bit mode $f_{ADCK} > 4$MHz $f_{ADCK} < 4$MHz		 — —	 — —	 5 10		
	8 bit mode (all valid f_{ADCK})		—	—	10		
ADC Conversion Clock Freq.	High Speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	
	Low Power (ADLPC=1)		0.4	—	4.0		

1 Typical values assume V_{DDA} = 5.0V, Temp = 25°C, f_{ADCK}=1.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

Table 14. 5 Volt 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Comment
Conversion Time (Including sample time)	Short Sample (ADLSMP=0)	T	t_{ADC}	—	20	—	ADCK cycles	See Table 9 for conversion time variances
	Long Sample (ADLSMP=1)			—	40	—		
Sample Time	Short Sample (ADLSMP=0)	T	t_{ADS}	—	3.5	—	ADCK cycles	
	Long Sample (ADLSMP=1)			—	23.5	—		
Total Unadjusted Error	12 bit mode	T	E_{TUE}	—	±3.0	—	LSB[2]	Includes quantization
	10 bit mode	P		—	±1	±2.5		
	8 bit mode	T		—	±0.5	±1.0		
Differential Non-Linearity	12 bit mode	T	DNL	—	±1.75	—	LSB[2]	
	10 bit mode[3]	P		—	±0.5	±1.0		
	8 bit mode[3]	T		—	±0.3	±0.5		
Integral Non-Linearity	12 bit mode	T	INL	—	±1.5	—	LSB[2]	
	10 bit mode	T		—	±0.5	±1.0		
	8 bit mode	T		—	±0.3	±0.5		
Zero-Scale Error	12 bit mode	T	E_{ZS}	—	±1.5	—	LSB[2]	$V_{ADIN} = V_{SSAD}$
	10 bit mode	P		—	±0.5	±1.5		
	8 bit mode	T		—	±0.5	±0.5		
Full-Scale Error	12 bit mode	T	E_{FS}	—	±1	—	LSB[2]	$V_{ADIN} = V_{DDAD}$
	10 bit mode	T		—	±0.5	±1		
	8 bit mode	T		—	±0.5	±0.5		
Quantization Error	12 bit mode	D	E_Q	—	-1 to 0	—	LSB[2]	
	10 bit mode			—	—	±0.5		
	8 bit mode			—	—	±0.5		
Input Leakage Error	12 bit mode	D	E_{IL}	—	±1	—	LSB[2]	Pad leakage[4] * R_{AS}
	10 bit mode			—	±0.2	±2.5		
	8 bit mode			—	±0.1	±1		
Temp Sensor Voltage	25°C	D	V_{TEMP25}	—	1.396	—	V	
Temp Sensor Slope	-40°C - 25°C	D	m	—	3.266	—	mV/°C	
	25°C - 125°C			—	3.638	—		

1 Typical values assume V_{DDA} = 5.0V, Temp = 25°C, f_{ADCK}=1.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Monotonicity and No-Missing-Codes guaranteed in 10 bit and 8 bit modes

4 Based on input pad leakage current. Refer to pad electricals.

2.9 External Oscillator (XOSC) Characteristics

Table 15. Oscillator Electrical Specifications (Temperature Range = –40 to 105°C Ambient)

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
1		Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) • Low range (RANGE = 0) • High range (RANGE = 1) FEE or FBE mode [2] • High range (RANGE = 1) PEE or PBE mode [3] • High range (RANGE = 1, HGO = 1) BLPE mode • High range (RANGE = 1, HGO = 0) BLPE mode	f_{lo} $f_{hi\text{-}fll}$ $f_{hi\text{-}pll}$ $f_{hi\text{-}hgo}$ $f_{hi\text{-}lp}$	32 1 1 1 1	— — — — —	38.4 5 16 16 8	kHz MHz MHz MHz MHz
2		Load capacitors	C_1 C_2	See crystal or resonator manufacturer's recommendation.			
3		Feedback resistor • Low range (32 kHz to 38.4 kHz) • High range (1 MHz to 16 MHz)	R_F		10 1		MΩ MΩ
4	—	Series resistor • Low range, low gain (RANGE = 0, HGO = 0) • Low range, high gain (RANGE = 0, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz • High range, low gain (RANGE = 1, HGO = 0) • High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	— — — — — —	0 100 0 0 0 0	— — — 0 10 20	kΩ
5	T	Crystal start-up time [4] • Low range, low gain (RANGE = 0, HGO = 0) • Low range, high gain (RANGE = 0, HGO = 1) • High range, low gain (RANGE = 1, HG0 = 0)[5] • High range, high gain (RANGE = 1, HG0 = 1)[5]	$t_{CSTL\text{-}LP}$ $t_{CSTL\text{-}HGO}$ $t_{CSTH\text{-}LP}$ $t_{CSTH\text{-}HGO}$	— — — —	200 400 5 15	— — — —	ms
6	T	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) • FEE or FBE mode [2] • PEE or PBE mode [3] • BLPE mode	f_{extal}	0.03125 1 0	— — —	5 16 40	MHz MHz MHz

[1] Data in Typical column was characterized at 5.0 V, 25°C or is typical recommended value.

[2] When MCG is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

[3] When MCG is configured for PEE or PBE mode, input clock source must be divisible using RDIV to within the range of 1 MHz to 2 MHz.

[4] This parameter is characterized and not tested on each device. Proper PC board-layout procedures must be followed to achieve specifications.

[5] 4 MHz crystal

2.10 MCG Specifications

Table 16. MCG Frequency Specifications (Temperature Range = –40 to 125°C Ambient)

Num	C	Rating		Symbol	Min	Typical[1]	Max	Unit
1	P	Internal reference frequency - factory trimmed at V_{DD} = 5 V and temperature = 25 °C		f_{int_ft}	—	32.768	—	kHz
2	P	Average internal reference frequency – untrimmed		f_{int_ut}	31.25	—	39.0625	kHz
3	T	Internal reference startup time		t_{irefst}	—	60	100	µs
4	P	DCO output frequency range - untrimmed [2]	Low range (DRS=00)	f_{dco_ut}	16	—	20	MHz
	P		Mid range (DRS=01)		32	—	40	
	P		High range (DRS=10)		48	—	60	
5	P	DCO output frequency[2] Reference =32768Hz and DMX32 = 1	Low range (DRS=00)	f_{dco_DMX32}	—	19.92	—	MHz
	P		Mid range (DRS=01)		—	39.85	—	
	P		High range (DRS=10)		—	59.77	—	
6	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
7	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	$\%f_{dco}$
8	D	Total deviation of trimmed DCO output frequency over voltage and temperature		Δf_{dco_t}	—	0.5 –1.0	±2	$\%f_{dco}$
9	D	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 – 70 °C		Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$
10	D	FLL acquisition time [3]		$t_{fll\_acquire}$	—	—	1	ms
11	D	PLL acquisition time [4]		$t_{pll\_acquire}$	—	—	1	ms
12	D	Long term Jitter of DCO output clock (averaged over 2ms interval) [5]		C_{Jitter}	—	0.02	0.2	$\%f_{dco}$
13	D	VCO operating frequency		f_{vco}	7.0	—	55.0	MHz
14	D	Jitter of PLL output clock measured over 625 ns[6]		$f_{pll\_jitter\_625ns}$	—	0.566[5]	—	$\%f_{pll}$
15	D	Lock entry frequency tolerance [7]		D_{lock}	±1.49	—	±2.98	%
16	D	Lock exit frequency tolerance [8]		D_{unl}	±4.47	—	±5.97	%
17	D	Lock time — FLL		t_{fll_lock}	—	—	$t_{fll\_acquire}$+ 1075(1/f_{int_t})	s
18	D	Lock time — PLL		t_{pll_lock}	—	—	$t_{pll\_acquire}$+ 1075(1/f_{pll_ref})	s
19	D	Loss of external clock minimum frequency – RANGE = 0		f_{loc_low}	(3/5) x f_{int}	—	—	kHz

1 Data in Typical column was characterized at 5.0 V, 25C or is typical recommended value

2 The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

3 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

5 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

6 625 ns represents 5 time quanta for CAN applications, under worst case conditions of 8 MHz CAN bus clock, 1 Mbps CAN bus speed, and 8 time quanta per bit for bit time settings. 5 time quanta is the minimum time between a synchronization edge and the sample point of a bit using 8 time quanta per bit.

7 Below D_{lock} minimum, the MCG is guaranteed to enter lock. Above D_{lock} maximum, the MCG will not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.

8 Below D_{unl} minimum, the MCG will not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.

2.11 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

2.11.1 Control Timing

Table 17. Control Timing

Num	C	Parameter	Symbol	Min	Typ[1]	Max	Unit
1		Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	dc	—	24	MHz
2		Internal low-power oscillator period	t_{LPO}	700		1300	µs
3		External reset pulse width[2] ($t_{cyc} = 1/f_{Self\_reset}$)	t_{extrst}	100		—	ns
4		Reset low drive	t_{rstdrv}	66 x t_{cyc}		—	ns
5		Active background debug mode latch setup time	t_{MSSU}	500		—	ns
6		Active background debug mode latch hold time	t_{MSH}	100		—	ns
7		IRQ pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}, t_{IHIL}	100 1.5 x t_{cyc}	—	—	ns
8		KBIPx pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}, t_{IHIL}	100 1.5 x t_{cyc}	—	—	ns
9		Port rise and fall time (load = 50 pF)[4] Slew rate control disabled (PTxSE = 0) High drive Slew rate control enabled (PTxSE = 1) High drive Slew rate control disabled (PTxSE = 0) Low drive Slew rate control enabled (PTxSE = 1) Low drive	t_{Rise}, t_{Fall}	— —	11 35 40 75		ns

1 Typical values are based on characterization data at V_{DD} = 5.0V, 25°C unless otherwise stated.

2 This is the shortest pulse guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

3 This is the minimum pulse width guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

4 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 105°C.

2.12 SPI Characteristics

Table 20 and Figure 14 through Figure 17 describe the timing requirements for the SPI system.

Table 20. SPI Timing

No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	$f_{Bus}/2048$ 0	$f_{Bus}/2$ $f_{Bus}/4$	Hz
1	D	SPSCK period Master Slave	t_{SPSCK}	2 4	2048 —	t_{cyc} t_{cyc}
2	D	Enable lead time Master Slave	t_{Lead}	1/2 1	— —	t_{SPSCK} t_{cyc}
3	D	Enable lag time Master Slave	t_{Lag}	1/2 1	— —	t_{SPSCK} t_{cyc}
4	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	$t_{cyc} – 30$ $t_{cyc} – 30$	1024 t_{cyc} —	ns ns
5	D	Data setup time (inputs) Master Slave	t_{SU}	15 15	— —	ns ns
6	D	Data hold time (inputs) Master Slave	t_{HI}	0 25	— —	ns ns
7	D	Slave access time	t_a	—	1	t_{cyc}
8	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
9	D	Data valid (after SPSCK edge) Master Slave	t_v	— —	25 25	ns ns
10	D	Data hold time (outputs) Master Slave	t_{HO}	0 0	— —	ns ns
11	D	Rise time Input Output	t_{RI} t_{RO}	— —	$t_{cyc} – 25$ 25	ns ns
12	D	Fall time Input Output	t_{FI} t_{FO}	— —	$t_{cyc} – 25$ 25	ns ns

Table 22. Internal USB 3.3V Voltage Regulator Characteristics

	Symbol	Unit	Min	Typ	Max
Regulator operating voltage	V_{regin}	V	3.9	—	5.5
Vreg output	V_{regout}	V	3	3.3	3.6
Vusb33 input with internal Vreg disabled	$V_{usb33in}$	V	3	3.3	3.6
VREG Quiescent Current	I_{VRQ}	mA	—	0.5	—

2.15 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

2.15.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East). For more detailed information concerning the evaluation results, conditions and setup, please refer to the EMC Evaluation Report for this device.

3 Mechanical Outline Drawings

3.1 80-pin LQFP

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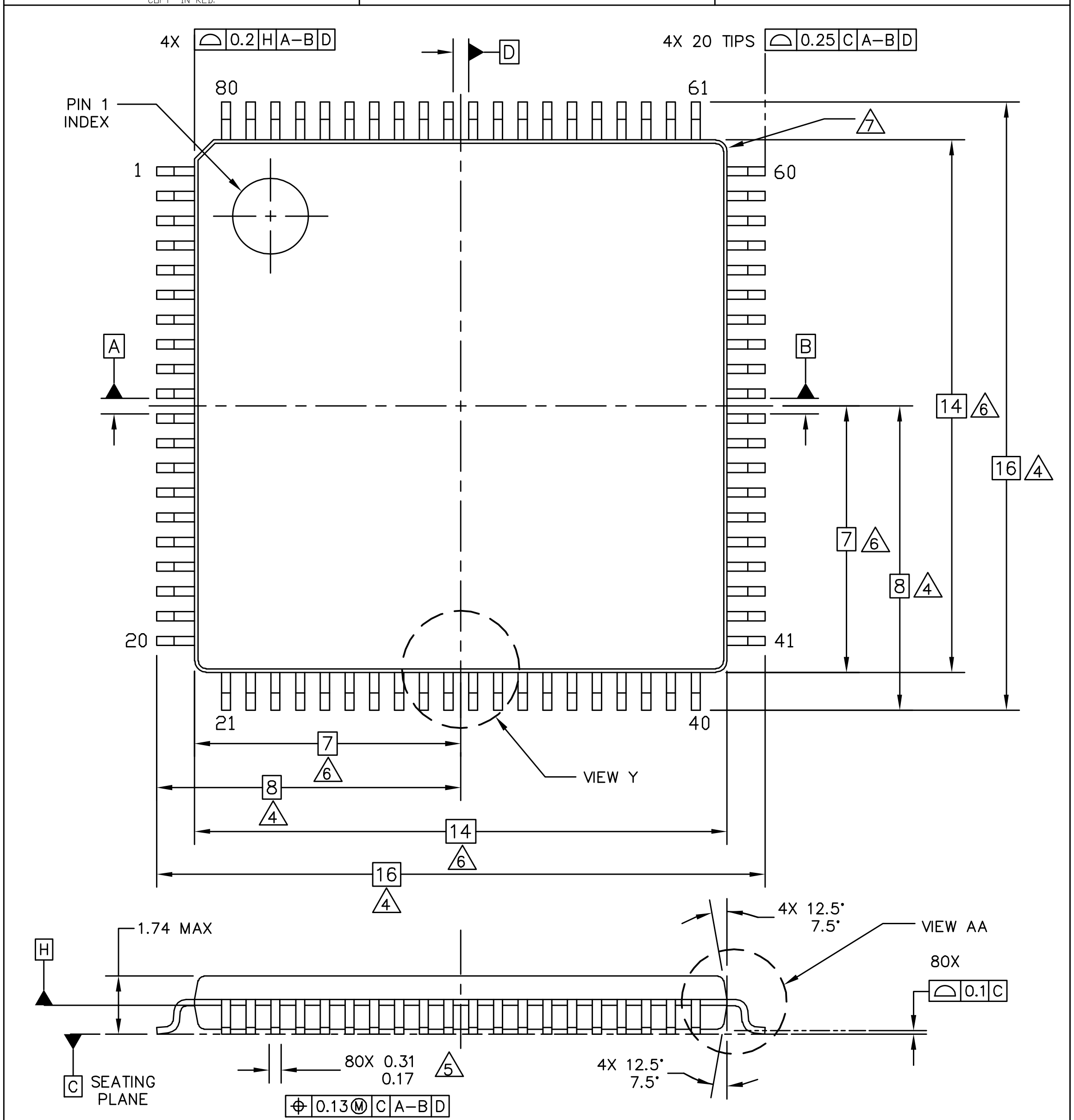
		PAGE: 1418
	DO NOT SCALE THIS DRAWING	REV: C



TITLE: 80LD LQFP, 14 X 14 X 1.4 PKG, 0.65 PITCH, CASE OUTLINE	CASE NUMBER: 1418-01
	STANDARD: NON-JEDEC
	PACKAGE CODE: 8245 SHEET: 1 OF 4

Figure 18. 80-pin LQFP Diagram - I

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		PAGE: 1418
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NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M—1994.

3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.

4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.

5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.

6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.

7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

TITLE: 80LD LQFP, 14 X 14 X 1.4 PKG, 0.65 PITCH, CASE OUTLINE	CASE NUMBER: 1418-01	
	STANDARD: NON-JEDEC	
	PACKAGE CODE: 8245	SHEET: 3 OF 4

Figure 20. 80-pin LQFP Diagram - III

3.2 64-pin LQFP

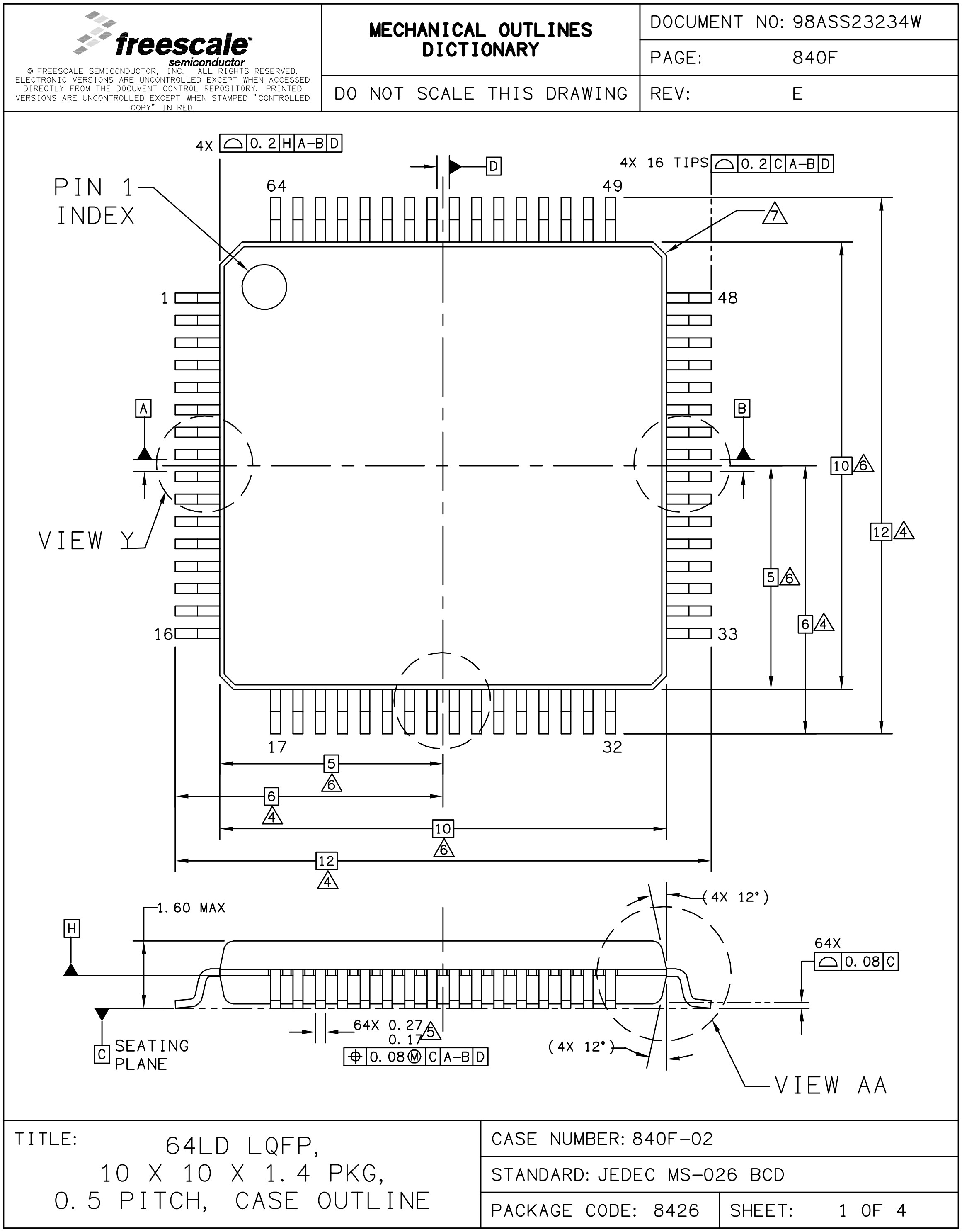


Figure 21. 64-pin LQFP Diagram - I

3.4 44-pin LQFP

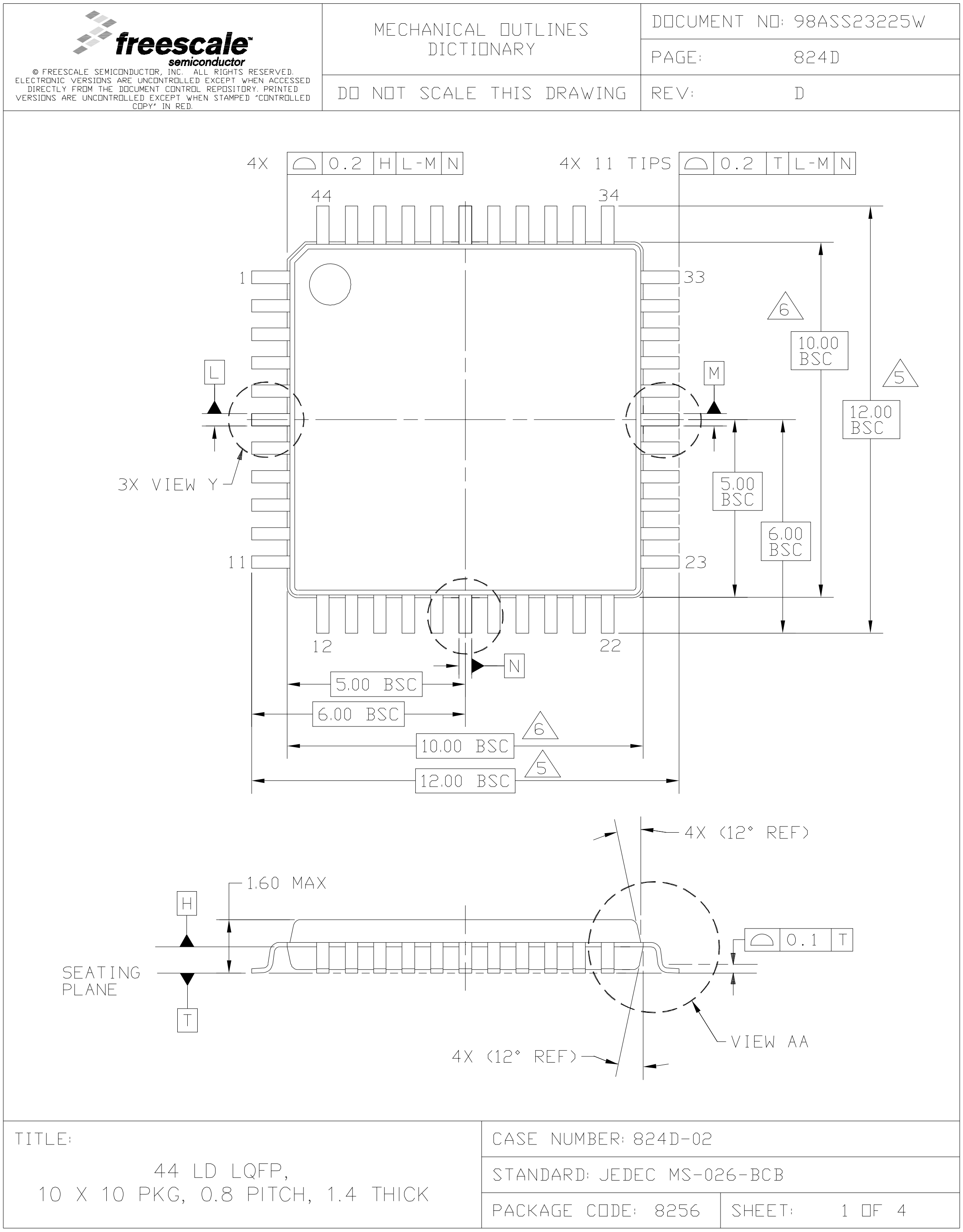
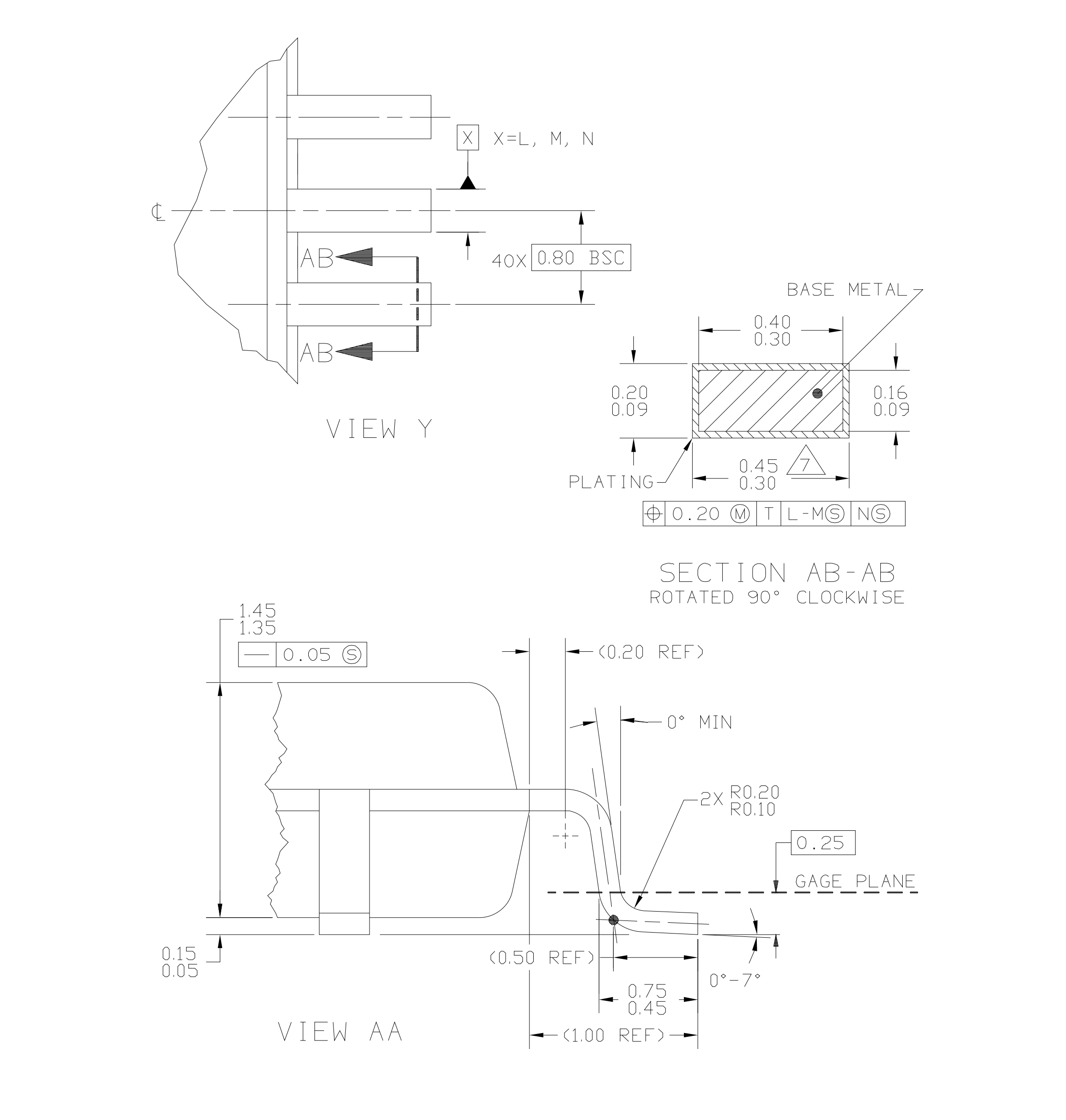


Figure 27. 44-pin LQFP Diagram - I

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23225W
		PAGE: 824D
	DO NOT SCALE THIS DRAWING	REV: D



TITLE: 44 LD LQFP, 10 X 10 PKG, 0.8 PITCH, 1.4 THICK	CASE NUMBER: 824D-02	
	STANDARD: JEDEC MS-026 BCB	
	PACKAGE CODE: 8256	SHEET: 2 OF 4

Figure 28. 44-pin LQFP Diagram - II