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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, I²C, SCI, SPI, USB OTG
Peripherals	LVD, PWM, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/pcf51jm64vlh

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[2] Up to 16 pins on Ports A, H, and J are shared with the ColdFire Rapid GPIO module.

1.2 Block Diagram

Figure 1 shows the connections between the MCF51JM128 series pins and modules.

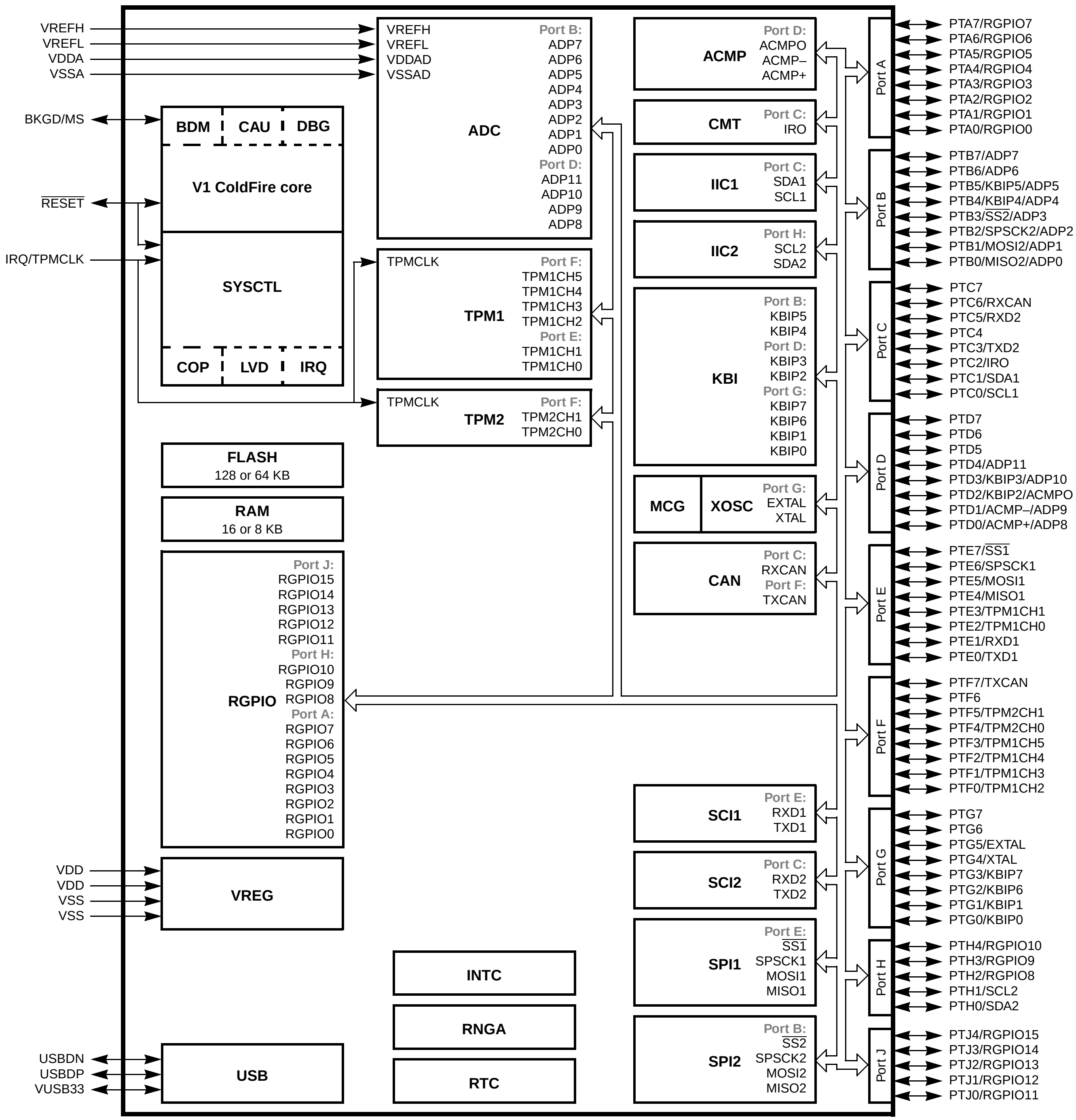


Figure 1. MCF51JM128 Block Diagram

- RTC
  - 8-bit modulus counter with binary- or decimal-based prescaler
  - External clock source for precise time base, time-of-day, calendar or task scheduling functions
  - Free running on-chip low power oscillator (1 kHz) for cyclic wake-up without external components
- Carrier modulator timer (CMT)
  - carrier generator, modulator, and transmitter drive the infrared out (IRO) pin
  - operation in independent high/low time control, baseband, FSK, and direct IRO control modes
- Input/Output
  - 66 GPIOs
  - Eight keyboard interrupt pins with selectable polarity
  - Hysteresis and configurable pull-up device on all input pins; configurable slew rate and drive strength on all output pins
  - 16 bits of Rapid GPIO connected to the processor's local 32-bit platform bus with set, clear, and faster toggle functionality

1.4 Part Numbers

Table 3. Orderable Part Number Summary

Freescale Part Number	Description	Flash / SRAM (KB)	Package	Temperature
MCF51JM128EVLK	MCF51JM128 ColdFire Microcontroller with CAU and RNGA Enabled	128 / 16	80 LQFP	–40 to +105 °C
MCF51JM128VLK	MCF51JM128 ColdFire Microcontroller	128 / 16	80 LQFP	–40 to +105 °C
MCF51JM128EVLH	MCF51JM128 ColdFire Microcontroller with CAU and RNGA Enabled	128 / 16	64 LQFP	–40 to +105 °C
MCF51JM128VLH	MCF51JM128 ColdFire Microcontroller	128 / 16	64 LQFP	–40 to +105 °C
MCF51JM128EVQH	MCF51JM128 ColdFire Microcontroller with CAU and RNGA Enabled	128 / 16	64 QFP	–40 to +105 °C
MCF51JM128VQH	MCF51JM128 ColdFire Microcontroller	128 / 16	64 QFP	–40 to +105 °C
MCF51JM128EVLD	MCF51JM128 ColdFire Microcontroller with CAU and RNGA Enabled	128 / 16	44 LQFP	–40 to +105 °C
MCF51JM128VLD	MCF51JM128 ColdFire Microcontroller	128 / 16	44 LQFP	–40 to +105 °C
MCF51JM64EVLK	MCF51JM64 ColdFire Microcontroller with CAU and RNGA Enabled	64 / 16	80 LQFP	–40 to +105 °C
MCF51JM64VLK	MCF51JM64 ColdFire Microcontroller	64 / 16	80 LQFP	–40 to +105 °C
MCF51JM64EVLH	MCF51JM64 ColdFire Microcontroller with CAU and RNGA Enabled	64 / 16	64 LQFP	–40 to +105 °C
MCF51JM64VLH	MCF51JM64 ColdFire Microcontroller	64 / 16	64 LQFP	–40 to +105 °C
MCF51JM64EVQH	MCF51JM64 ColdFire Microcontroller with CAU and RNGA Enabled	64 / 16	64 QFP	–40 to +105 °C
MCF51JM64VQH	MCF51JM64 ColdFire Microcontroller	64 / 16	64 QFP	–40 to +105 °C

1.5 Pinouts and Packaging

Figure 2 shows the pinout of the 80-pin LQFP.

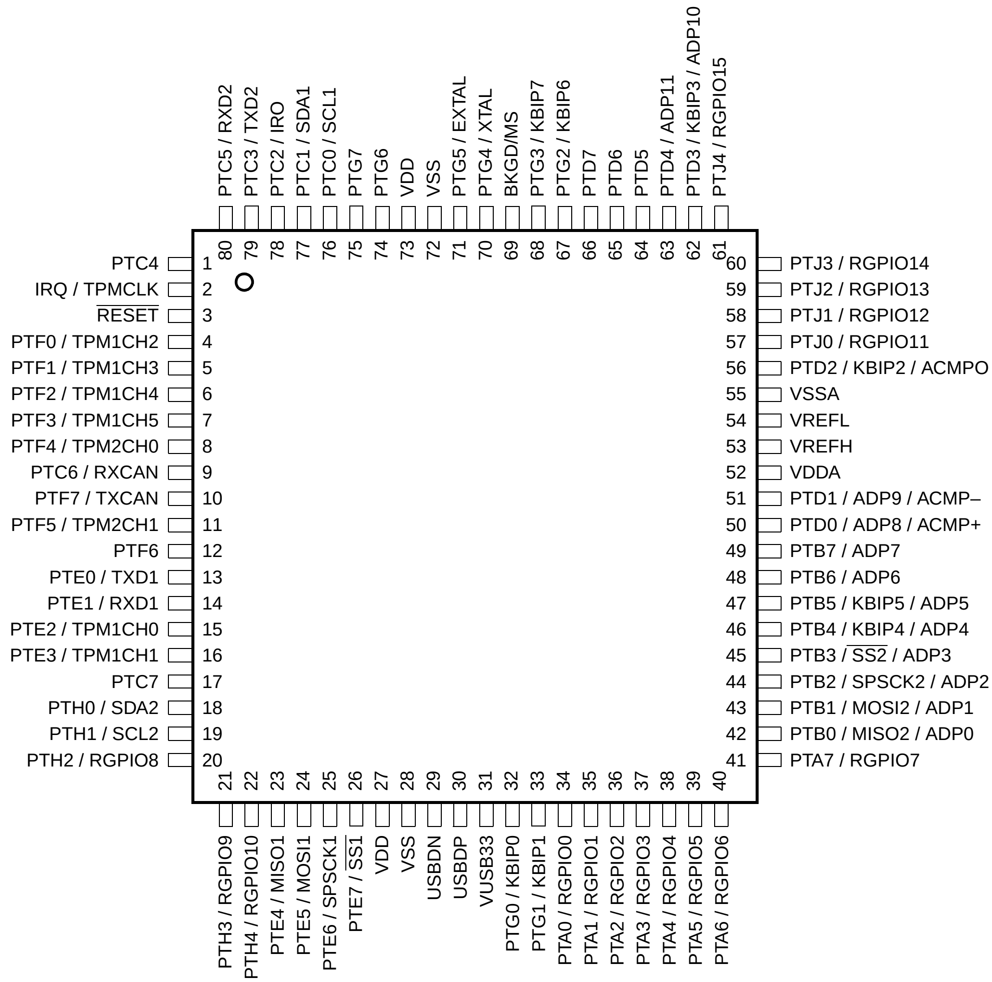


Figure 2. 80-pin LQFP

Figure 4 shows the pinout of the 44-pin LQFP.

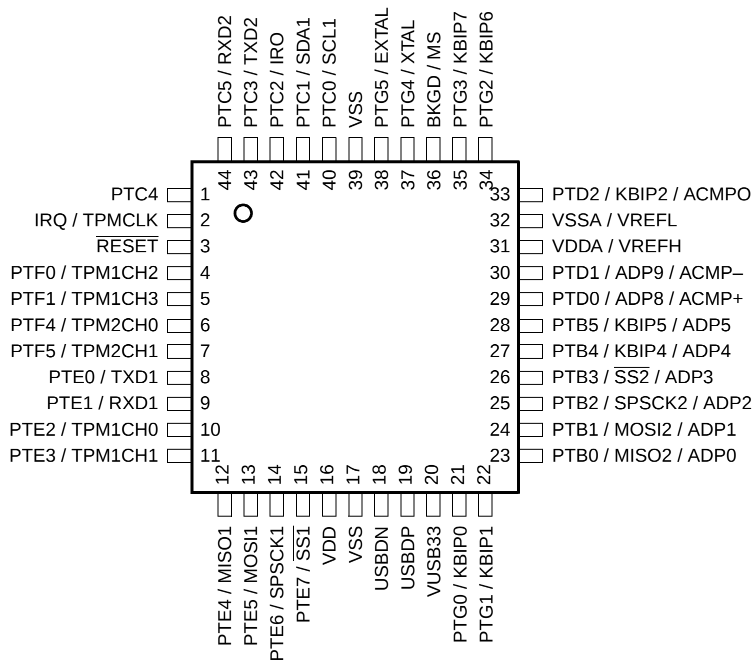


Figure 4. 44-pin LQFP

Table 4 shows the package pin assignments.

Table 4. Pin Assignments by Package and Pin Sharing Priority

Pin Number			<-- Lowest **Priority** --> Highest		
80	**64**	**44**	**Port Pin**	**Alt 1**	**Alt 2**
1	1	1	PTC4		—
2	2	2	—	IRQ	TPMCLK
3	3	3	—	$\overline{\text{RESET}}$	—
4	4	4	PTF0	TPM1CH2	—
5	5	5	PTF1	TPM1CH3	—
6	6	—	PTF2	TPM1CH4	—
7	7	—	PTF3	TPM1CH5	—
8	8	6	PTF4	TPM2CH0	BUSCLK_OUT
9	9	—	PTC6	RXCAN	—
10	10	—	PTF7	TXCAN	—
11	11	7	PTF5	TPM2CH1	—
12	12	—	PTF6	—	—
13	13	8	PTE0	TXD1	—
14	14	9	PTE1	RXD1	—
15	15	10	PTE2	TPM1CH0	—

Table 4. Pin Assignments by Package and Pin Sharing Priority (continued)

Pin Number			<-- Lowest **Priority** --> Highest		
80	**64**	**44**	**Port Pin**	**Alt 1**	**Alt 2**
16	16	11	PTE3	TPM1CH1	—
17	—	—	PTC7	—	—
18	—	—	PTH0	SDA2	—
19	—	—	PTH1	SCL2	—
20	—	—	PTH2	RGPIO8	—
21	—	—	PTH3	RGPIO9	—
22	—	—	PTH4	RGPIO10	—
23	17	12	PTE4	MISO1	—
24	18	13	PTE5	MOSI1	—
25	19	14	PTE6	SPSCK1	—
26	20	15	PTE7	$\overline{\text{SS1}}$	—
27	21	16	—	—	VDD
28	22	17	—	—	VSS
29	23	18	—	—	USBDN
30	24	19	—	—	USBDP
31	25	20	—	—	VUSB33
32	26	21	PTG0	KBIP0	USB_ALT_CLK
33	27	22	PTG1	KBIP1	—
34	28	—	PTA0	RGPIO0	USB_SESSVLD
35	29	—	PTA1	RGPIO1	USB_SESSEND
36	30	—	PTA2	RGPIO2	USB_VBUSVLD
37	31	—	PTA3	RGPIO3	USB_PULLUP(D+)
38	32	—	PTA4	RGPIO4	USB_DM_DOWN
39	33	—	PTA5	RGPIO5	USB_DP_DOWN
40	—	—	PTA6	RGPIO6	USB_ID
41	—	—	PTA7	RGPIO7	—
42	34	23	PTB0	MISO2	ADP0
43	35	24	PTB1	MOSI2	ADP1
44	36	25	PTB2	SPSCK2	ADP2
45	37	26	PTB3	$\overline{\text{SS2}}$	ADP3
46	38	27	PTB4	KBIP4	ADP4
47	39	28	PTB5	KBIP5	ADP5
48	40	—	PTB6	ADP6	—

2 Preliminary Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MCF51JM128 microcontroller, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 5. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled C in the parameter tables where appropriate.

2.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 6 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, V_{SS} or V_{DD}).

Table 10. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typ[1]	Max	Unit
7	P	Input low voltage; all digital inputs V_{DD} = 5V V_{DD} = 3V	V_{IL}	—	—	1.75 1.05	V
8	P	Input hysteresis; all digital inputs	V_{hys}	0.06 x V_{DD}			mV
9	P	Input leakage current; input only pins[3]	$\|I_{In}\|$	—	0.1	1	μA
10	P	High Impedance (off-state) leakage current[3]	$\|I_{OZ}\|$	—	0.1	1	μA
11	P	Internal pullup resistors[4]	R_{PU}	20	45	65	kΩ
12	P	Internal pulldown resistors[5]	R_{PD}	20	45	65	kΩ
13		Internal pullup resistor to USBDP (to V_{USB33}) Idle Transmit	R_{PUPD}	900 1425	1300 2400	1575 3090	kΩ
14	C	Input Capacitance; all non-supply pins	C_{In}	—	—	8	pF
15	D	RAM retention voltage[6]	V_{RAM}	—	0.6	1.0	V
16	P	POR rearm voltage	V_{POR}	0.9	1.4	2.0	V
17	D	POR rearm time	t_{POR}	10	—	—	μs
18	P	Low-voltage detection threshold — high range V_{DD} falling V_{DD} rising	V_{LVD1}	3.9 4.0	4.0 4.1	4.1 4.2	V
19	P	Low-voltage detection threshold — low range V_{DD} falling V_{DD} rising	V_{LVD0}	2.48 2.54	2.56 2.62	2.64 2.70	V
20	C	Low-voltage warning threshold — high range 1 V_{DD} falling V_{DD} rising	V_{LVW3}	4.5 4.6	4.6 4.7	4.7 4.8	V
21	P	Low-voltage warning threshold — high range 0 V_{DD} falling V_{DD} rising	V_{LVW2}	4.2 4.3	4.3 4.4	4.4 4.5	V
22	P	Low-voltage warning threshold low range 1 V_{DD} falling V_{DD} rising	V_{LVW1}	2.84 2.90	2.92 2.98	3.00 3.06	V
23	C	Low-voltage warning threshold — low range 0 V_{DD} falling V_{DD} rising	V_{LVW0}	2.66 2.72	2.74 2.80	2.82 2.88	V
24	T	Low-voltage inhibit reset/recover hysteresis 5 V 3 V	V_{hys}	— —	100 60	— —	mV

[1] Typical values are based on characterization data at 25°C unless otherwise stated.
[2] Operating voltage with USB enabled can be found in Section 2.14, "USB Electricals."
[3] Measured with $V_{In} = V_{DD}$ or V_{SS}.
[4] Measured with $V_{In} = V_{SS}$.
[5] Measured with $V_{In} = V_{DD}$.
[6] This is the voltage below which the contents of RAM are not guaranteed to be maintained.

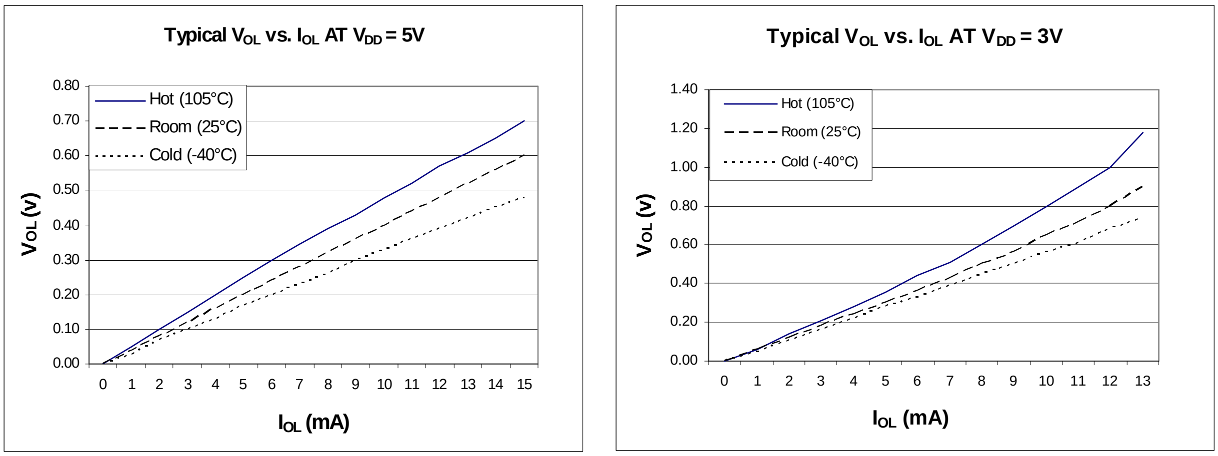


Figure 5. Typical Low-side Drive (sink) characteristics – High Drive (PTxDSn = 1)

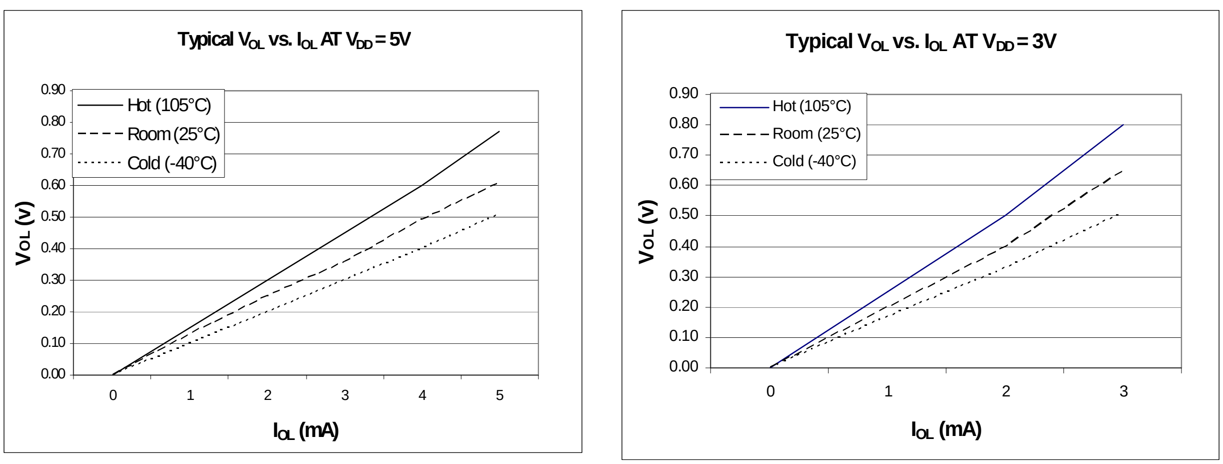


Figure 6. Typical Low-side Drive (sink) characteristics – Low Drive (PTxDSn = 0)

Table 11. Supply Current Characteristics

Num	C	Parameter		Symbol	V_{DD} (V)	Typical[1]	Max[2]	Unit
4	C	Wait mode supply current[3] measured at (CPU clock = 2 MHz, f_{Bus} = 1 MHz)		WI_{DD}	5	2.03	3	mA
					3	2	3	
5	C	Wait mode supply current[3] measured at (CPU clock = 16 MHz, f_{Bus} = 8 MHz)			5	7.73	12	mA
					3	7.7	12	
6	C	Wait mode supply current[3] measured at (CPU clock = 48 MHz, f_{Bus} = 24 MHz)			5	22	30	mA
					3	21.9	30	
7	C	Stop2 mode supply current	–40 °C 25 °C 105 °C	$S2I_{DD}$	5	1.35	3 3 35	µA
			–40 °C 25 °C 105 °C		3	1.25	3 3 35	µA
8	P	Stop3 mode supply current	–40 °C 25 °C 105 °C	$S3I_{DD}$	5	1.41	3 3 35	µA
			–40 °C 25 °C 105 °C		3	1.35	3 3 35	µA
9	C	Stop4 mode supply current	–40 °C 25 °C 105 °C	$S4I_{DD}$	5	106	200	µA
			–40 °C 25 °C 105 °C		3	96	200	µA
10	P	RTC adder to stop2 or stop3[4], 25°C		$S23I_{DDRTC}$	5	300	—	nA
					3	300	—	nA
11	P	Adder to stop3 for oscillator enabled[5] (ERCLKEN =1 and EREFSTEN = 1)		$S23I_{DDOSC}$	5	5	—	µA
					3	5	—	µA

1 Typicals are measured at 25°C.
2 Values given here are preliminary estimates prior to completing characterization.
3 All modules' clocks are switched on, code runs from flash, in FEI mode, and there are no DC loads on port pins.
4 Most customers are expected to find that auto-wakeup from stop2 or stop3 can be used instead of the higher current wait mode.
5 Values given under the following conditions: low range operation (RANGE = 0), low power mode (HGO = 0)

2.7 Analog Comparator (ACMP) Electricals

Table 12. Analog Comparator Electrical Specifications

Num	C	Rating	Symbol	Min	Typical	Max	Unit
1		Supply voltage	V_{DD}	2.7	—	5.5	V
2		Supply current (active)	I_{DDAC}	—	20	35	μA
3		Analog input voltage	V_{AIN}	$V_{SS} - 0.3$	—	V_{DD}	V
4		Analog input offset voltage	V_{AIO}		20	40	mV
5		Analog Comparator hysteresis	V_H	3.0	6.0	20.0	mV
6		Analog input leakage current	I_{ALKG}	--	--	1.0	μA
7		Analog Comparator initialization delay	t_{AINIT}	—	—	1.0	μs
8		Bandgap Voltage Reference Factory trimmed at V_{DD} = 3.0 V, Temp = 25°C	V_{BG}	1.19	1.20	1.21	V

2.8 ADC Characteristics

Table 13. 5 Volt 12-bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	
	Delta to V_{DD} (V_{DD}-V_{DDA})[2]	ΔV_{DDA}	–100	0	+100	mV	
Ground voltage	Delta to V_{SS} (V_{SS}-V_{SSA})[2]	ΔV_{SSA}	–100	0	+100	mV	
Ref Voltage High		V_{REFH}	2.7	V_{DDA}	V_{DDA}	V	
Ref Voltage Low		V_{REFL}	V_{SSA}	V_{SSA}	V_{SSA}	V	
Input Voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
Input Capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input Resistance		R_{ADIN}	—	3	5	kΩ	
Analog Source Resistance	12 bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz	R_{AS}	 — —	 — —	 2 5	kΩ	External to MCU
	10 bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz		 — —	 — —	 5 10		
	8 bit mode (all valid f_{ADCK})		—	—	10		
ADC Conversion Clock Freq.	High Speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	
	Low Power (ADLPC=1)		0.4	—	4.0		

1 Typical values assume V_{DDA} = 5.0V, Temp = 25°C, f_{ADCK}=1.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

2.9 External Oscillator (XOSC) Characteristics

Table 15. Oscillator Electrical Specifications (Temperature Range = –40 to 105°C Ambient)

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
1		Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) • Low range (RANGE = 0) • High range (RANGE = 1) FEE or FBE mode [2] • High range (RANGE = 1) PEE or PBE mode [3] • High range (RANGE = 1, HGO = 1) BLPE mode • High range (RANGE = 1, HGO = 0) BLPE mode	f_{lo} $f_{hi\text{-}fll}$ $f_{hi\text{-}pll}$ $f_{hi\text{-}hgo}$ $f_{hi\text{-}lp}$	32 1 1 1 1	— — — — —	38.4 5 16 16 8	kHz MHz MHz MHz MHz
2		Load capacitors	C_1 C_2	See crystal or resonator manufacturer's recommendation.			
3		Feedback resistor • Low range (32 kHz to 38.4 kHz) • High range (1 MHz to 16 MHz)	R_F		10 1		MΩ MΩ
4	—	Series resistor • Low range, low gain (RANGE = 0, HGO = 0) • Low range, high gain (RANGE = 0, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz • High range, low gain (RANGE = 1, HGO = 0) • High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	— — — — — —	0 100 0 0 0 0	— — — 0 10 20	kΩ
5	T	Crystal start-up time [4] • Low range, low gain (RANGE = 0, HGO = 0) • Low range, high gain (RANGE = 0, HGO = 1) • High range, low gain (RANGE = 1, HG0 = 0)[5] • High range, high gain (RANGE = 1, HG0 = 1)[5]	$t_{CSTL\text{-}LP}$ $t_{CSTL\text{-}HGO}$ $t_{CSTH\text{-}LP}$ $t_{CSTH\text{-}HGO}$	— — — —	200 400 5 15	— — — —	ms
6	T	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) • FEE or FBE mode [2] • PEE or PBE mode [3] • BLPE mode	f_{extal}	0.03125 1 0	— — —	5 16 40	MHz MHz MHz

[1] Data in Typical column was characterized at 5.0 V, 25°C or is typical recommended value.

[2] When MCG is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

[3] When MCG is configured for PEE or PBE mode, input clock source must be divisible using RDIV to within the range of 1 MHz to 2 MHz.

[4] This parameter is characterized and not tested on each device. Proper PC board-layout procedures must be followed to achieve specifications.

[5] 4 MHz crystal

2.10 MCG Specifications

Table 16. MCG Frequency Specifications (Temperature Range = –40 to 125°C Ambient)

Num	C	Rating		Symbol	Min	Typical[1]	Max	Unit
1	P	Internal reference frequency - factory trimmed at V_{DD} = 5 V and temperature = 25 °C		f_{int_ft}	—	32.768	—	kHz
2	P	Average internal reference frequency – untrimmed		f_{int_ut}	31.25	—	39.0625	kHz
3	T	Internal reference startup time		t_{irefst}	—	60	100	µs
4	P	DCO output frequency range - untrimmed [2]	Low range (DRS=00)	f_{dco_ut}	16	—	20	MHz
	P		Mid range (DRS=01)		32	—	40	
	P		High range (DRS=10)		48	—	60	
5	P	DCO output frequency[2] Reference =32768Hz and DMX32 = 1	Low range (DRS=00)	f_{dco_DMX32}	—	19.92	—	MHz
	P		Mid range (DRS=01)		—	39.85	—	
	P		High range (DRS=10)		—	59.77	—	
6	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
7	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	$\%f_{dco}$
8	D	Total deviation of trimmed DCO output frequency over voltage and temperature		Δf_{dco_t}	—	0.5 –1.0	±2	$\%f_{dco}$
9	D	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 – 70 °C		Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$
10	D	FLL acquisition time [3]		$t_{fll\_acquire}$	—	—	1	ms
11	D	PLL acquisition time [4]		$t_{pll\_acquire}$	—	—	1	ms
12	D	Long term Jitter of DCO output clock (averaged over 2ms interval) [5]		C_{Jitter}	—	0.02	0.2	$\%f_{dco}$
13	D	VCO operating frequency		f_{vco}	7.0	—	55.0	MHz
14	D	Jitter of PLL output clock measured over 625 ns[6]		$f_{pll\_jitter\_625ns}$	—	0.566[5]	—	$\%f_{pll}$
15	D	Lock entry frequency tolerance [7]		D_{lock}	±1.49	—	±2.98	%
16	D	Lock exit frequency tolerance [8]		D_{unl}	±4.47	—	±5.97	%
17	D	Lock time — FLL		t_{fll_lock}	—	—	$t_{fll\_acquire}$+ 1075(1/f_{int_t})	s
18	D	Lock time — PLL		t_{pll_lock}	—	—	$t_{pll\_acquire}$+ 1075(1/f_{pll_ref})	s
19	D	Loss of external clock minimum frequency – RANGE = 0		f_{loc_low}	(3/5) x f_{int}	—	—	kHz

1 Data in Typical column was characterized at 5.0 V, 25C or is typical recommended value

2 The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

3 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

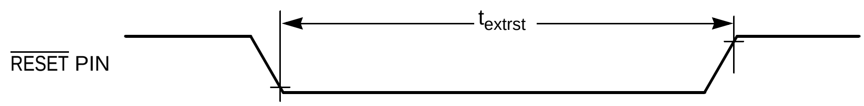


Figure 10. Reset Timing

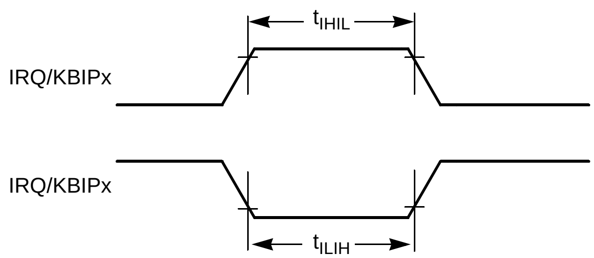


Figure 11. IRQ/KBIPx Timing

2.11.2 Timer/PWM (TPM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 18. TPM Input Timing

NUM	C	Function	Symbol	Min	Max	Unit
1	—	External clock frequency	f_{TPMext}	dc	$f_{Bus}/4$	MHz
2	—	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

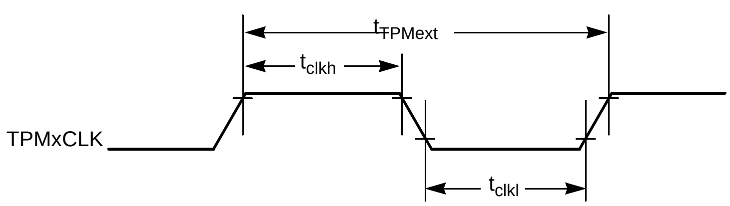


Figure 12. Timer External Clock

Table 22. Internal USB 3.3V Voltage Regulator Characteristics

	Symbol	Unit	Min	Typ	Max
Regulator operating voltage	V_{regin}	V	3.9	—	5.5
Vreg output	V_{regout}	V	3	3.3	3.6
Vusb33 input with internal Vreg disabled	$V_{usb33in}$	V	3	3.3	3.6
VREG Quiescent Current	I_{VRQ}	mA	—	0.5	—

2.15 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

2.15.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East). For more detailed information concerning the evaluation results, conditions and setup, please refer to the EMC Evaluation Report for this device.

3.2 64-pin LQFP

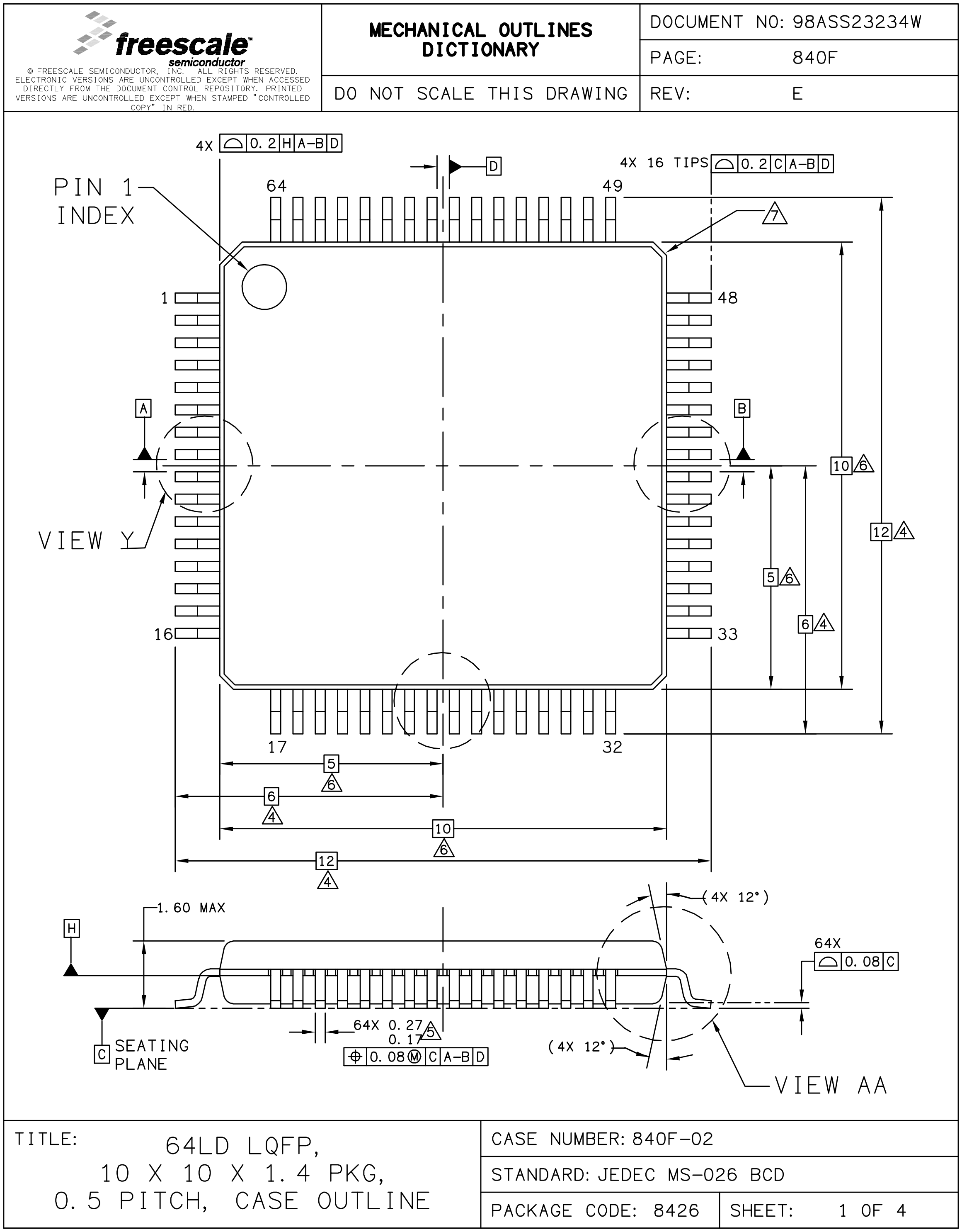


Figure 21. 64-pin LQFP Diagram - I

3.3 64-pin QFP

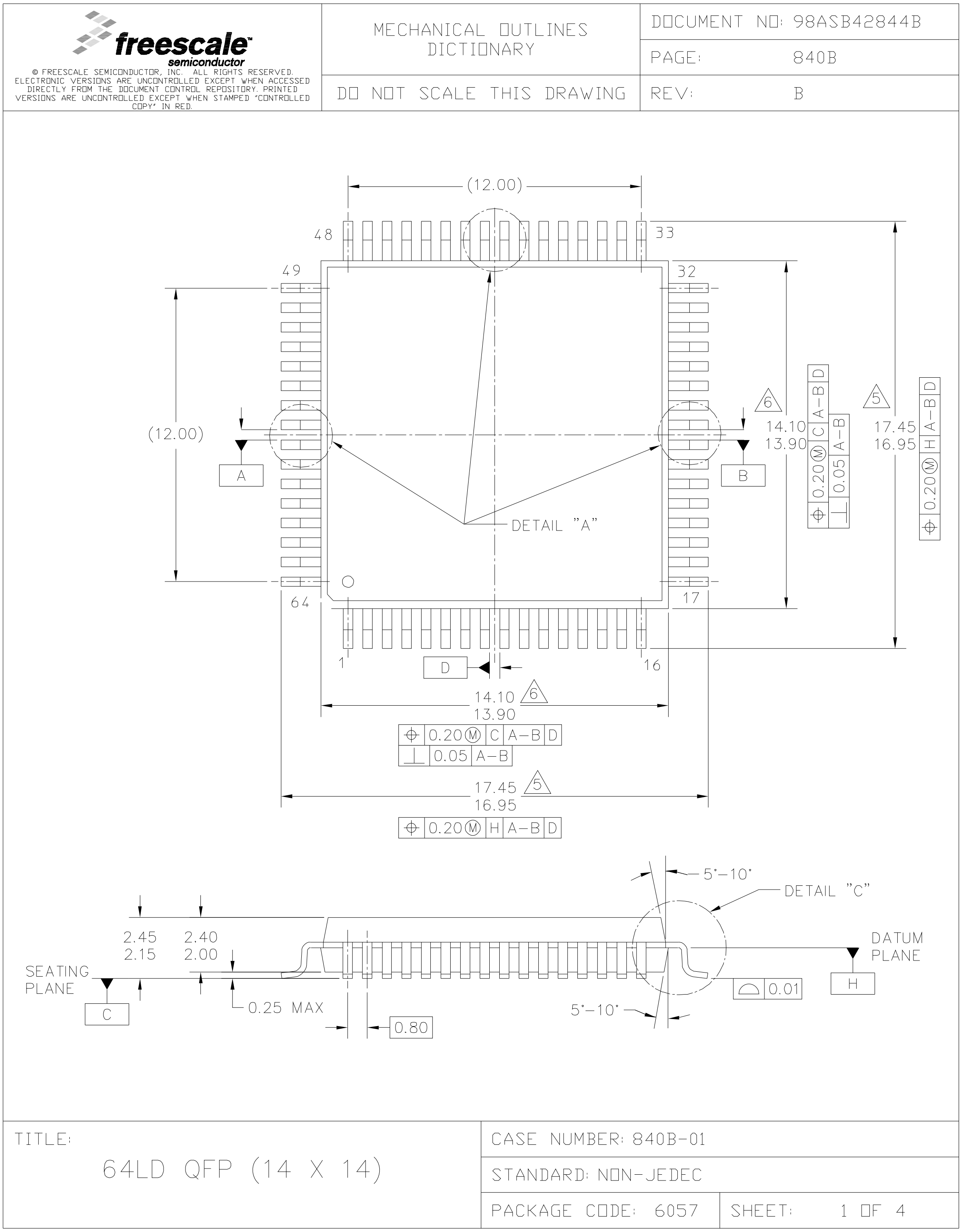
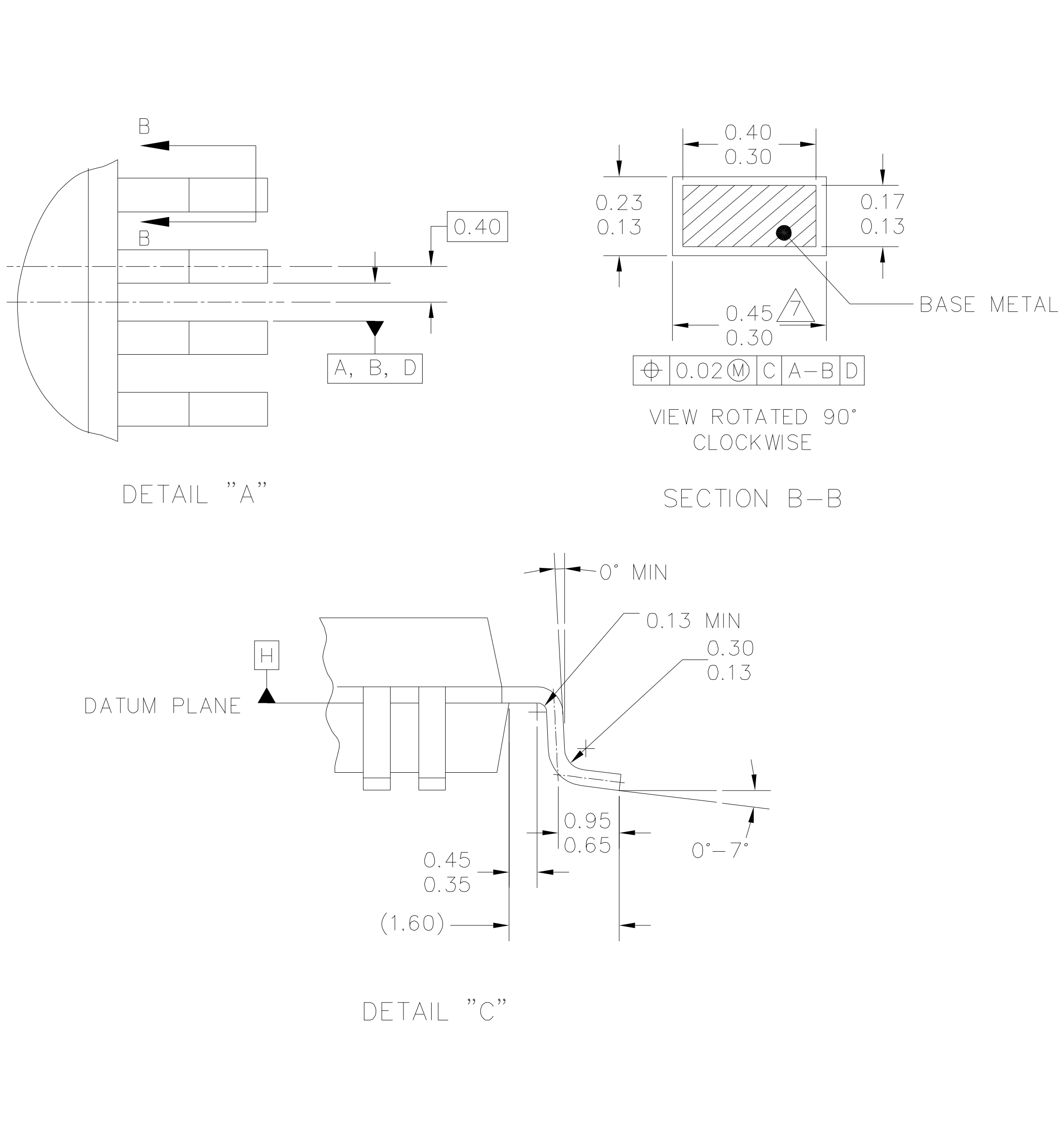


Figure 24. 64-pin QFP Diagram - I

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASB42844B
		PAGE: 840B
	DO NOT SCALE THIS DRAWING	REV: B



TITLE: 64LD QFP (14 X 14)	CASE NUMBER: 840B-01	
	STANDARD: NON-JEDEC	
	PACKAGE CODE: 6057	SHEET: 2 OF 4

Figure 25. 64-pin QFP Diagram - II

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		PAGE: 840B
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NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A–B AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE –C–.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

TITLE: 64LD QFP (14 X 14)	CASE NUMBER: 840B–01	
	STANDARD: NON–JEDEC	
	PACKAGE CODE: 6057	SHEET: 3 OF 4

Figure 26. 64-pin QFP Diagram - III

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Freescale Semiconductor, Inc.
Technical Information Center, EL516
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Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
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81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
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Japan:
Freescale Semiconductor Japan Ltd. Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
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Chaoyang District
Beijing 100022
China
+86 10 5879 8000
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