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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR60 RISC
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	109
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	72K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 32x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f467tapmc-gsk5e2

Feature	MB91V460A	MB91FV460B *4	MB91F467TA	MB91F469TA *3
Power Consumption	n.a.	< 3 W	< 1.3 W	< 1.3 W
Temperature Range (T_A)	0..70 C	0..70 C	-40..105 C	-40..105 C
Package	BGA660	BGA-896	QFP144	QFP144
Power on to PLL run	< 20 ms	< 20 ms	< 20 ms	< 20 ms
Flash Download Time	n.a.	< 8 sec typical	< 5 sec. typical	< 6 sec typical

*1 : MPU channels use EDSU breakpoint registers (shared operation between MPU and EDSU).

*2 : Maximum channel count is shown; function is multiplexed with other pins

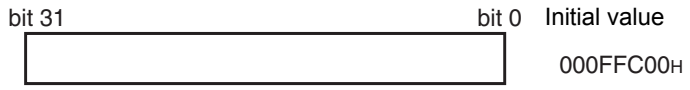
*3 : This device is planned.

*4 : The new emulation device MB91FV460B can emulate the MB91460T series special pin multiplexing as well as the behaviour of the external bus at startup.

Pin no.	Pin name	I/O	I/O circuit type*	MUX	Function
62	P22_6	I/O	C	-	General-purpose input/output port
	SDA1				I^2C bus DATA input/output pin (open drain)
	INT15				External interrupt input pin
63	P22_7	I/O	C	-	General-purpose input/output port
	SCL1				I^2C bus clock input/output pin (open drain)
64 to 67	P14_0 to P14_3	I/O	A	-	General-purpose input/output ports
	ICU0 to ICU3				Input capture input pins
	TIN0 to TIN3				External trigger input pins of reload timer
	TTG8/0 to TTG11/3				External trigger input pins of PPG timer
68 to 71	P15_0 to P15_3	I/O	A	-	General-purpose input/output ports
	OCU0 to OCU3				Output compare output pins
	TOT0 to TOT3				Reload timer output pins
74	MD_0	I	G	-	Mode setting pin
75	MD_1	I	G	-	Mode setting pin
76	MD_2	I	G	-	Mode setting pin
77	MONCLK	O	M	-	Clock Monitor pin
78	MD_3	I	G	-	Fast clock input pin
79	X1	-	J1	-	Clock (oscillation) output
80	X0	-	J1	-	Clock (oscillation) input
82	X0A	-	J2	-	Sub clock (oscillation) input
83	X1A	-	J2	-	Sub clock (oscillation) output
84	INITX	I	H	-	External reset input pin
85	NMIX	I	H	-	Non-maskable interrupt input pin
92	P19_0	I/O	A	-	General-purpose input/output port
	SIN4				Data input pin of USART4
93	P19_1	I/O	A	-	General-purpose input/output port
	SOT4				Data output pin of USART4
94	P19_2	I/O	A	-	General-purpose input/output port
	SCK4				Clock input/output pin of USART4
	CK4				External clock input pin of free-run timer 4
95	P19_4	I/O	A	-	General-purpose input/output port
	SIN5				Data input pin of USART5
96	P19_5	I/O	A	-	General-purpose input/output port
	SOT5				Data output pin of USART5

Pin no.	Pin name	I/O	I/O circuit type*	MUX	Function
131	P20_1	I/O	A	PPMUX.PS1=0 and_not (PPMUX.PR13=1 and PPMUX.PRPS0=1)	General-purpose input/output port
	SOT2				Data output pin of USART2
	BIN0				Up/down counter input pin
	OR				
	P27_3	I/O	A	PPMUX.PS1=1 or (PPMUX.PR13=1 and PPMUX.PRPS0=1)	General-purpose input/output port
	AN19				Analog input pin of A/D converter
132	P20_2	I/O	A	PPMUX.PS1=0 and_not (PPMUX.PR14=1 and PPMUX.PRPS0=1)	General-purpose input/output port
	SCK2				Clock input/output pin of USART2
	ZIN0				Up/down counter input pin
	CK2				External clock input pin of free-run timer 2
	OR				
	P27_4	I/O	A	PPMUX.PS1=1 or (PPMUX.PR14=1 and PPMUX.PRPS0=1)	General-purpose input/output port
	AN20				Analog input pin of A/D converter
133	P20_4	I/O	A	PPMUX.PS1=0 and_not (PPMUX.PR15=1 and PPMUX.PRPS0=1)	General-purpose input/output port
	SIN3				Data input pin of USART3
	AIN1				Up/down counter input pin
	OR				
	P27_5	I/O	A	PPMUX.PS1=1 or (PPMUX.PR15=1 and PPMUX.PRPS0=1)	General-purpose input/output port
	AN21				Analog input pin of A/D converter
134	P20_5	I/O	A	PPMUX.PS1=0 and_not (PPMUX.PR16=1 and PPMUX.PRPS0=1)	General-purpose input/output port
	SOT3				Data output pin of USART3
	BIN1				Up/down counter input pin
	OR				
	P27_6	I/O	A	PPMUX.PS1=1 or (PPMUX.PR16=1 and PPMUX.PRPS0=1)	General-purpose input/output port
	AN22				Analog input pin of A/D converter

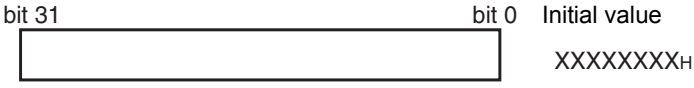
9.4.7 TBR (Table Base Register)



The table base register stores the starting address of the vector table used in EIT processing.

The initial value at reset is $000FFC00_H$.

9.4.8 RP (Return Pointer)



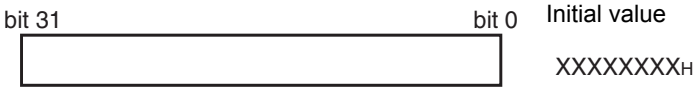
The return pointer stores the address for return from subroutines.

During execution of a CALL instruction, the PC value is transferred to this RP register.

During execution of a RET instruction, the contents of the RP register are transferred to PC.

The initial value at reset is undefined.

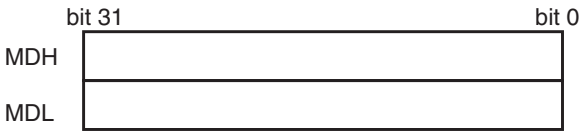
9.4.9 USP (User Stack Pointer)



The user stack pointer, when the S flag is “1”, this register functions as the R15 register.

- The USP register can also be explicitly specified.
  The initial value at reset is undefined.
- This register cannot be used with RETI instructions.

9.4.10 Multiply & divide registers



These registers are for multiplication and division, and are each 32 bits in length.

The initial value at reset is undefined.

Address	Register				Block
	+0	+1	+2	+3	
000154_H	PDUT08 [W] XXXXXXXX XXXXXXXX		PCNH08 [R/W] 0000000 -	PCNL08 [R/W] 000000 - 0	
000158_H	PTMR09 [R] 11111111 11111111		PCSR09 [W] XXXXXXXX XXXXXXXX		PPG 9
$00015C_H$	PDUT09 [W] XXXXXXXX XXXXXXXX		PCNH09 [R/W] 0000000 -	PCNL09 [R/W] 000000 - 0	
000160_H	PTMR10 [R] 11111111 11111111		PCSR10 [W] XXXXXXXX XXXXXXXX		PPG 10
000164_H	PDUT10 [W] XXXXXXXX XXXXXXXX		PCNH10 [R/W] 0000000 -	PCNL10 [R/W] 000000 - 0	
000168_H	PTMR11 [R] 11111111 11111111		PCSR11 [W] XXXXXXXX XXXXXXXX		PPG 11
$00016C_H$	PDUT11 [W] XXXXXXXX XXXXXXXX		PCNH11 [R/W] 0000000 -	PCNL11 [R/W] 000000 - 0	
000170_H	P0TMCSRH [R/W] - 0000000	P0TMCSRL [R/W] 01000000	P1TMCSRH [R/W] - 0000000	P1TMCSRL [R/W] 01000000	Pulse Frequency Modulator
000174_H	P0TMRLR [W] XXXXXXXX XXXXXXXX		P0TMR [R] XXXXXXXX XXXXXXXX		
000178_H	P1TMRLR [W] XXXXXXXX XXXXXXXX		P1TMR [R] XXXXXXXX XXXXXXXX		
$00017C_H$	Reserved				
000180_H	Reserved	ICS01 [R/W] 00000000	Reserved	ICS23 [R/W] 00000000	Input Capture 0 to 3
000184_H	IPCP0 [R] XXXXXXXX XXXXXXXX		IPCP1 [R] XXXXXXXX XXXXXXXX		
000188_H	IPCP2 [R] XXXXXXXX XXXXXXXX		IPCP3 [R] XXXXXXXX XXXXXXXX		
$00018C_H$	OCS01 [R/W] - - - 0 - - 00 0000 - - 00		OCS23 [R/W] - - - 0 - - 00 0000 - - 00		Output Compare 0 to 3
000190_H	OCCP0 [R/W] XXXXXXXX XXXXXXXX		OCCP1 [R/W] XXXXXXXX XXXXXXXX		
000194_H	OCCP2 [R/W] XXXXXXXX XXXXXXXX		OCCP3 [R/W] XXXXXXXX XXXXXXXX		
000198_H	SGCRH [R/W] 0000 - - 00	SGCRL [R/W] - - 0 - - 000	SGFR [R/W, R] XXXXXXXX XXXXXXXX		Sound Generator
$00019C_H$	SGAR [R/W] 00000000	Reserved	SGTR [R/W] XXXXXXXX	SGDR [R/W] XXXXXXXX	
$0001A0_H$	ADERH [R/W] 00000000 00000000		ADERL [R/W] 00000000 00000000		A/D Converter
0001A4	ADCS1 [R/W] 00000000	ADCS0 [R/W] 00000000	ADCR1 [R] 000000XX	ADCR0 [R] XXXXXXXX	
$0001A8_H$	ADCT1 [R/W] 00010000	ADCT0 [R/W] 00101100	ADSCH [R/W] - - - 00000	ADECH [R/W] - - - 00000	

Address	Register				Block
	+0	+1	+2	+3	
000494_H	OSCC1 [R/W] - - - - - 010	OSCS1 [R/W] 00001111	OSCC2 [R/W] - - - - - 010	OSCS2 [R/W] 00001111	Main/Sub Oscillator Control
000498_H	PORTEN [R/W] - - - - - - 00	Reserved	PPMUX [R/W] *1 00000000 00000000		Port Input Enable Control / PortMux Control
$00049C_H$	Reserved				
$0004A0_H$	Reserved	WTCER [R/W] - - - - - - 00	WTCR [R/W] 00000000 000 – 00 – 0		Real Time Clock (Watch Timer)
$0004A4_H$	Reserved	WTBR [R/W] - - - XXXXX XXXXXXXX XXXXXXXX			
$0004A8_H$	WTHR [R/W] - - - 00000	WTMR [R/W] - - 000000	WTSR [R/W] - - 000000	Reserved	
$0004AC_H$	CSVTR [R/W] - - - 00010	CSVCR [R/W] 00011100	CSCFG [R/W] 0X000000	CMCFG [R/W] 00000000	Clock-Supervisor / Selector / Monitor
$0004B0_H$	CUCR [R/W] - - - - - - - - - - - - 0 - - 00		CUTD [R/W] 10000000 00000000		Calibration Unit of Sub Oscillation
$0004B4_H$	CUTR1 [R] - - - - - - - - 00000000		CUTR2 [R] 00000000 00000000		
$0004B8_H$	CMPR [R/W] - - 000010 11111101		Reserved	CMCR [R/W] - 001 - - 00	Clock Modulation
$0004BC_H$	CMT1 [R/W] 00000000 1 - - - 0000		CMT2 [R/W] - - 000000 - - 000000		
$0004C0_H$	CANPRE [R/W] 0 - - - 0000	CANCKD [R/W] - - - - - 000 *2	Reserved	Reserved	CAN Clock Control
$0004C4_H$	LVSEL [R/W] 00000111	LVDET [R/W] 0000 0 - 00	HWWDE [R/W] - - - - - - 00	HWWD [R/W,W] 00011000	LV Detection / Hardware-Watchdog
$0004C8_H$	OSCRH [R/W] 000 - - 001	OSCRL [R/W] - - - - - 000	WPCRH [R/W] 00 - - - 000	WPCRL [R/W] - - - - - - 00	Main-/Sub-Oscillation Stabilization Timer
$0004CC_H$	OSCCR [R/W] - - - - - - 00	Reserved	REGSEL [R/W] - - 000110	REGCTR [R/W] - - - 0 - - 00	Main-Oscillation Standby Control Main/Sub Regulator Control
000500_H to $00063C_H$	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
$00C180_H$	TREQR21 [R] 00000000 00000000		TREQR11 [R] 00000000 00000000		CAN 1 Status Flags
$00C184_H$ to $00C18C_H$	Reserved				
$00C190_H$	NEWDT21 [R] 00000000 00000000		NEWDT11 [R] 00000000 00000000		
$00C194_H$ to $00C19C_H$	Reserved				
$00C1A0_H$	INTPND21 [R] 00000000 00000000		INTPND11 [R] 00000000 00000000		
$00C1A4_H$ to $00C1AC_H$	Reserved				
$00C1B0_H$	MSGVAL21 [R] 00000000 00000000		MSGVAL11 [R] 00000000 00000000		
$00C1B4_H$ to $00EFF_H$	Reserved				
$00F000_H$	BCTRL [R/W] -------- -------- 11111100 00000000				EDSU / MPU
$00F004_H$	BSTAT [R/W] -------- -----000 00000000 10--0000				
$00F008_H$	BIAC [R] -------- -------- 00000000 00000000				
$00F00C_H$	BOAC [R] -------- -------- 00000000 00000000				
$00F010_H$	BIRQ [R/W] -------- -------- 00000000 00000000				
$00F014_H$ to $00F01C_H$	Reserved				EDSU / MPU
$00F020_H$	BCR0 [R/W] -------- 00000000 00000000 00000000				
$00F024_H$	BCR1 [R/W] -------- 00000000 00000000 00000000				
$00F028_H$	BCR2 [R/W] -------- 00000000 00000000 00000000				
$00F02C_H$	BCR3 [R/W] -------- 00000000 00000000 00000000				
$00F030_H$ to $00F07C_H$	Reserved				

*4 : TCR [3 : 0] INIT value = 0000, keeps value after RST

*5: PFR initial values for ports 00..10 depend on the selected mode at the mode pins MD_0..MD_2:
internal usermode (000): PFR00..PFR10 initialized to all 0
external usermode (001): PFR00..PFR10 initialized to all 1

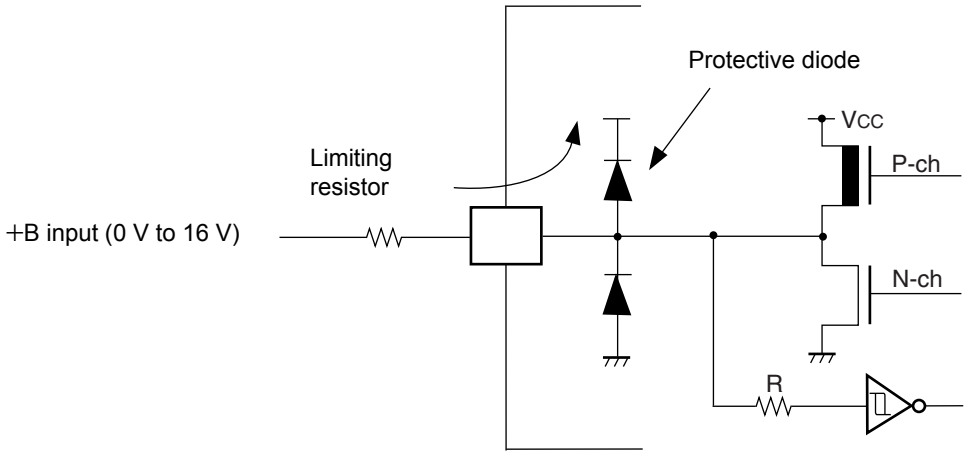
Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		DMA *3 Resource Number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
Reserved	86	56	ICR35	463_H	$2A4_H$	000FFEA4	74
Reserved	87	57			$2A0_H$	000FFEA0	75
Reserved	88	58	ICR36	464_H	$29C_H$	000FFE9C	76
Reserved	89	59			298_H	000FFE98	77
Reserved	90	5A	ICR37	465_H	294_H	000FFE94	78
Reserved	91	5B			290_H	000FFE90	79
Input Capture 0	92	5C	ICR38	466_H	$28C_H$	000FFE8C	80
Input Capture 1	93	5D			288_H	000FFE88	81
Input Capture 2	94	5E	ICR39	467_H	284_H	000FFE84	82
Input Capture 3	95	5F			280_H	000FFE80	83
Input Capture 4	96	60	ICR40	468_H	$27C_H$	000FFE7C	84
Input Capture 5	97	61			278_H	000FFE78	85
Input Capture 6	98	62	ICR41	469_H	274_H	000FFE74	86
Input Capture 7	99	63			270_H	000FFE70	87
Output Compare 0	100	64	ICR42	$46A_H$	$26C_H$	000FFE6C	88
Output Compare 1	101	65			268_H	000FFE68	89
Output Compare 2	102	66	ICR43	$46B_H$	264_H	000FFE64	90
Output Compare 3	103	67			260_H	000FFE60	91
Output Compare 4	104	68	ICR44	$46C_H$	$25C_H$	000FFE5C	92
Output Compare 5	105	69			258_H	000FFE58	93
Output Compare 6	106	6A	ICR45	$46D_H$	254_H	000FFE54	94
Output Compare 7	107	6B			250_H	000FFE50	95
Sound Generator	108	6C	ICR46	$46E_H$	$24C_H$	000FFE4C	-
Phase Frequency Modulator	109	6D			248_H	000FFE48	-
System reserved	110	6E	ICR47 *4	$46F_H$	244_H	000FFE44	-
System reserved	111	6F			240_H	000FFE40	-
PPG 0	112	70	ICR48	470_H	$23C_H$	000FFE3C	15, 96
PPG 1	113	71			238_H	000FFE38	97
PPG 2	114	72	ICR49	471_H	234_H	000FFE34	98
PPG 3	115	73			230_H	000FFE30	99

Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		DMA *3 Resource Number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
PPG 4	116	74	ICR50	472_H	$22C_H$	000FFE2C	100
PPG 5	117	75			228_H	000FFE28	101
Reserved	118	76	ICR51	473_H	224_H	000FFE24	102
Reserved	119	77			220_H	000FFE20	103
PPG 8	120	78	ICR52	474_H	$21C_H$	000FFE1C	104
PPG 9	121	79			218_H	000FFE18	105
PPG 10	122	7A	ICR53	475_H	214_H	000FFE14	106
PPG 11	123	7B			210_H	000FFE10	107
PPG 12	124	7C	ICR54	476_H	$20C_H$	000FFE0C	108
PPG 13	125	7D			208_H	000FFE08	109
PPG 14	126	7E	ICR55	477_H	204_H	000FFE04	110
PPG 15	127	7F			200_H	000FFE00	111
Up/Down Counter 0	128	80	ICR56	478_H	$1FC_H$	000FFDFC	-
Up/Down Counter 1	129	81			$1F8_H$	000FFDF8	-
Up/Down Counter 2	130	82	ICR57	479_H	$1F4_H$	000FFDF4	-
Up/Down Counter 3	131	83			$1F0_H$	000FFDF0	-
Real Time Clock	132	84	ICR58	$47A_H$	$1EC_H$	000FFDEC	-
Calibration Unit	133	85			$1E8_H$	000FFDE8	-
A/D Converter 0	134	86	ICR59	$47B_H$	$1E4_H$	000FFDE4	14, 112
-	135	87			$1E0_H$	000FFDE0	-
Reserved	136	88	ICR60	$47C_H$	$1DC_H$	000FFDDC	-
Reserved	137	89			$1D8_H$	000FFDD8	-
Low Voltage Detection	138	8A	ICR61	$47D_H$	$1D4_H$	000FFDD4	-
Reserved	139	8B			$1D0_H$	000FFDD0	-
Timebase Overflow	140	8C	ICR62	$47E_H$	$1CC_H$	000FFDCC	-
PLL Clock Gear	141	8D			$1C8_H$	000FFDC8	-
DMA Controller	142	8E	ICR63	$47F_H$	$1C4_H$	000FFDC4	-
Main/Sub OSC stability wait	143	8F			$1C0_H$	000FFDC0	-
Security vector	144	90	-	-	$1BC_H$	000FFDBC	-

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
1	5	02AE	40	34.9	46.8
1	7	02ED	40	33.1	50.5
1	9	032C	40	31.5	54.8
1	11	036B	40	30	59.9
1	13	03AA	40	28.7	66.1
1	15	03E9	40	27.4	73.7
2	3	046E	40	34.9	46.8
2	5	04AC	40	31.5	54.8
2	7	04EA	40	28.7	66.1
2	9	0528	40	26.3	83.3
3	3	066D	40	33.1	50.5
3	5	06AA	40	28.7	66.1
3	7	06E7	40	25.3	95.8
4	3	086C	40	31.5	54.8
4	5	08A8	40	26.3	83.3
5	3	0A6B	40	30	59.9
6	3	0C6A	40	28.7	66.1
7	3	0E69	40	27.4	73.7
8	3	1068	40	26.3	83.3
9	3	1267	40	25.3	95.8
1	3	026F	36	33.3	39.2
1	5	02AE	36	31.5	42
1	7	02ED	36	29.9	45.3
1	9	032C	36	28.4	49.2
1	11	036B	36	27.1	53.8
1	13	03AA	36	25.8	59.3
1	15	03E9	36	24.7	66.1
2	3	046E	36	31.5	42
2	5	04AC	36	28.4	49.2
2	7	04EA	36	25.8	59.3
2	9	0528	36	23.7	74.7
3	3	066D	36	29.9	45.3
3	5	06AA	36	25.8	59.3
3	7	06E7	36	22.8	85.8
4	3	086C	36	28.4	49.2
4	5	08A8	36	23.7	74.7
5	3	0A6B	36	27.1	53.8
6	3	0C6A	36	25.8	59.3

- Do not leave +B input pins open.
- Example of recommended circuit :

Input/output equivalent circuit



*4 : Maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*5 : Average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 100 ms period.

*6 : Total average output current is defined as the value of the average current flowing through all of the corresponding pins for a 100 ms period.

*7 : The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.

The actual power dissipation depends on the customer application and can be calculated as follows:

$P_D = P_{IO} + P_{INT}$

$P_{IO} = \Sigma (|V_{SS}-V_{OL}| * I_{OL} + |V_{DD}-V_{OH}| * I_{OH})$ (IO load power dissipation, sum is performed on all IO ports)

$P_{INT} = V_{DD}5R * I_{CC} + AV_{CC}5 * I_A + AVRH5 * I_R$ (internal power dissipation)

*8 : Worst case value for the QFP package mounted on a 4-layer PCB at specified T_A without air flow.

*9 : Please contact Cypress for reliability limitations when using under these conditions.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

16.4 A/D converter characteristics

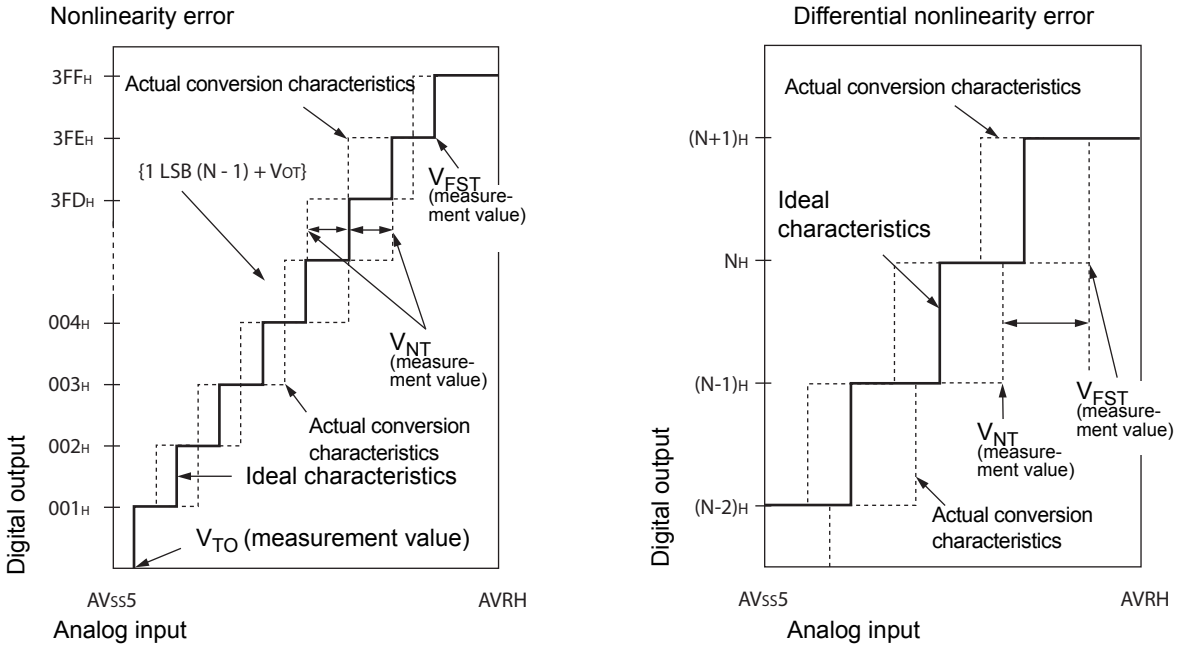
($V_{DD}5 = AV_{CC}5$ = 3.0 V to 5.5 V, $V_{SS}5 = AV_{SS}5$ = 0 V, T_A = −40°C to $T_{A(max)}$)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	- 3	—	+ 3	LSB	
Nonlinearity error	—	—	- 2.5	—	+ 2.5	LSB	
Differential nonlinearity error	—	—	- 1.9	—	+ 1.9	LSB	
Zero reading voltage	V_{OT}	ANn	AVRL−1.5 LSB	AVRL + 0.5 LSB	AVRL + 2.5 LSB	V	
Full scale reading voltage	V_{FST}	ANn	AVRH−3.5 LSB	AVRH−1.5 LSB	AVRH + 0.5 LSB	V	
Compare time	T_{comp}	—	0.6	—	16,500	µs	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V
			2.0	—	—	µs	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V
Sampling time	T_{samp}	—	0.4	—	—	µs	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V, R_{EXT} < 2 kΩ
			1.0	—	—	µs	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V, R_{EXT} < 1 kΩ
Conversion time	T_{conv}	—	1.0	—	—	µs	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V
			3.0	—	—	µs	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V
Input capacitance	C_{IN}	ANn	—	—	11	pF	
Input resistance	R_{IN}	ANn	—	—	2.6	kΩ	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V
			—	—	12.1	kΩ	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V
Analog input leakage current	I_{AIN}	ANn	- 1	—	+ 1	µA	T_A = + 25 °C
			- 3	—	+ 3	µA	T_A = + 105 °C
Analog input voltage range	V_{AIN}	ANn	AVRL	—	AVRH	V	
Offset between input channels	—	ANn	—	—	4	LSB	

(Continued)

Note : The accuracy gets worse as AVRH - AVRL becomes smaller

(Continued)

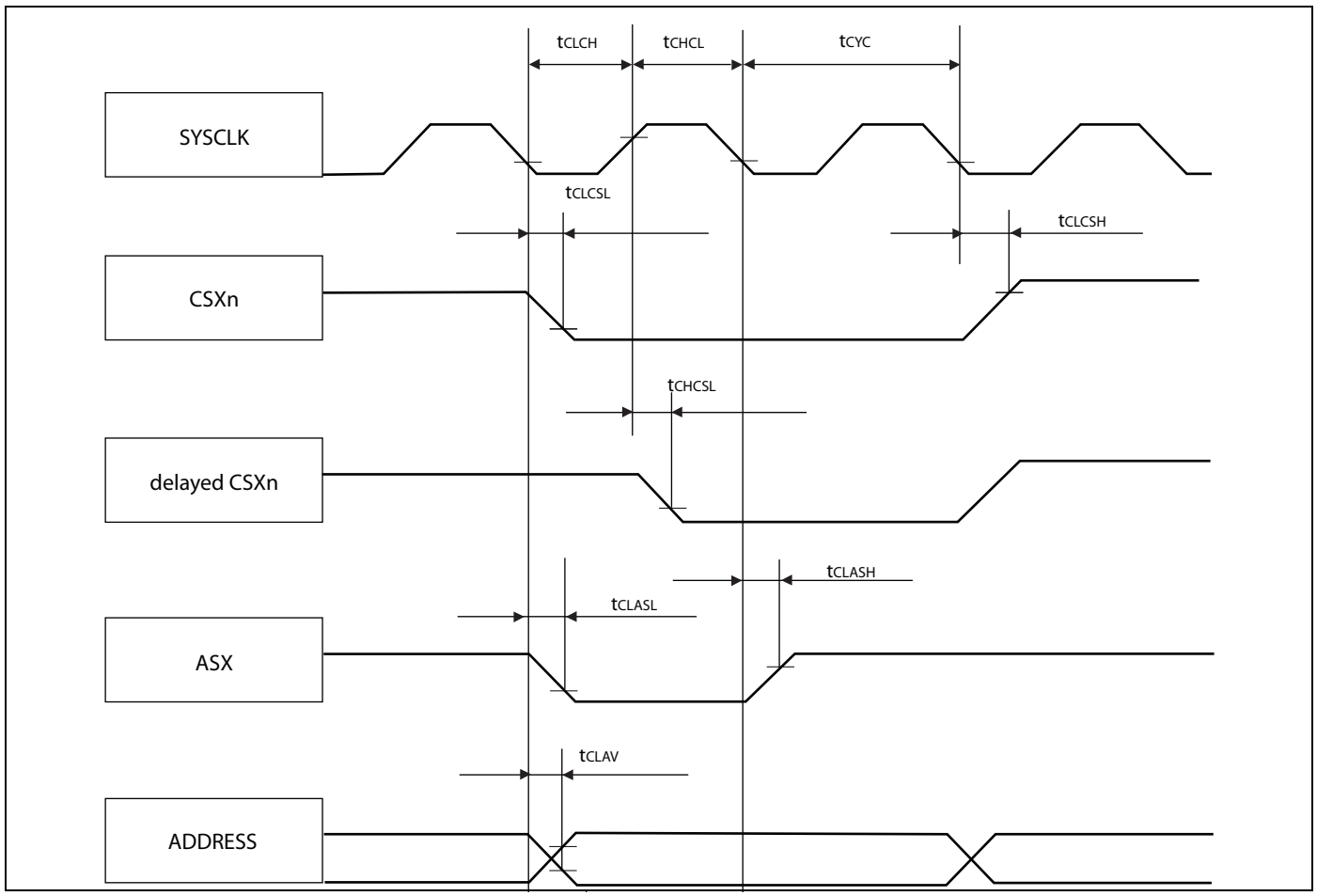


$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1LSB \cdot (N - 1) + V_{OT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

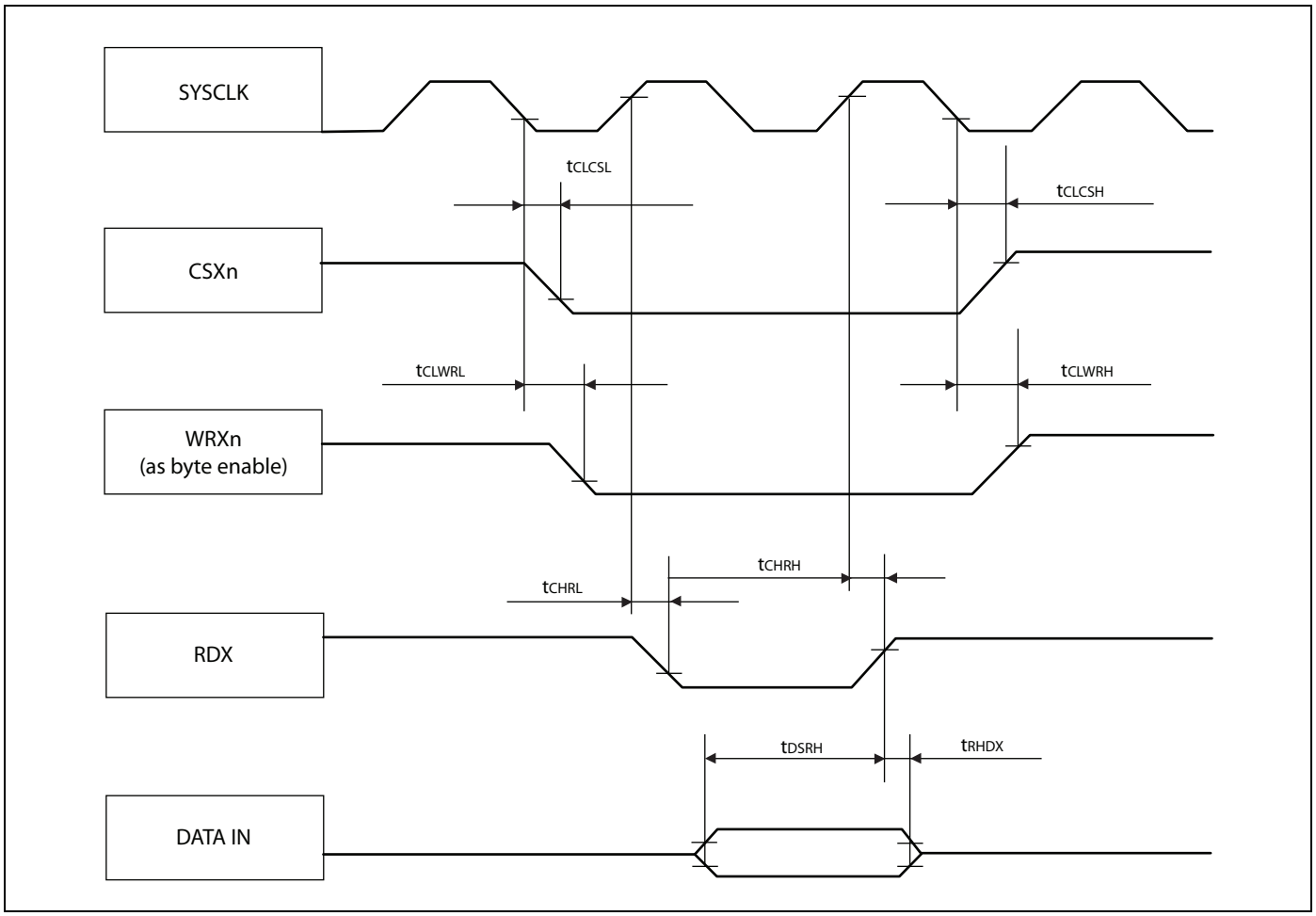
N : A/D converter digital output value
V_{OT} : Voltage at which the digital output changes from 000_H to 001_H.
V_{FST} : Voltage at which the digital output changes from $3FE_H$ to $3FF_H$.


tCLCH
tCHCL
tCYC
SYSCLK
tCLCSL
tCLCSH
CSXn
tCHCSL
delayed CSXn
tCLASH
tCLASL
ASX
tCLAV
ADDRESS

Synchronous/Asynchronous read access

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = 0 V, T_A = −40°C to $T_{A(max)}$)

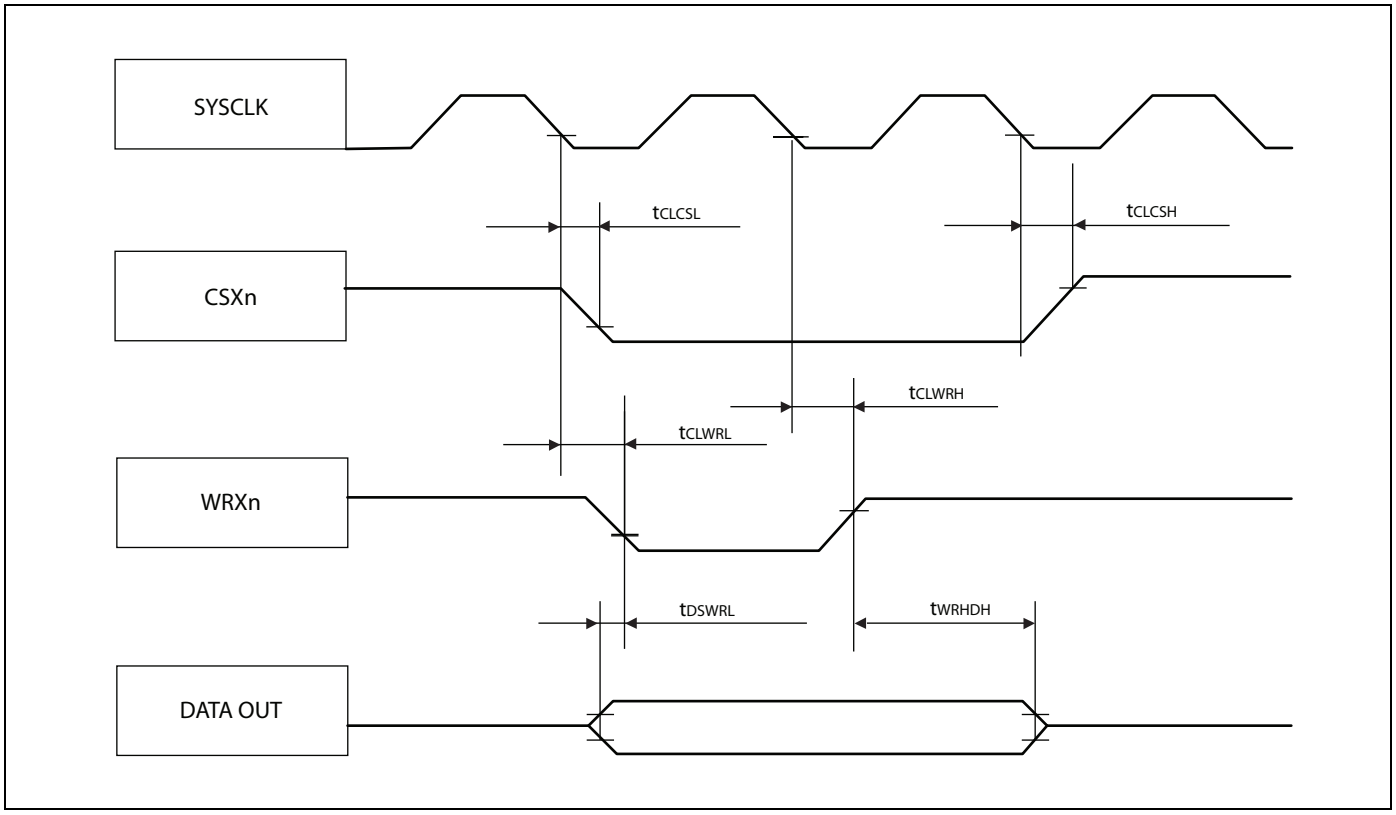
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK ↑ to RDX delay time	TCHRL	SYSCLK RDX	−5	2	ns
	TCHRH		−5	2	ns
Data valid to RDX ↑ setup time	TDSRH	RDX D31 to D16	20	—	ns
RDX ↑ to Data valid hold time	TRHDX	RDX D31 to D16	0	—	ns
SYSCLK ↓ to WRXn (as byte enable) delay time	TCLWRL	SYSCLK WRXn	—	9	ns
	TCLWRH		−1	—	ns
SYSCLK ↓ to CSXn delay time	TCLCSL	SYSCLK CSXn	—	9	ns
	TCLCSH		—	8	ns



Synchronous write access - no byte control type

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = 0 V, T_A = −40°C to $T_{A(max)}$)

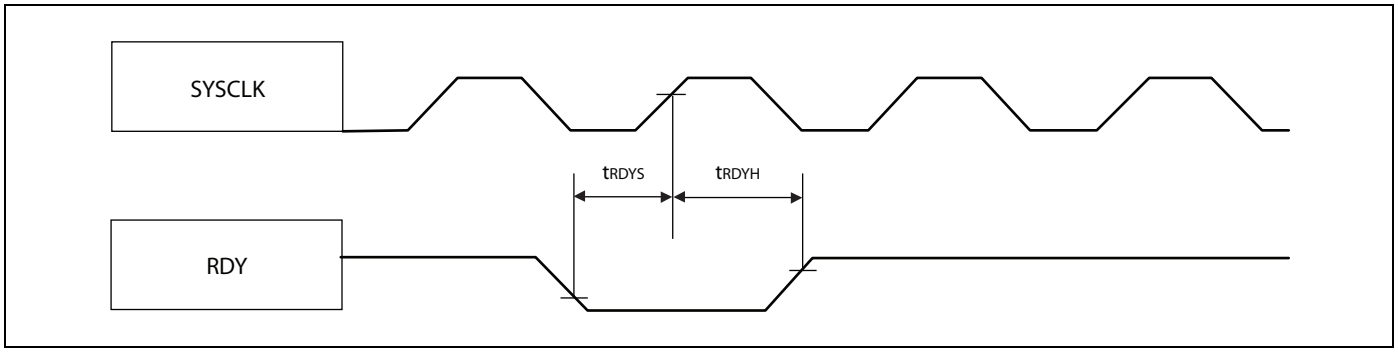
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK ↓ to WRXn delay time	TCLWRL	SYSCLK WRXn	—	9	ns
	TCLWRH		−1	—	ns
Data valid to WRXn ↓ setup time	TDSWRL	WRXn D31 to D16	−12	—	ns
WRXn ↑ to Data valid hold time	TWRHDH	WRXn D31 to D16	t_{CLKT} − 8	—	ns
SYSCLK ↓ to CSXn delay time	TCLCSL	SYSCLK CSXn	—	9	ns
	TCLCSH		—	8	ns



RDY waitcycle insertion

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = 0 V, T_A = −40°C to $T_{A(max)}$)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
RDY setup time	TRDYS	SYSCLK RDY	21	—	ns
RDY hold time	TRDYH	SYSCLK RDY	0	—	ns



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117	6.7.3. Synchronous write access - byte control type	
118	6.7.4. Synchronous write access - no byte control type	
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123	6.8.1. Basic Timing	
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