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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, SCI, SSU
Peripherals	LVD, POR, PWM, WDT
Number of I/O	45
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36034gfpv

1.4 Pin Functions

Table 1.1 Pin Functions

Type	Symbol	Pin No. FP-64K FP-64A	I/O	Functions
Power source pins	V_{CC}	12	Input	Power supply pin. Connect this pin to the system power supply.
	V_{SS}	9	Input	Ground pin. Connect this pin to the system power supply (0 V).
	AV_{CC}	3	Input	Analog power supply pin for the A/D converter. When the A/D converter is not used, connect this pin to the system power supply.
	V_{CL}	6	Input	Internal step-down power supply pin. Connect a capacitor of around 0.1 μF between this pin and the Vss pin for stabilization.
Clock pins	OSC1	11	Input	These pins connect with crystal or ceramic resonator for the system clock, or can be used to input an external clock. See section 5, Clock Pulse Generators, for a typical connection.
	OSC2	10	Output	
System control	$\overline{RES}$	7	Input	Reset pin. The pull-up resistor (typ. 150 kΩ) is incorporated. When driven low, the chip is reset.
	TEST	8	Input	Test pin. Connect this pin to Vss.
Interrupt pins	$\overline{NMI}$	35	Input	Non-maskable interrupt request input pin. Must be pulled-up with a resistor.
	$\overline{IRQ0}$ to $\overline{IRQ3}$	51 to 54	Input	External interrupt request input pins. Can select the rising or falling edge.
	$\overline{WKP0}$ to $\overline{WKP5}$	13, 14, 19 to 22	Input	External interrupt request input pins. Can select the rising or falling edge.
Timer B1	TMIB1	52	Input	External event input pin.
Timer V	TMOV	30	Output	This is an output pin for waveforms generated by the output compare function.
	TMCIV	29	Input	External event input pin.
	TMRIV	28	Input	Counter reset input pin.
	TRGV	54	Input	Counter start trigger input pin.

2.8 Usage Notes

2.8.1 Notes on Data Access to Empty Areas

The address space of this LSI includes empty areas in addition to the ROM, RAM, and on-chip I/O registers areas available to the user. When data is transferred from CPU to empty areas, the transferred data will be lost. This action may also cause the CPU to malfunction. When data is transferred from an empty area to CPU, the contents of the data cannot be guaranteed.

2.8.2 EEPMOV Instruction

EEPMOV is a block-transfer instruction and transfers the byte size of data indicated by R4L, which starts from the address indicated by R5, to the address indicated by R6. Set R4L and R6 so that the end address of the destination address (value of R6 + R4L) does not exceed H'FFFF (the value of R6 must not change from H'FFFF to H'0000 during execution).

2.8.3 Bit-Manipulation Instruction

The BSET, BCLR, BNOT, BST, and BIST instructions read data from the specified address in byte units, manipulate the data of the target bit, and write data to the same address again in byte units. Special care is required when using these instructions in cases where two registers are assigned to the same address, or when a bit is directly manipulated for a port or a register containing a write-only bit, because this may rewrite data of a bit other than the bit to be manipulated.

(1) Bit manipulation for two registers assigned to the same address

Example 1: Bit manipulation for the timer load register and timer counter

(Applicable for timer B1 in the H8/36057 Group and H8/36037 Group.)

Figure 2.13 shows an example of a timer in which two timer registers are assigned to the same address. When a bit-manipulation instruction accesses the timer load register and timer counter of a reloadable timer, since these two registers share the same address, the following operations takes place.

1. Data is read in byte units.
2. The CPU sets or resets the bit to be manipulated with the bit-manipulation instruction.
3. The written data is written again in byte units to the timer load register.

Table 7.7 Flash Memory Operating States

	Flash Memory Operating State	
LSI Operating State	**PDWND = 0 (Initial Value)**	**PDWND = 1**
Active mode	Normal operating mode	Normal operating mode
Subactive mode	Power-down mode	Normal operating mode
Sleep mode	Normal operating mode	Normal operating mode
Subsleep mode	Standby mode	Standby mode
Standby mode	Standby mode	Standby mode

9.7 Port 9

Port 9 is a general I/O port also functioning as a TinyCAN I/O pin and an SSU I/O pin. Each pin of the port 9 is shown in figure 9.7.

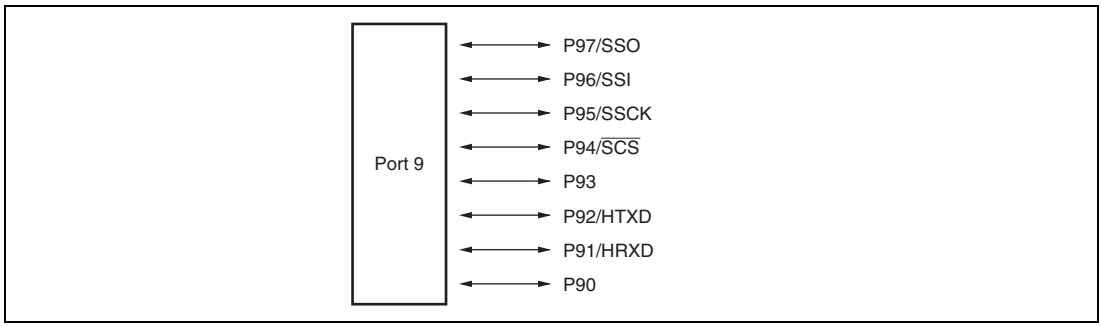

Figure 9.7 Port 9 Pin Configuration

Port 9 has the following registers.

- Port control register 9 (PCR9)
- Port data register 9 (PDR9)

9.7.1 Port Control Register 9 (PCR9)

PCR9 selects inputs/outputs in bit units for pins to be used as general I/O ports of port 9.

Bit	Bit Name	Initial Value	R/W	Description
7	PCR97	0	W	When each of the port 9 pins P97 to P90 functions as a general I/O port, setting a PCR9 bit to 1 makes the corresponding pin an output port, while clearing the bit to 0 makes the pin an input port.
6	PCR96	0	W	
5	PCR95	0	W	
4	PCR94	0	W	
3	PCR93	0	W	
2	PCR92	0	W	
1	PCR91	0	W	
0	PCR90	0	W	

Bit	Bit Name	Initial Value	R/W	Description
1	OS1	0	R/W	Output Select 1 and 0
0	OS0	0	R/W	These bits select an output method for the TMOV pin by the compare match of TCORA and TCNTV. 00: No change 01: 0 output 10: 1 output 11: Output toggles

OS3 and OS2 select the output level for compare match B. OS1 and OS0 select the output level for compare match A. The two output levels can be controlled independently. After a reset, the timer output is 0 until the first compare match.

11.3.5 Timer Control Register V1 (TCRV1)

TCRV1 selects the edge at the TRGV pin, enables TRGV input, and selects the clock input to TCNTV.

Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	All 1	—	Reserved These bits are always read as 1.
4	TVEG1	0	R/W	TRGV Input Edge Select
3	TVEG0	0	R/W	These bits select the TRGV input edge. 00: TRGV trigger input is prohibited 01: Rising edge is selected 10: Falling edge is selected 11: Rising and falling edges are both selected
2	TRGE	0	R/W	TCNT starts counting up by the input of the edge which is selected by TVEG1 and TVEG0. 0: Disables starting counting-up TCNTV by the input of the TRGV pin and halting counting-up TCNTV when TCNTV is cleared by a compare match. 1: Enables starting counting-up TCNTV by the input of the TRGV pin and halting counting-up TCNTV when TCNTV is cleared by a compare match.

Example of Input Capture Operation: Figure 12.17 shows an example of input capture operation.

In this example, both rising and falling edges have been selected as the FTIOA pin input capture input edge, the falling edge has been selected as the FTIOB pin input capture input edge, and counter clearing by GRB input capture has been designated for TCNT.

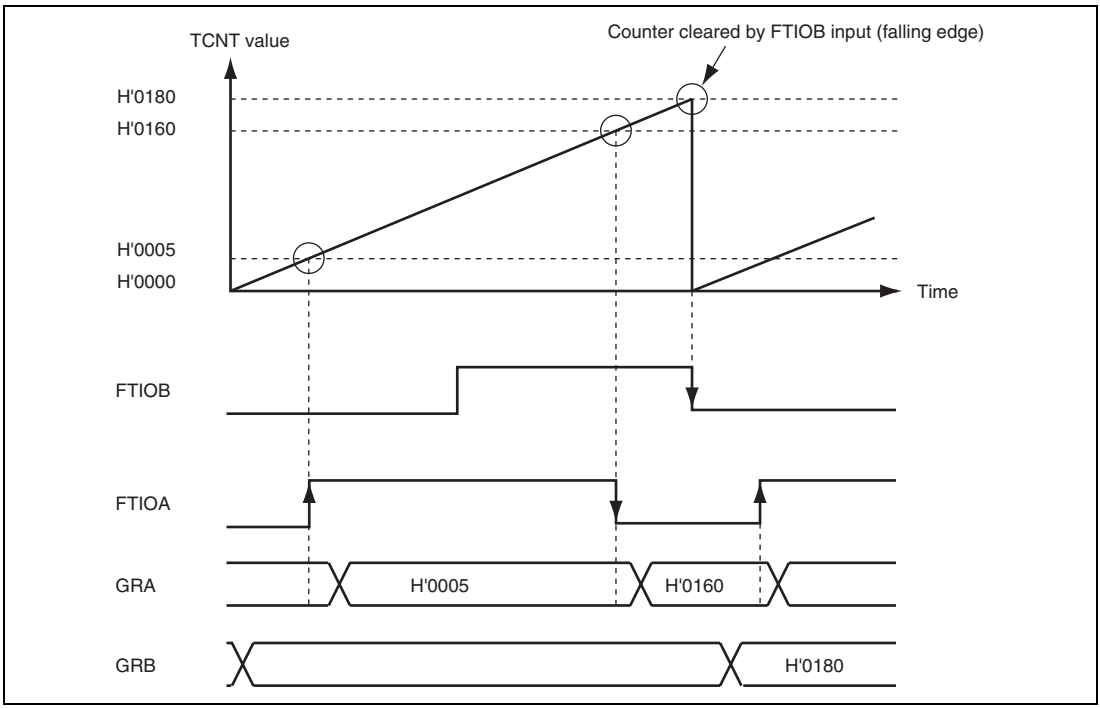

Figure 12.17 Example of Input Capture Operation

Input Capture Signal Timing: Input capture on the rising edge, falling edge, or both edges can be selected through settings in TIOR. Figure 12.18 shows the timing when the rising edge is selected. The pulse width of the input capture signal must be at least two system clock (ϕ) cycles.

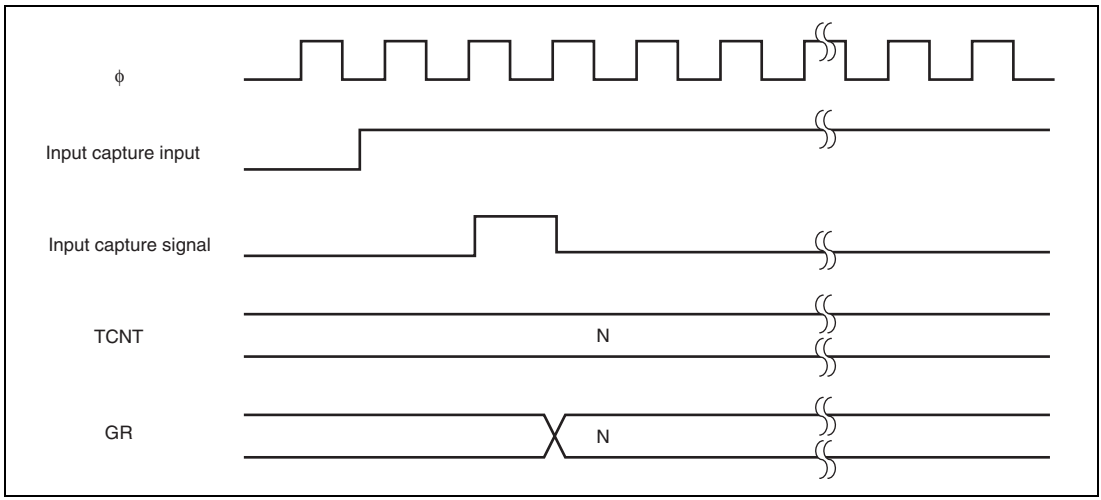

Figure 12.18 Input Capture Signal Timing

Contention between GR Read and Input Capture: If an input capture signal is generated in the T_1 state of a GR read cycle, the data that is read will be transferred before input capture transfer. Figure 12.56 shows the timing in this case.

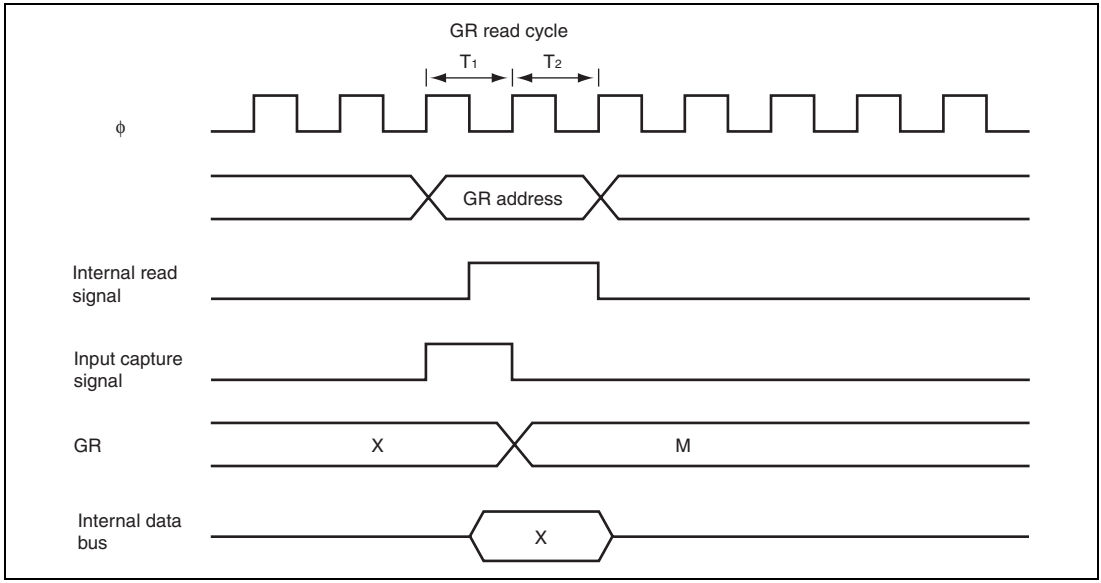

Figure 12.56 Contention between GR Read and Input Capture

Table 14.5 Examples of BRR Settings for Various Bit Rates (Clocked Synchronous Mode) (1)

Bit Rate (bit/s)	Operating Frequency φ (MHz)									
	2		4		8		10		16	
	n	N	n	N	n	N	n	N	n	N
110	3	70	—	—	—	—	—	—		
250	2	124	2	249	3	124	—	—	3	249
500	1	249	2	124	2	249	—	—	3	124
1k	1	124	1	249	2	124	—	—	2	249
2.5k	0	199	1	99	1	199	1	249	2	99
5k	0	99	0	199	1	99	1	124	1	199
10k	0	49	0	99	0	199	0	249	1	99
25k	0	19	0	39	0	79	0	99	0	159
50k	0	9	0	19	0	39	0	49	0	79
100k	0	4	0	9	0	19	0	24	0	39
250k	0	1	0	3	0	7	0	9	0	15
500k	0	0*	0	1	0	3	0	4	0	7
1M			0	0*	0	1	—	—	0	3
2M					0	0*	—	—	0	1
2.5M							0	0*	—	—
4M									0	0*

[Legend]

Blank: No setting is available.

—: A setting is available but error occurs.

*: Continuous transfer is not possible.

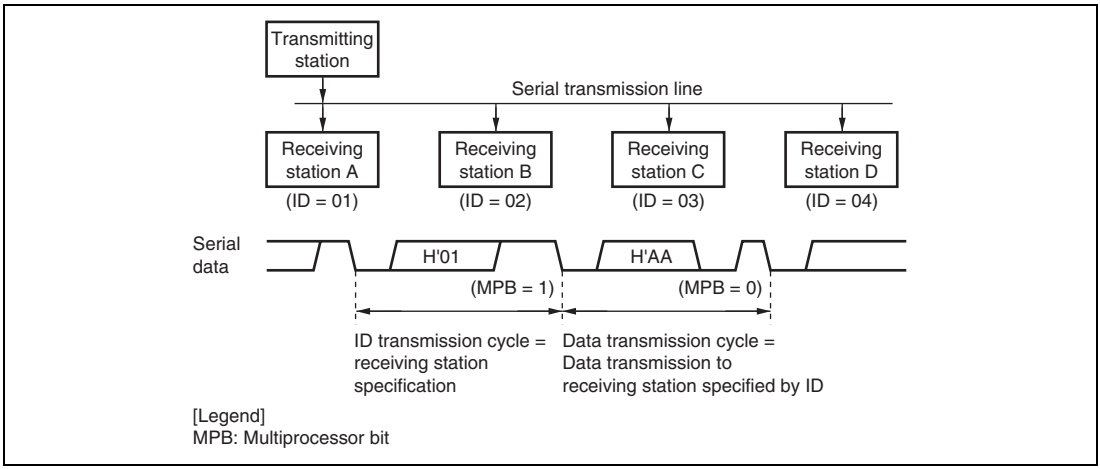

Figure 14.15 Example of Inter-Processor Communication Using Multiprocessor Format (Transmission of Data H'AA to Receiving Station A)

14.6.1 Multiprocessor Serial Data Transmission

Figure 14.14 shows a sample flowchart for multiprocessor serial data transmission. For an ID transmission cycle, set the MPBT bit in SSR to 1 before transmission. For a data transmission cycle, clear the MPBT bit in SSR to 0 before transmission. All other SCI3 operations are the same as those in asynchronous mode.

Section 15 Controller Area Network for Tiny (TinyCAN)

The TinyCAN is a module for controlling a controller area network (CAN) for realtime communication in vehicular and industrial equipment systems, etc and conforms to the Bosch 2.0B active. For details on CAN specifications, refer to Bosch CAN Specification Version 2.0 1991, Robert Bosch GmbH.

15.1 Features

- CAN version: Conforms to Bosch 2.0B active
  Communication systems: NRZ (Non-Return to Zero) system (with bit-stuffing function)
  Broadcast communication system
  Transmission path: Bidirectional 2-wire serial communication
  Communication speed: Max. 1 Mbps
  Data length: 0 to 8 bytes
- Data buffers
  Four (one receive-only buffer and three buffers settable for transmission/reception)
- Data transmission
  Mailbox (buffer) number order (high-to-low)
- Data reception
  Message identifier match
  Reception with message identifier masked
  Supports four buffers for the filter mask
- CPU interrupt sources
  Various error interrupts
  Reset/Halt mode processing interrupt
  Message reception interrupt
  Message transmission interrupt
- TinyCAN operating modes
  Software reset
  Normal status (error-active, error-passive)
  Bus off state
  Configuration mode
  Halt mode
  Module standby mode

Bit	Bit Name	Initial Value	R/W	Description
6	BOFIM	1	R/W	Bus Off Interrupt Mask Enables or disables a bus-off interrupt request. 0: The bus-off interrupt request is enabled 1: The bus-off interrupt request is disabled
5	EPIM	1	R/W	Error Passive Interrupt Mask Enables or disables an error passive interrupt request. 0: The error passive interrupt request is enabled 1: The error passive interrupt request is disabled
4	ROWIM	1	R/W	Receive Overload Warning Interrupt Mask Enables or disables an interrupt request for a receive overload warning. 0: The interrupt request for the receive overload warning is enabled 1: The interrupt request for the receive overload warning is disabled
3	TOWIM	1	R/W	Transmit Overload Warning Interrupt Mask Enables or disables an interrupt request for a transmit overload warning. 0: The interrupt request for the transmit overload warning is enabled 1: The interrupt request for the transmit overload warning is disabled
2	RFRIM	1	R/W	Remote Frame Request Interrupt Mask Enables or disables an interrupt request for a remote frame request. 0: The interrupt request for the remote frame request is enabled 1: The interrupt request for the remote frame request is disabled
1	DFRIM	1	R/W	Data Frame Receive Message Interrupt Mask Enables or disables an interrupt request for a data frame receive message. 0: The interrupt request for the data frame receive message is enabled 1: The interrupt request for the data frame receive message is disabled

15.5.3 Message Transmission

Message Transmission Request: Figure 15.6 shows a transmission flowchart.

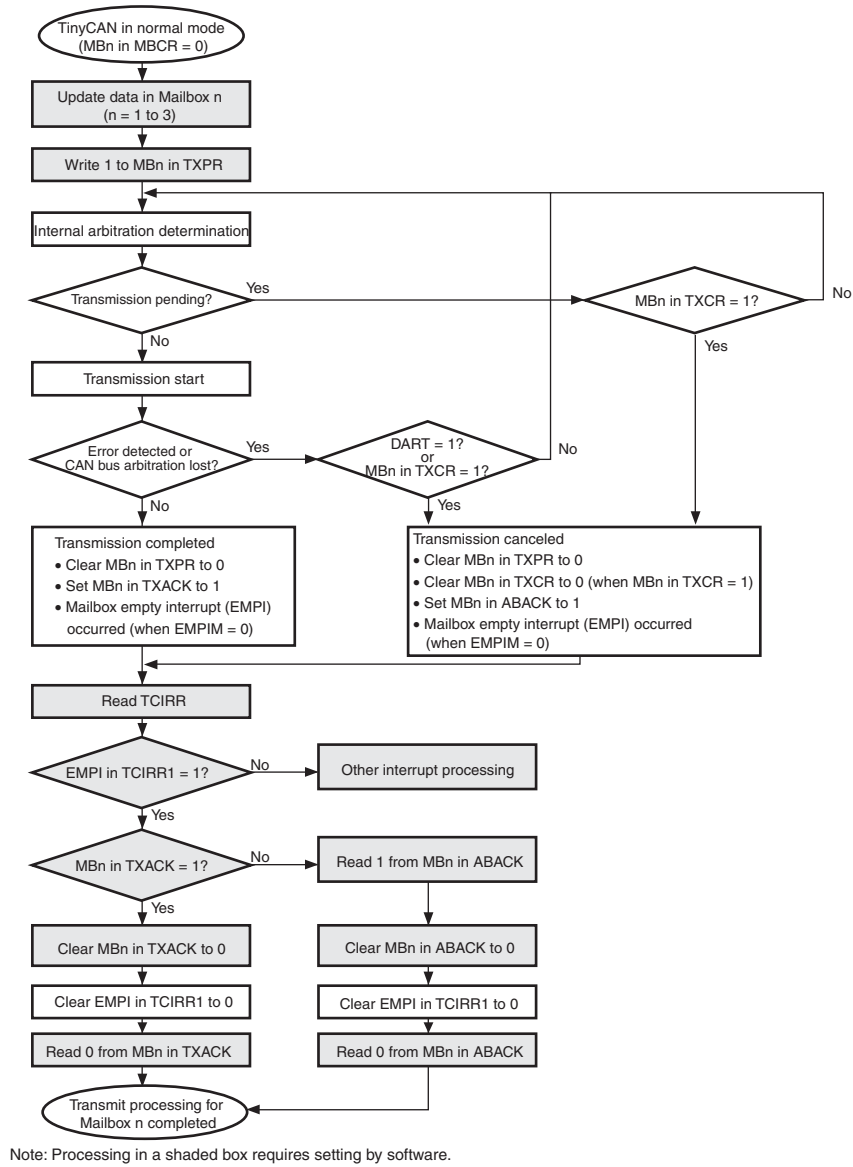

Figure 15.6 Transmission Request Flowchart

Bit	Bit Name	Initial Value	R/W	Description
3	TEND	0	R/W	Transmit End [Setting condition] • When the last bit of data is transmitted, the TDRE bit is 1 [Clearing conditions] • When 0 is written to this bit after reading 1 • When data is written in SSTDR
2	TDRE	1	R/W	Transmit Data Empty [Setting conditions] • When the TE bit in SSER is 0 • When data transfer is performed from SSTDR to SSTRSR and data can be written in SSTDR [Clearing conditions] • When 0 is written to this bit after reading 1 • When data is written in SSTDR
1	RDRF	0	R/W	Receive Data Register Full [Setting condition] • When serial reception is completed normally and receive data is transferred from SSTRSR to SSRDR [Clearing conditions] • When 0 is written to this bit after reading 1 • When data is read from SSRDR
0	CE	0	R/W	Conflict Error Flag [Setting conditions] • When serial communication is started while SSUMS = 1 and MSS =1, the $\overline{SCS}$ pin input is low • When the $\overline{SCS}$ pin level changes from low to high during transfer while SSUMS = 1 and MSS = 0 [Clearing condition] • When 0 is written to this bit after reading 1

17.2 Register Descriptions

The subtimer has the following registers.

- Subtimer control register (SBTCTL)
- Subtimer counter (SBTDCNT)
- Ring oscillator prescaler setting register (ROPCR)

17.2.1 Subtimer Control Register (SBTCTL)

SBTCTL controls oscillation of the on-chip oscillator, subclock output, and counter operation and indicates the operating state. SBTCTL is initialized to H'60.

Bit	Bit Name	Initial Value	R/W	Description
7	PCEF	0	R/W	Division Count End Flag [Setting condition] When counting starts at the first falling edge and SBTPS halts at the third falling edge after the on-chip oscillator starts oscillation. [Clearing condition] When 0 is written to this bit after reading 1
6, 5	—	All 1	—	Reserved These bits are always read as 1.
4	START	0	R/W	Count Down Start Starts or halts the SBTDCNT operation. 0: SBTDCNT halts counting down. 1: SBTDCNT starts counting down.
3	OSCEB	0	R/W	On-Chip Oscillator Oscillation Enable Enables or disables the oscillation of the on-chip oscillator. 0: Oscillation of on-chip oscillator is disabled. 1: Oscillation of on-chip oscillator is enabled.

17.5 Usage Notes

17.5.1 Clock Supply to Watchdog Timer

When the on-chip oscillator for the subtimer is used to supply clocks to the watchdog timer, the setting is necessary not only for the subtimer but also for the watchdog timer. For details, refer to section 13, Watchdog Timer.

17.5.2 Writing to ROPCR

ROPCR must be written to in active mode with the PCEF bit in SBTCTL set to 1. Otherwise, the subtimer may operate incorrectly.

22.2.6 Flash Memory Characteristics

Table 22.9 Flash Memory Characteristics

V_{CC} = 3.0 to 5.5 V, V_{SS} = 0.0 V, T_a = –20 to +75°C (regular specifications) or T_a = –40 to +85°C (wide-range specifications), unless otherwise indicated.

Item		Symbol	Test Condition	Values Min.	Typ.	Max.	Unit
Programming time (per 128 bytes)*1*2*4		t_P		—	7	200	ms
Erase time (per block) *1*3*6		t_E		—	100	1200	ms
Reprogramming count		N_{WEC}		1000	10000	—	Times
Programming	Wait time after SWE bit setting*1	x		1	—	—	µs
	Wait time after PSU bit setting*1	y		50	—	—	µs
	Wait time after P bit setting *1*4	z1	1 ≤ n ≤ 6	28	30	32	µs
		z2	7 ≤ n ≤ 1000	198	200	202	µs
		z3	Additional-programming	8	10	12	µs
	Wait time after P bit clear*1	α		5	—	—	µs
	Wait time after PSU bit clear*1	β		5	—	—	µs
	Wait time after PV bit setting*1	γ		4	—	—	µs
	Wait time after dummy write*1	ε		2	—	—	µs
	Wait time after PV bit clear*1	η		2	—	—	µs
	Wait time after SWE bit clear*1	θ		100	—	—	µs
	Maximum programming count *1*4*5	N		—	—	1000	Times

22.3.4 A/D Converter Characteristics

Table 22.18 A/D Converter Characteristics

V_{CC} = 2.7 to 5.5 V, V_{SS} = 0.0 V, T_a = –20 to +75°C (regular specifications) or T_a = –40 to +85°C (wide-range specifications), unless otherwise indicated.

Item	Symbol	Applicable Pins	Test Condition	Values			Unit	Reference Figure
				Min.	Typ.	Max.		
Analog power supply voltage	AV_{CC}	AV_{CC}		3.3	V_{CC}	5.5	V	*1
Analog input voltage	AV_{IN}	AN0 to AN7		V_{SS} – 0.3	—	AV_{CC} + 0.3	V	
Analog power supply current	AI_{OPE}	AV_{CC}	AV_{CC} = 5.0 V f_{OSC} = 20 MHz	—	—	2.0	mA	
	AI_{STOP1}	AV_{CC}		—	50	—	µA	*2 Reference value
	AI_{STOP2}	AV_{CC}		—	—	5.0	µA	*3
Analog input capacitance	C_{AIN}	AN0 to AN7		—	—	30.0	pF	
Allowable signal source impedance	R_{AIN}	AN0 to AN7		—	—	5.0	kΩ	
Resolution (data length)				10	10	10	bit	
Conversion time (single mode)			AV_{CC} = 3.3 to 5.5 V	134	—	—	t_{cyc}	
Nonlinearity error				—	—	±7.5	LSB	
Offset error				—	—	±7.5	LSB	
Full-scale error				—	—	±7.5	LSB	
Quantization error				—	—	±0.5	LSB	
Absolute accuracy				—	—	±8.0	LSB	
Conversion time (single mode)			AV_{CC} = 4.0 to 5.5 V	70	—	—	t_{cyc}	
Nonlinearity error				—	—	±7.5	LSB	
Offset error				—	—	±7.5	LSB	
Full-scale error				—	—	±7.5	LSB	
Quantization error				—	—	±0.5	LSB	
Absolute accuracy				—	—	±8.0	LSB	

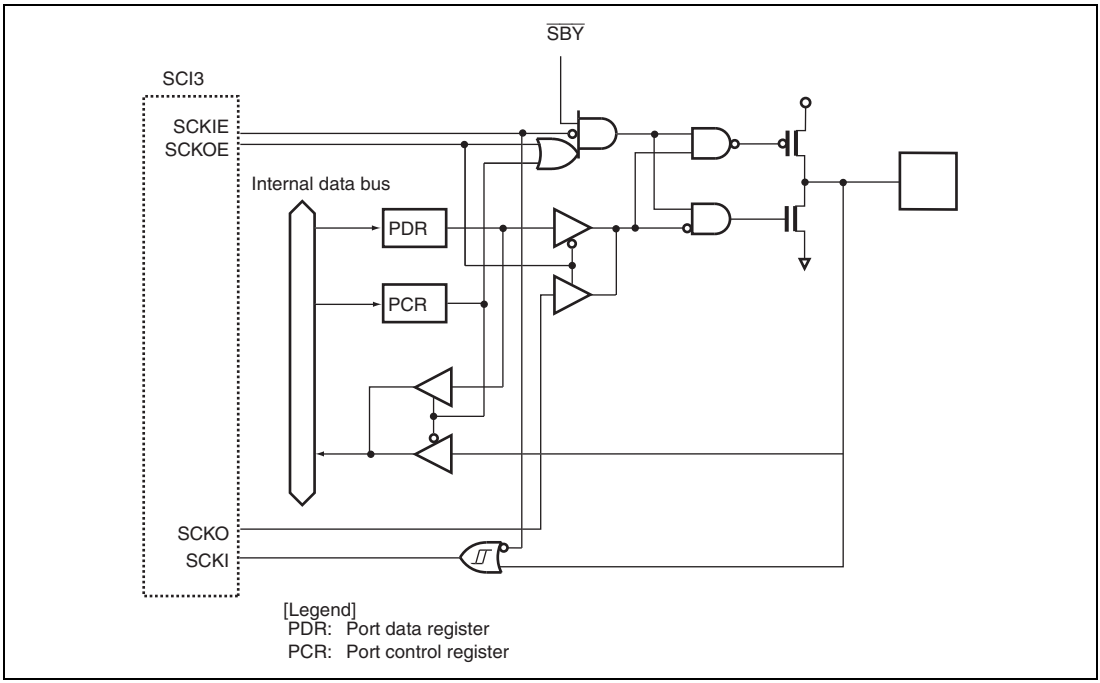

Figure B.8 Port 2 Block Diagram (P20)

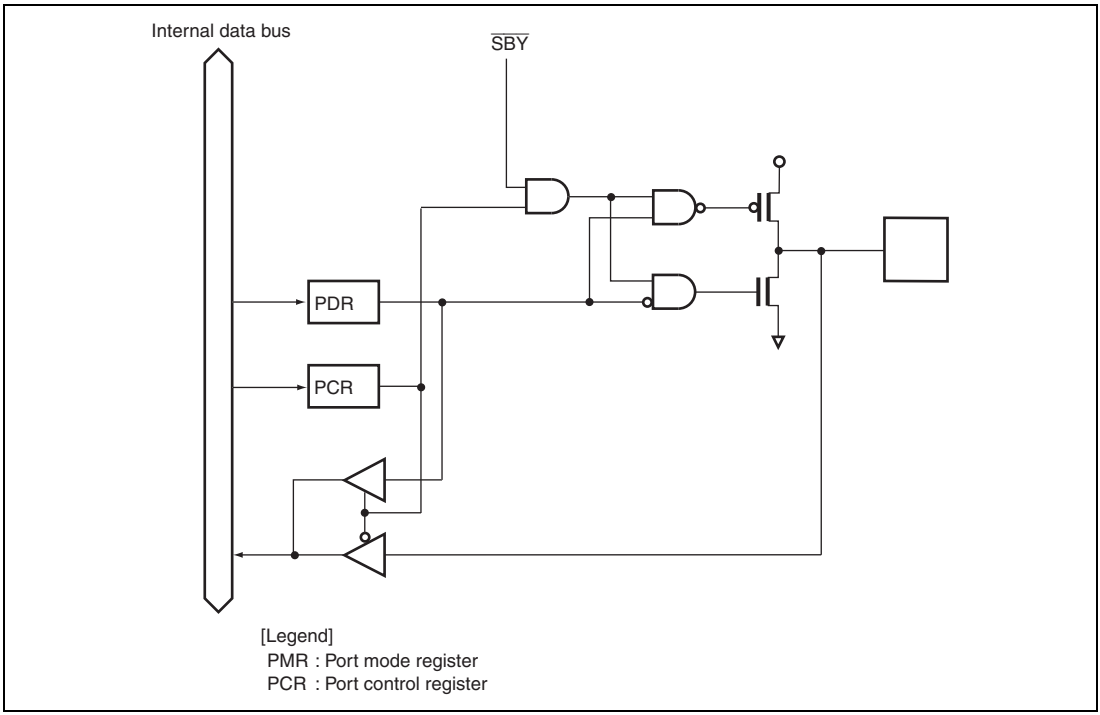

Figure B.22 Port 9 Block Diagram (P94, P95)